Intel® Stratix® 10 GX Production Device Errata
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**Intel® Stratix® 10 GX Production Device Errata**

This errata sheet provides information about known device issues affecting Intel® Stratix® 10 GX devices.

**Device Errata for the Intel Stratix 10 GX L-Tile Devices**

This section lists the errata that apply to the Intel Stratix 10 GX L-Tile production devices. Each listed erratum has an associated status that identifies any planned fixes.

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Device Power Supply, Core, Configuration and I/O

Power-on Configuration Intermittent Configuration Failures

Description

Your device may encounter intermittent configuration failures if it is not programmed with at least 256 kB of configuration data within 18 seconds after completion of the power up sequence. This erratum does not apply to FPGA reconfiguration, provided a successful configuration was completed after the power up sequence. If the nSTATUS pin remains low for 110 ms after toggling the nCONFIG pin from low to high, it may indicate you have encountered this issue. To confirm, toggle nCONFIG again and if the nSTATUS pin remains low for another 10 ms, then you have confirmed the failure.

Note: Configuration via Protocol (CvP) that uses an open or closed PCIe system must also adhere to the above requirements for successful configuration.

Workaround

Hardware workaround: Use a MOSFET as a switch to briefly toggle the VCCIO_SDM voltage level when the host is ready to configure the FPGA using an arrangement as shown in the figure below.

Figure 1. Hardware Workaround
Software workaround: Configure your FPGA with a dummy design within 18 seconds of the power up sequence completion. When the system is ready to configure, then reconfigure with the full design. Note the following considerations regarding the software workaround:

- For Intel Quartus® Prime Pro Edition versions prior to 18.0:
  - You must use the same version of Intel Quartus Prime Pro Edition to create the first programmed bitstream and any subsequent programmed bitstreams.

- For Intel Quartus Prime Pro Edition version 18.0:
  - You can ensure compatibility of Intel Quartus Prime Pro Edition version 18.0 with future versions of Intel Quartus Prime Pro Edition by installing patch 0.13 for Microsoft® Windows® 10 or patch 0.13 for Linux®. To install patch 0.13, you must have Intel Quartus Prime Pro Edition version 18.0 installed. For more information, refer to the associated Knowledge Base entry.

- For Intel Quartus Prime Pro Edition versions after 18.0:
  - You can create subsequent configuration files with any Intel Quartus Prime Pro Edition version later than 18.0.

Status

Affects: Intel Stratix 10 GX 2800 and GX 2500 L-Tile production devices

Status: If you are using an Intel Stratix 10 GX 2800 or 2500 L-Tile device and a fix is required, move to the Intel Stratix 10 SX 2800/2500 L-Tile device, which is drop-in compatible.

Device Security Features

Description

If you intend to use the device security features, please contact Intel Premier Support.

Status

Affects: Intel Stratix 10 GX 2800 and GX 2500 L-Tile production devices

Status: No planned fix

Unexpected AVST_READY Signal Behavior After Power-On-Reset (POR)

After powering up the FPGA device power supplies in the proper sequence, the device asserts a Power On Reset (POR). When you drive the nCONFIG pin high, subsequently the nSTATUS pin goes high. If you use either of the Avalon-ST configuration scheme(s) (32/16/8 bits), you may notice an unexpected low pulse (20 to 100 µs) on AVST_READY pin.

Figure 2. Timing Diagram
If you begin the configuration via Avalon-ST scheme by driving the AVST_VALID pin high before the unexpected AVST_READY low pulse (20 to 100 µs), then the configuration will be unsuccessful.

**Note:**
This issue only impacts the first configuration after POR, it does not impact the subsequent reconfiguration attempts.

**Workaround**

After the nCONFIG and nSTATUS pins are high, wait for 500 µs before you monitor the AVST_READY pin and drive the AVST_VALID pin to initiate the Avalon-ST configuration.

**Status**

Affects:
- Intel Stratix 10 GX 2800 L-Tile production devices
- Intel Stratix 10 GX 2500 L-Tile production devices

Status: No planned fix.
Transceivers

On-Die Instrumentation (ODI) Availability

**Description**

On-die instrumentation (ODI) (Eye-Q) is not available in Intel Stratix 10 devices that use the transceiver L-tile.

**Workaround**

None

**Status**

Affects:

- Intel Stratix 10 GX L-Tile Production

Status: No planned fix.

PCI Express Tile Usage Restrictions

**Description**

If any transceiver channels share a tile with active PCI Express interfaces that are Gen2 or Gen3 capable and bonded with more than two lanes (x4, x8, x16), the maximum data rate supported for the non-PCIe channels in those tiles is 6.5 Gbps. This restriction applies to both Hard IP and Soft IP implementations for the active PCI Express interfaces.

Running the neighboring transceiver channels within the same tile at data rates faster than 6.5 Gbps may result in bit errors being observed during a PCIe speed change. Transceiver channels that share a tile with active PCI Express interfaces that are only Gen1 capable are not impacted.

**Workaround**

- Avoid placing other transceiver instances above 6.5 Gbps data rates in the same tile as PCIe channels that are Gen2 or Gen3 capable.
- Bring up the PCIe channels first, followed by non-PCIe channels.

**Status**

Affects:

- Intel Stratix 10 GX L-Tile Production (in PIPE mode)

Status: Fixed in:

- Intel Stratix 10 GX L-Tile Production (in Hard IP mode)

Device Errata for the Intel Stratix 10 GX H-Tile Devices

This section lists the errata that apply to the Intel Stratix 10 GX H-Tile production devices. Currently, there are no known issues.
# Revision History of Intel Stratix 10 GX Production Device Errata

<table>
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<th>Document Version</th>
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</table>
| 2018.11.20       | • Added new erratum:  
|                  |   — *Unexpected AVST READY Signal Behavior After Power-On-Reset (POR).*  
|                  |   — *On-Die Instrumentation (ODI) Availability*  
|                  |   — *PCI Express Tile Usage Restrictions*  
|                  | • Added a new section: *Device Errata for the Intel Stratix 10 GX H-Tile Devices.* |
| 2018.10.05       | Made the following changes:  
|                  | • Updated the "Power-on Configuration Intermittent Configuration Failures" section. |
| 2018.07.09       | Made the following changes:  
|                  | • Updated the "Power-on Configuration Intermittent Configuration Failures" section. |
| 2018.02.05       | Initial release. |

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