This document addresses known errata and documentation issues for the QDRII SRAM Controller MegaCore® function version 1.3.0. Errata are functional defects or errors, which may cause the QDRII SRAM Controller MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the QDRII SRAM Controller MegaCore function v1.3.0.

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For the most up-to-date errata for this release, refer to the errata page on the Altera® website:

QDRII SRAM Controller MegaCore Function v1.3.0 Issues

This section describes the QDRII SRAM Controller MegaCore function v1.3.0 issues.

Simulator Error With qdrii_cq Signal

In non-DQS mode the QDRII SRAM controller generates an unused signal: qdrii_cq. Some simulators may issue an error message about the unused signal and fail to simulate.

Affected Configurations

This issue affects all non-DQS mode QDRII SRAM controllers.

Design Impact

The design does not simulate.

Workaround

For non-DQS mode designs, in the IP Toolbench-generated top-level design, connect the qdrii_cq signal to a static 1 or static 0.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

TimeQuest Timing Analyzer Failure

When you use the Quartus II TimeQuest timing analyzer, it reports a recovery issue, because the reset is not in the same clock domain as the system clock.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Change the reset sequence for the signals clocked on the CQ clock, before you run the TimeQuest analyzer.
**Solution Status**

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

**Simulating with the VCS Simulator**

The QDRII SRAM Controller MegaCore function v1.3.0 does not support the VCS simulator.

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

The design does not simulate.

**Workaround**

There is no workaround for VHDL simulations. For Verilog HDL simulations, change line 154 in the `qdrii_model.v` file to:

```
begin : f1
```

Also, change line 417 to:

```
begin : f2
```

**Solution Status**

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

**Pin Planner Nonoperational**

The Quartus II Pin Planner code in the add constraints script does not work with custom variations with device width or device depth of greater than one.

**Affected Configurations**

This issue affects all configurations with a device width or depth greater than 1.
Design Impact
The design does not compile.

Workaround
Ensure you select 1 for **Device depth** and **Device width** on the IP Toolbench Memory tab.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

PLL Placement
The IP Toolbench-generated example design uses a PLL phase shift of 90°, which can cause the design to miss hold timing analysis. The source synchronous PLL for the read capture should have a location constraint to place it on the same side of the device as the Q pins, otherwise, the source synchronous compensation does not compensate for the expected delays.

Affected Configurations
This issue affects all configurations.

Design Impact
The design misses hold timing analysis.

Workaround
The PLL must be located on the same side of the device as the CQ/CQN groups, for the PLL to compensate properly.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

IP Toolbench Allows Editing of Memory Devices
When you choose a memory device other than **Default** in the memory device list, all the following parameters are set for that specific device:

- Data width
Address width
Burst type

If you change any of these parameters, you no longer have the correct parameters for the chosen memory device, but instead have parameters for a custom memory device. However, IP Toolbench incorrectly indicates that you still have a specific device rather than a custom device, in the memory devices list.

Affected Configurations
This issue affects all noncustom configurations.

Design Impact
There is a design impact if you choose incompatible data width, address width, or burst type parameters for your chosen memory.

Workaround
If you edit any of the following parameters, choose Default in the memory device list:

Data width
Address width
Burst type

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Constraints Errors With Companion Devices
When you change the device in your project or add a HardCopy II companion device to a Stratix II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

Affected Configurations
This issue affects all configurations.
Design Impact
The design fails.

Workaround
Reassign the byte groups for the new device in the constraints editor.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Supported Device Families
The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy® II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard® Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot compile a design.

Workaround
Ensure you choose a supported device family for the Quartus II project.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

No Description of Datapath Signals
The QDRII SRAM Controller MegaCore Function User Guide does not describe the controller’s internal signals that interface the datapath to the control logic and the resynchronization logic. For the signal descriptions, contact Altera mySupport.
Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

For the signal descriptions, contact Altera mySupport.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore Function User Guide.

Changing HDL

Be aware that when you change the HDL (Verilog HDL to VHDL or VHDL to Verilog HDL) of your custom variation. IP Toolbench does not delete all the necessary files and during compilation the Quartus II software may try to access incorrect files, which results in errors.

Affected Configurations

This issue affects all configurations.

Design Impact

When you choose Start Compilation, there may be error messages and the design may not compile.

Workaround

If you change which HDL you use, ensure you remove all unnecessary files from the Quartus II project.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.
Compilation Error When You Choose ByteGroups On the Top & Bottom of the Device (Stratix II Series & HardCopy II Devices Only)

You will see an error during compilation if in the Constraints window you choose bytegroups on the top and the bottom of a Stratix II series or HardCopy II device.

Affected Configurations
This issue affects all Stratix II series and HardCopy II devices.

Design Impact
When you choose Start Compilation, there is an error message and the design does not compile.

Workaround
If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytegroups on either the top or the bottom of the device, but not both.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects <project name>.vho or .vo and <project name>_v or _vhd.sdo files to be present.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot run gate-level simulations.
Workaround

For VHDL gate-level simulations, in the `simulation/modelsim` directory follow these steps:

1. Rename `<filename>.vho` file to `<project name>.vho`.
2. Rename `<filename>.sdo` file to `<project name>_vhd.sdo`.

For Verilog HDL gate-level simulations, in the `simulation/modelsim` directory follow these steps:

1. Rename the `<filename>.vo` file to `<project name>.vo`.
2. Rename the `<filename>.sdo` file to `<project name>_v.sdo`.
3. In the `<project name>.vo` file change the following line to point to the `<project name>_v.sdo` file:

   ```
   initial $sdf_annotate("<project name>_v.sdo");
   ```

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

The ModelSim Script Does Not Support Companion Devices

If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

Affected Configurations

This issue affects designs with companion devices.

Design Impact

The simulation script does not run.

Workaround

Edit the Modelsim script to include the correct libraries.
Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

No Performance Numbers In The User Guide

The QDRII SRAM Controller MegaCore Function User Guide does not list the following QDRII SRAM performance.

Stratix II devices support QDRII SRAM at up to 250 MHz/1,000 Megabits per second (Mbps). Stratix and Stratix GX devices support QDRII SRAM at up to 200 MHz/800 Mbps. Tables 2 through 4 show the clock frequency support for each device family.

<table>
<thead>
<tr>
<th>Table 2. QDRII SDRAM Maximum Clock Frequency Support in Stratix II Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed Grade</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>–3</td>
</tr>
<tr>
<td>–4</td>
</tr>
<tr>
<td>–5</td>
</tr>
</tbody>
</table>

Notes to Table 2:
1. This analysis is based on the EP2S90F1020 device. Ensure you perform a timing analysis for your chosen FPGA.
2. These numbers are from the Quartus II software, version 5.1. Altera recommends using the latest version of the Quartus II software for your design.
3. These numbers apply to both commercial and industrial devices.

<table>
<thead>
<tr>
<th>Table 3. QDRII SRAM Maximum Clock Frequency Supported in Stratix &amp; Stratix GX Devices (EP1S10 to EP1S40 &amp; EP1SGX10 to EP1SGX40 Devices)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed Grade</strong></td>
</tr>
<tr>
<td>–5</td>
</tr>
<tr>
<td>–6</td>
</tr>
<tr>
<td>–7</td>
</tr>
</tbody>
</table>

Notes to Table 3:
1. This analysis is based on the EP1S25F1020 device. Ensure you perform a timing analysis for your chosen FPGA.
2. These numbers are from the Quartus II software, version 5.1. Altera recommends using the latest version of the Quartus II software for your design.
3. These numbers apply to both commercial and industrial devices.
### Table 4. QDRII SRAM Maximum Clock Frequency Supported in Stratix Devices (EP1S60 to EP1S80 Devices)

<table>
<thead>
<tr>
<th>Speed Grade</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–5</td>
<td>167</td>
</tr>
<tr>
<td>–6</td>
<td>167</td>
</tr>
<tr>
<td>–7</td>
<td>133</td>
</tr>
</tbody>
</table>

**Notes to Table 4:**
1. This analysis is based on the EP1S60F1020 device. Ensure you perform a timing analysis for your chosen FPGA.
2. These numbers are from the Quartus II software, version 5.1. Altera recommends using the latest version of the Quartus II software for your design.
3. These numbers apply to both commercial and industrial devices.

**Affected Configurations**

This issue has no effects.

**Design Impact**

There is no design impact.

**Workaround**

There is no workaround.

**Solution Status**

This issue will be fixed in the next version of the QDRII SRAM Controller MegaCore Function User Guide.

**Contact Information**

For more information, contact Altera’s mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click Create New Service Request. Choose the Product Related Request form.
Revision History

Table 5 shows the errata sheet revision history for the QDRII SRAM Controller MegaCore function v1.3.0.

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<tr>
<th>Version</th>
<th>Date</th>
<th>Errata Summary</th>
</tr>
</thead>
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| 1.2     | October 2006 | Added the following issues:  
  - Simulator Error With qdrii_cq Signal  
  - TimeQuest Timing Analyzer Failure  
  - Simulating with the VCS Simulator |
| 1.1     | May 2006  | Removed six erroneous errata issues.  
  - Added Pin Planner Nonoperational issue. |
| 1.0     | April 2006 | First release.                                                                 |