This document addresses known errata and documentation issues for the DDR and DDR2 SDRAM Controller Compiler version 3.4.1. Errata are functional defects or errors, which may cause the DDR and DDR2 SDRAM Controller Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the DDR and DDR2 SDRAM Controller Compiler v3.4.1.

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For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

This section describes the DDR and DDR2 SDRAM Controller Compiler v3.4.1 issues.

Simulating with the NCSim Software

The DDR or DDR2 SDRAM Controller MegaCore functions do not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

The following workarounds exist.

VHDL

When using the RTL model described in `generic_ddr2_sdram_rtl.v`, instantiation fails because some parameters in the model have values that are functions of other parameters. Therefore, NCSim cannot determine the data type of those parameters and omits the instantiation. Remove any such parameter value assignments and pass these values as parameters during instantiation. In `generic_ddr2_sdram_rtl.v`, follow these steps:

1. Change lines 89 to 93 to assign integer values, for example:

   ```vhdl
   parameter ROW_BITS         = 13;
   parameter ADDR_BITS        = 13;
   parameter COL_BITS         = 10;
   parameter DQ_BITS          = 8;
   parameter BA_BITS          = 2;
   ```

2. Change the instantiation of the `generic_ddr2_sdram_rtl` Verilog HDL module to assign the correct values to the parameters:

   ```vhdl
   generic map(
     ROWBITS  => ROWBITS,
     DATABITS => DATABITS,
     COLBITS  => COLBITS,
     BANKBITS => BANKBITS,
     ROW_BITS => ROW_BITS,
   )
   ```
ADDR_BITS   => ROWBITS,
COL_BITS    => COLBITS,
DQ_BITS     => DATABITS,
BA_BITS     => BANKBITS
--                    DISABLE_TIMING_CHECK =>
DISABLE_TIMING_CHECK,
--                    memory_spec => memory_spec,
--                    init_file   => init_file
)

3. Set the –relax switch for all calls to the VHDL analyzer.

Verilog HDL
Set the –relax switch for all calls to the VHDL analyzer.

Solution Status
This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

Simulating with the VCS Simulator
The DDR or DDR2 SDRAM Controller MegaCore functions do not fully support the VCS simulator.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not simulate.

Workaround
The following workarounds exist.

VHDL
Change the following code.

- In file `<variation name>_example_driver.vhd`, change all `when statements between lines 333 and 503 from when std_logic_vector’ (“<bit_pattern>”) to when “<bit_pattern>”.`
In file `testbench\<example name>_tb`, change line 191 from

```verilog
signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1',
others => '0')
```

to

```verilog
signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0').
```

**Verilog HDL**

No changes are necessary. Calls to the Verilog analyzer sets the `+v2k` switch to enable Verilog 2000 constructs.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

**Add Constraints Script Overwrites User Clock Pin Assignments**

On Stratix® II designs, the add constraints script applies general IO bank assignments for the clock outputs, so that they are placed in the same IO bank as rest of the interface. If you change the location of the clock outputs to specific pin assignments, running the add constraints script overwrites the specific locations with a more general IO bank assignment. Your design then no longer works in hardware, because the clock output pins are not placed on the correct pin locations.

**Affected Configurations**

This issue affects all Stratix II designs.

**Design Impact**

The design does not function correctly in hardware.

**Workaround**

You should reapply your specific clock pin assignments after each time you run the add constraints script.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.
VHDL Package Declaration Error When Upgrading the MegaCore Function

If you upgrade an existing custom variation of the MegaCore function to v3.4.0, the following error occurs:

```
Error (10624): VHDL Package Declaration error at
auk_ddr_tb_functions.vhd(23): package "auk_ddr_tb_functions" already
exists in the work library
```

IP Toolbench adds files to your Quartus II project when you generate your custom variation. When you upgrade your megaCore function, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.

Affected Configurations

This issue affects all designs that were created in a previous version of the MegaCore function and then upgraded to v3.4.0.

Workaround

From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files’ directory names.

Design Impact

You cannot compile your Quartus II project until you remove the duplicate files.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

Quartus II Timing Analyzer Reports Incorrect Capture Cycles

If you load settings into the DDR Timing Wizard from the DDR or DDR2 SDRAM <variation name>_ddr_settings.txt file, you occasionally get incorrect values for the Resynchronize read data in cycle and Postamble reset control clock in cycle parameters.
**Affected Configurations**

This issue only affects you if you use the DDR Timing Wizard to add timing constraints to DDR or DDR2 SDRAM MegaCore® functions, and import the settings from the MegaCore settings file to the DDR Timing Wizard.

**Design Impact**

The timing margins reported by the Quartus® II Timing Analyzer will be wrong by a complete cycle.

**Workaround**

Edit the **Resynchronize read data in cycle** and **Postamble reset control clock in cycle parameters** and add or remove a cycle to ensure correct timing analysis.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

**Using Regional Clocks**

Versions of the DDR or DDR2 SDRAM MegaCore function before v3.3.1 incorrectly allow the use of regional clocks for the datapath logic.

The static timing analysis performed after the design compiles requires that all the clocks in the datapath are global, but this requirement is not checked version 3.2.0 or earlier.

**Affected Configurations**

This issue affect designs that force the clocks going to the datapath logic onto regional clocks.

**Design Impact**

Timing margins may be incorrect.

**Workaround**

Do not use regional clocks for the datapath logic.
Solution Status
Timing analysis will report an error for these designs in the Quartus II software v5.1 and later.

Some Timing Assignments Are Not Converted To HardCopy II Devices

The Quartus II HardCopy® II migration tool gives warnings about assignments that are not convertible to HardCopy II devices.

When compiling a design that uses the DDR or DDR2 SDRAM MegaCore function, which targets a HardCopy II device, the Quartus II HardCopy II Netlist Writer gives warning messages because it ignores the MAX_DATA_ARRIVAL_SKEW assignments.

Affected Configurations
This issue affects designs that use the DDR or DDR2 SDRAM MegaCore function, which target HardCopy II devices.

Workaround
Ignore these messages because timing analysis for the interface is provided by the DDR Timing Wizard.

Contact Altera Support for more information on DDR and DDR2 SDRAM timing analysis for HardCopy II designs.

Solution Status
This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

Error Message When Recompiling a Project

If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

Error: DDR timing cannot be verified until project has been successfully compiled.

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.
**Affected Configurations**

This issue affects all configurations.

**Design Impact**

The timing script does not verify your design.

**Workaround**

Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

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**Remove Redundant Logic Cells Option (Stratix Devices Only)**

Do not turn on Remove Redundant Logic Cells in the Quartus II software if you are targeting Stratix devices.

**Affected Configurations**

This issue affect all designs targeted at Stratix® devices, if you turn on Remove Redundant Logic Cells in the Quartus II software.

**Design Impact**

For Stratix devices, removing redundant logic cells makes the Quartus II software optimize away the important DQS delay matching buffers that the postamble circuitry uses.

**Workaround**

Ensure you turn off Remove Redundant Logic Cells in the Quartus II software if you are targeting Stratix devices.

**Solution Status**

There are no plans to fix this issue.
SOPC Builder Supported Memory Data Bus Widths

SOPC Builder currently only supports data bus widths that are a power of 2. IP Toolbench does not impose these limitations in the SOPC Builder flow, and can therefore generate bus widths incompatible with SOPC builder, which results in the following error message during SOPC Builder system generation.

ERROR: slave data width (48) for slave ddr_sdram/s1 unexpected

Affected Configurations

This issue affects all configurations that specify data bus widths that are not a power of two when you use the SOPC Builder flow.

Design Impact

You cannot generate the design in SOPC Builder.

Workaround

Ensure you restrict the data bus width parameter in the DDR SDRAM Controller IP Toolbench to a power of 2, for example, 8, 16, 32 or 64.

Solution Status

This issue will be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

Precompile Timing Estimates With Four or More DQS Delay Matching Buffers (Stratix Devices Only)

For Stratix devices, if you turn on Manual postamble control and choose 4 or more for the Number of DQS delay matching buffers, the pre-compile timing estimates in the system timing report for the read postamble enable property are incorrect. The correct timing analysis result is shown in the post-compile timing analysis report after compiling the design in the Quartus II software.

Affected Configurations

This issue affects designs on Stratix devices that require four or more DQS delay matching buffers.

Design Impact

This issue does not affect your design.
**Workaround**

Ignore the pre-compile timing estimates in the system timing report for the read postamble enable property.

**Solution Status**

This issue will be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

**Illegal Byte Group Placements (Stratix & Stratix GX devices only)**

The IP Toolbench constraint editor allows you to place byte groups on both top and bottom of a Stratix or Stratix GX device at the same time, which causes an error in the Quartus II software. While you can split a DDR or DDR2 SDRAM interface across both the top and bottom of a Stratix device, some manual editing of the data path is required.

**Affected Configurations**

This issue affects designs on Stratix and Stratix GX devices that split the interface across the top and bottom.

**Design Impact**

The design does not compile.

**Workaround**

For more information, contact Altera.

**Solution Status**

This issue will never be fixed.

**DQS I/O Pin Error (Cyclone Devices Only)**

Under some circumstances, the timing analysis may show that the design requires a dedicated resynchronization clock. The IP Toolbench-generated example top-level design does not automatically support a separate resynchronization clock on Cyclone™ devices, which causes the following error message:

```
Error: DQS I/O pin <path name>cyclone_ddio_bidir:ddio_bidir[0]|ioatom must have a combinational output to the device
Error: Can't fit design in device
```
Affected Configurations

This issue affects Cyclone designs for which IP Toolbench recommends a separate resynchronization clock.

Design Impact

The design does not compile.

Workaround

Edit the example top-level design to instantiate a second PLL to provide a resynchronization clock with the IP Toolbench-recommended phase offset and connect this clock to the resynch_clk input of the controller.

Solution Status

This issue will never be fixed.

Design Assistant Warning Messages

The Quartus II Design Assistant generates warning messages when the design does not follow a Design Assistant rule, and generates information messages to provide information regarding a rule. If you enable the Design Assistant for a design containing a DDR or DDR2 SDRAM Controller, during compilation you will see the following messages for each of the following device families, which you can safely disregard.

Cyclone Devices

Medium

Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0

Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk1

Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n
Cyclone II Devices

Medium
Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0

Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n

Stratix Devices

Medium
Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers reset_n

Reset signal that is generated in one clock domain and used in other, asynchronous clock domains should be synchronized
Node: dq_enable_reset[0]

Stratix II Devices

High
Input clock pin should fan out to only one set of clock gating logic
Node: altpll:altpll_component|_clk0

Medium
Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0

Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n
HardCopy II Devices

High
Input clock pin should fan out to only one set of clock gating logic
Node: altpll:altpll_component|_clk0

Medium
Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0

Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n

PLL drives multiple clock network types
Node: altpll:altpll_component|pll

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact.

Workaround
No workaround is necessary.

Solution Status
This issue may be fixed in the next version of the Quartus II software and the DDR and DDR2 SDRAM Controller Compiler.
IP Toolbench Generated Files List Is Incomplete

When you click Generate in IP Toolbench, it displays a list of the generated files in your project directory. This list is incomplete. The user guide shows the full list of generated files. Table 2 shows the files that are missing from the IP Toolbench generated files list.

### Table 2. IP Toolbench Missing Generated Files

<table>
<thead>
<tr>
<th>Filename</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;variation name&gt;_bb.v</code></td>
<td>Verilog HDL black-box file for the MegaCore function variation. Use this file when using a third-party EDA tool to synthesize your design.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_auk_ddr_datapath_pack.vhd</code> or <code>.v</code></td>
<td>A VHDL package, which contains a component that the IP functional simulation model uses.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_ddr_sdram_vsim.tcl</code></td>
<td>The ModelSim simulation script.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_example_driver.vhd</code> or <code>.v</code></td>
<td>The example driver.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_example_settings.txt</code></td>
<td>The settings file for your variation, which the add constraints and the verify timing scripts use.</td>
</tr>
<tr>
<td><code>auto_add_ddr_constraints.tcl</code></td>
<td>The add constraints script, which calls the variation-specific add constraints scripts.</td>
</tr>
<tr>
<td><code>auto_verify_ddr_timing_constraints.tcl</code></td>
<td>The auto verify timing script, which calls the variation-specific verify timing scripts.</td>
</tr>
<tr>
<td><code>drr_lib_path.tcl</code></td>
<td>The Tcl library path file.</td>
</tr>
<tr>
<td><code>drr_pll_fb_stratixii.vhd</code> or <code>.v</code></td>
<td>Design file for the Stratix II feedback PLL.</td>
</tr>
<tr>
<td><code>drr_pll_&lt;device name&gt;.vhd</code> or <code>.v</code></td>
<td>Design file for the system PLL.</td>
</tr>
<tr>
<td><code>generic_ddr_dimm_model.vhd</code></td>
<td>VHDL simulation file.</td>
</tr>
<tr>
<td><code>generic_ddr_sdram.vhd</code></td>
<td>VHDL simulation file.</td>
</tr>
<tr>
<td><code>generic_ddr2_sdram.vhd</code></td>
<td>VHDL simulation file.</td>
</tr>
<tr>
<td><code>remove_constraints_for_&lt;variation name&gt;.tcl</code></td>
<td>The remove constraints script for the variation.</td>
</tr>
</tbody>
</table>

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

There is no design impact.

**Workaround**

There is no workaround.
Solution Status
This issue may be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

Contact Information
For more information, contact Altera’s mySupport website at www.altera.com/mysupport and click Create New Service Request. Choose the Product Related Request form.

Revision History
Table 3 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler v3.4.1.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Errata Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>June 2006</td>
<td>First release.</td>
</tr>
</tbody>
</table>