This document addresses known errata and documentation changes for the DDR and DDR2 SDRAM Controller Compiler version 3.3.0.

Errata are design functional defects or errors. Errata may cause the DDR and DDR2 SDRAM Controller Compiler to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions, or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated into an upcoming release of the DDR and DDR2 SDRAM Controller Compiler.

Altera has identified the following issues that affect the DDR and DDR2 SDRAM Controller Compiler:

1. “DDR SDRAM Controller Write Data Slip Errors” on page 2
2. “Quartus II Timing Analyzer Reports Incorrect Capture Cycles For Postamble Control and Resynchronization” on page 3
3. “Using Regional Clocks” on page 3
4. “Some Timing Assignments Are Not Converted To HardCopy II Devices” on page 4
5. “DDR2 SDRAM On-Die Termination (ODT) Control Pins Do Not Toggle” on page 5
6. “IP Toolbench Does Not Remember the Resynchronization Clock Setting” on page 5
7. “SOPC Builder-Generated DDR or DDR2 SDRAM Model Only Supports Widths Up To 32 Bits” on page 6
8. “Constraints Error (Linux & Solaris Only)” on page 7
9. “Creating a Variation in the Quartus II Software v5.0” on page 8
10. “DDR SDRAM in the Nios II Processor version 5.1” on page 8


15. “Illegal Byte Group Placements (Stratix & Stratix GX devices only)” on page 11.


18. “Multiple VHDL Support Files” on page 15

19. “IP Toolbench Generated Files List Is Incomplete” on page 16

For the most up-to-date errata for this release, continue to refer to the errata page on the Altera® website:


**DDR SDRAM Controller Write Data Slip Errors**

Under some circumstances, the DDR SDRAM Controller may issue a write command to the memory before the write data is available to be written. This issue causes a write data slip—the same data is written to two consecutive locations and all subsequent writes receive the data intended for the previous location.

**Affected Configurations**

This issue affects only DDR SDRAM Controllers configured to use the native interface and a memory burst length of 4 or 8. DDR2 SDRAM designs and designs that use the Avalon® interface or a memory burst length of 2 are unaffected.

**Design Impact**

This issue leads to the controller writing incorrect data to the memory.
Workaround

To prevent this error from occurring, turn on **Insert extra pipeline registers in the datapath** on the IP Toolbench Controller tab.

Solution Status

This issue will be fixed in a future release of the DDR and DDR2 SDRAM controller.

Quartus II Timing Analyzer Reports Incorrect Capture Cycles For Postamble Control and Resynchronization

If you load settings into the DDR Timing Wizard from the DDR or DDR2 SDRAM `<variation name>_ddr_settings.txt` file, you occasionally get incorrect values for the **Resynchronize read data in cycle** and **Postamble reset control clock in cycle** parameters.

Affected Configurations

This issue only affects you if you use the DDR Timing Wizard to add timing constraints to DDR or DDR2 SDRAM MegaCore® functions, and import the settings from the MegaCore settings file to the DDR Timing Wizard.

Design Impact

The timing margins reported by the Quartus® II Timing Analyzer will be wrong by a complete cycle.

Workaround

Edit the **Resynchronize read data in cycle** and **Postamble reset control clock in cycle** parameters and add or remove a cycle to ensure correct timing analysis.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

Using Regional Clocks

Versions of the DDR or DDR2 SDRAM MegaCore function before v3.3.0 incorrectly allow the use of regional clocks for the datapath logic.
The static timing analysis performed after the design compiles requires that the all the clocks in the datapath are global, but this requirement is not checked version 3.2.0 or earlier.

**Affected Configurations**

This issue affect designs that force the clocks going to the datapath logic onto regional clocks.

**Design Impact**

Timing margins may be incorrect.

**Workaround**

Do not use regional clocks for the datapath logic.

**Solution Status**

Timing analysis will report an error for these designs in the Quartus II software v5.1 and later.

**Some Timing Assignments Are Not Converted To HardCopy II Devices**

The Quartus II HardCopy® II migration tool gives warnings about assignments that are not convertible to HardCopy II devices.

When compiling a design that uses the DDR or DDR2 SDRAM MegaCore function, which targets a HardCopy II device, the Quartus II HardCopy II Netlist Writer gives warning messages because it ignores the MAX_DATA_ARRIVAL_SKEW assignments.

**Affected Configurations**

This issue affects designs that use the DDR or DDR2 SDRAM MegaCore function, which target HardCopy II devices.

**Workaround**

Ignore these messages because timing analysis for the interface is provided by the DDR Timing Wizard.

Contact Altera Support for more information on DDR and DDR2 SDRAM timing analysis for HardCopy II designs.
Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

DDR2 SDRAM On-Die Termination (ODT) Control Pins Do Not Toggle

The DDR2 SDRAM ODT control pins do not toggle. Choosing 50, 75, or 150 Ohms for the ODT setting makes no difference.

Affected Configurations

This issue affects DDR2 SDRAM designs that have control of the memory ODT enabled.

Design Impact

Some designs may exhibit incorrect behavior in hardware.

Workaround

To enable correct behavior of the ODT pins, edit the <variation name>_auk_ddr_sdram.v or .vhd file and set the gMEM_ODT_RANKS parameter or generic value on the instantiation of the controller (auk_ddr_controller) to 1 or 2. Set the value for gMEM_ODT_RANKS to the number of DIMM slots in your memory system, which is derived from the Number of chip selects divided by the Number of chip selects per DIMM, as specified in IP Toolbench.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

IP Toolbench Does Not Remember the Resynchronization Clock Setting

If you turn on Manual resynchronization control and choose a Resynchronization clock setting, when you exit and restart IP Toolbench, IP Toolbench does not remember the Resynchronization clock setting—it defaults to clk. This issue does not affect the postamble clock and capture clock settings. When this issue occurs, the post-compile timing script shows different margins on the resynchronization window.
Affected Configurations

This issue affects designs in which you turn on Manual resynchronization control, for example, to specify a dedicated clock phase rather than using the automatically chosen resynchronization clock phase. This issue does not affect designs that use the automatic setting (Manual resynchronization control is turned off).

Design Impact

This issue can result in read data failures in simulation or hardware as the design uses the wrong clock phase to resynchronize the captured read data.

Workaround

Ensure that you choose the Resynchronization clock setting every time you regenerate your variation.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

SOPC Builder-Generated DDR or DDR2 SDRAM Model Only Supports Widths Up To 32 Bits

The memory model generated when creating a DDR or DDR2 SDRAM Controller in SOPC Builder only supports widths up to 32 bits on the Avalon interface (16 bits on the memory interface). Creating an Avalon interface wider than 32 bits results in an incomplete memory model; however, the memory controller is correctly generated.

Affected Configurations

This issue affects interfaces with widths of greater than 32 bits generated in SOPC Builder.

Design Impact

This issue prevents you from correctly simulating the DDR or DDR2 SDRAM controller in the automatically-generated SOPC Builder testbench.
**Workaround**

Edit the memory model (<variation name>_test_component.v or .vhd) file and correct the clocked process that handles the incomplete writes at the bottom of the file. You should duplicate the existing assignments for all data bits greater than 32 with the appropriate data mask bits.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

**Constraints Error (Linux & Solaris Only)**

On RedHat Linux or Solaris computers, if you install the MegaCore function into a location with upper-case characters in its path, and you create a DDR or DDR2 SDRAM Stratix® II design with a HardCopy II companion device, you will see the following error message in the Constraints window and no byte groups will be available for you to select:

Floorplan unavailable for <Stratix II device>: <filename>

**Affected Configurations**

This issue affects designs created on UNIX machines that have upper-case characters in the MegaCore install path and that target Stratix II devices with a HardCopy II companion device.

**Design Impact**

This issue prevents you from assigning the byte groups of your memory interface to locations on the device and means that your design is not properly constrained.

**Workaround**

Reinstall the MegaCore function into a directory that has no upper-case characters in its path.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.
Creating a Variation in the Quartus II Software v5.0

IP Toolbench does not prevent you from creating a DDR or DDR2 SDRAM Controller version 3.3.0 in the Quartus II software v5.0, even though this operation is not supported. If you attempt this operation, you will see the following error message:

Error: Can't process assignment. Attribute name "SUPPRESS_DA_RULE_INTERNAL" is illegal -- use a legal attribute for assignment in ALTERA_ATTRIBUTE assignment.

Affected Configurations

This issue affects any variation of the v3.3.0 MegaCore function that you try to compile in the Quartus II software v5.0.

Design Impact

You are unable to compile projects containing the v3.3.0 MegaCore function in the Quartus II software v5.0.

Workaround

Upgrade to the Quartus II software v5.1, which is the supported version.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

DDR SDRAM in the Nios II Processor version 5.1

The first time that you regenerate and then recompile the Nios II 5.1 example designs that include a DDR SDRAM controller variation, you will see the following critical warning:

Critical Warning: Internal Error: pin_file <dirname>/sopc_cycloneii_nios_pins.tcl not found

This warning has no effect on the design. Recompile the design a second time to remove the warning message.

Affected Configurations

This issue affects the Nios II 5.1 example designs that include a DDR SDRAM controller variation.
Design Impact
There is no impact from this warning message.

Workaround
Recompile the example design again and the warning does not reappear.

Solution Status
This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

Error Message When Recompiling a Project
If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

Error: DDR timing cannot be verified until project has been successfully compiled.

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.

Affected Configurations
This issue affects all configurations.

Design Impact
The timing script does not verify your design.

Workaround
Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

Solution Status
This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.
**Remove Redundant Logic Cells Option (Stratix Devices Only)**

Do not turn on **Remove Redundant Logic Cells** in the Quartus II software if you are targeting Stratix devices.

**Affected Configurations**

This issue affects all designs targeted at Stratix devices, if you turn on **Remove Redundant Logic Cells** in the Quartus II software.

**Design Impact**

For Stratix devices, removing redundant logic cells makes the Quartus II software optimize away the important DQS delay matching buffers that the postamble circuitry uses.

**Workaround**

Ensure you turn off **Remove Redundant Logic Cells** in the Quartus II software if you are targeting Stratix devices.

**Solution Status**

There are no plans to fix this issue.

**SOPC Builder Supported Memory Data Bus Widths**

SOPC Builder currently only supports data bus widths that are a power of 2. IP Toolbench does not impose these limitations in the SOPC Builder flow, and can therefore generate bus widths incompatible with SOPC builder, which results in the following error message during SOPC Builder system generation.

```
ERROR: slave data width (48) for slave ddr_sdram/s1 unexpected
```

**Affected Configurations**

This issue affects all configurations that specify data bus widths that are not a power of two when you use the SOPC Builder flow.

**Design Impact**

You cannot generate the design in SOPC Builder.
Workaround

Ensure you restrict the data bus width parameter in the DDR SDRAM Controller IP Toolbench to a power of 2, for example, 8, 16, 32 or 64.

Solution Status

This issue will be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

Precompile Timing Estimates With Four or More DQS Delay Matching Buffers (Stratix Devices Only)

For Stratix devices, if you turn on Manual postamble control and choose 4 or more for the Number of DQS delay matching buffers, the pre-compile timing estimates in the system timing report for the read postamble enable property are incorrect. The correct timing analysis result is shown in the post-compile timing analysis report after compiling the design in the Quartus II software.

Affected Configurations

This issue affects designs on Stratix devices that require four or more DQS delay matching buffers.

Design Impact

This issue does not affect your design.

Workaround

Ignore the pre-compile timing estimates in the system timing report for the read postamble enable property.

Solution Status

This issue will be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

Illegal Byte Group Placements (Stratix & Stratix GX devices only)

The IP Toolbench constraint editor allows you to place byte groups on both top and bottom of a Stratix or Stratix GX device at the same time, which causes an error in the Quartus II software. While you can split a DDR or DDR2 SDRAM interface across both the top and bottom of a Stratix device, some manual editing of the data path is required.
Affected Configurations

This issue affects designs on Stratix and Stratix GX devices that split the interface across the top and bottom.

Design Impact

The design does not compile.

Workaround

For more information, contact Altera.

Solution Status

This issue will never be fixed.

DQS I/O Pin Error (Cyclone Devices Only)

Under some circumstances, the timing analysis may show that the design requires a dedicated resynchronization clock. The IP Toolbench-generated example top-level design does not automatically support a separate resynchronization clock on Cyclone™ devices, which causes the following error message:

```
Error: DQS I/O pin <path name>cyclone_ddio_bidir:ddio_bidir[0]|ioatom must have a combinational output to the device
Error: Can't fit design in device
```

Affected Configurations

This issue affects Cyclone designs for which IP Toolbench recommends a separate resynchronization clock.

Design Impact

The design does not compile.

Workaround

Edit the example top-level design to instantiate a second PLL to provide a resynchronization clock with the IP Toolbench-recommended phase offset and connect this clock to the resynch_clk input of the controller.

Solution Status

This issue will never be fixed.
Design Assistant Warning Messages

The Quartus II Design Assistant generates warning messages when the design does not follow a Design Assistant rule, and generates information messages to provide information regarding a rule. If you enable the Design Assistant for a design containing a DDR or DDR2 SDRAM Controller, during compilation you will see the following messages for each of the following device families, which you can safely disregard.

**Cyclone Devices**

**Medium**

Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0

Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk1

Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n

**Cyclone II Devices**

**Medium**

Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0

Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n

**Stratix Devices**

**Medium**

Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers reset_n
Reset signal that is generated in one clock domain and used in other, asynchronous clock domains should be synchronized
Node: dq_enable_reset[0]

**Stratix II Devices**

**High**
Input clock pin should fan out to only one set of clock gating logic
Node: altpll:altpll_component|_clk0

**Medium**
Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0
Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n

**HardCopy II Devices**

**High**
Input clock pin should fan out to only one set of clock gating logic
Node: altpll:altpll_component|_clk0

**Medium**
Clock signal source should drive only input clock ports
Node: altpll:altpll_component|_clk0
Clock signal source should not drive registers that are triggered by different clock edges
Node: altpll:altpll_component|_clk0

External reset should be synchronized using two cascaded registers
Node: reset_n
PLL drives multiple clock network types
Node: altpll:altpll_component|pll

**Affected Configurations**

This issue affects all configurations.
Design Impact
There is no design impact.

Workaround
No workaround is necessary.

Solution Status
This issue may be fixed in the next version of the Quartus II software and the DDR and DDR2 SDRAM Controller Compiler.

Multiple VHDL Support Files
The following Altera MegaCore functions generate the Altera VHDL support package (altera vhdl support.vhd):

- DDR or DDR2 SDRAM Controller MegaCore function
- QDRII SRAM Controller MegaCore function
- RLDRAM II Controller MegaCore function
- PCI Express MegaCore function

When you have a Quartus II project that contains multiple MegaCore functions that are in separate directories, there are multiple instances of the altera vhdl support.vhd file. If the Quartus II compilation adds two or more separate copies of altera vhdl support.vhd, the compilation fails.

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact.

Workaround
Either generate all the project MegaCore functions in the Quartus II project directory, or ensure only one instance of the altera vhdl support.vhd file exists in your project.

Ignore the warning that IP Toolbench running outside of SOPC Builder generates, when it overwrites an existing altera vhdl support.vhd file.
To ensure your project only includes one instance of the `altera_vhdl_support.vhd` file, follow these steps:

1. Choose Add/Remove Files in Project (Project menu).

2. Choose all instances of `altera_vhdl_support.vhd` except the first instance.

3. Click Remove.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

**IP Toolbench Generated Files List Is Incomplete**

When you click Generate in IP Toolbench, it displays a list of the generated files in your project directory. This list is incomplete. The user guide shows the full list of generated files. Table 1 shows the files that are missing from the IP Toolbench generated files list.

<table>
<thead>
<tr>
<th>Filename</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;variation name&gt;_bb.v</code></td>
<td>Verilog HDL black-box file for the MegaCore function variation. Use this file when using a third-party EDA tool to synthesize your design.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_auk_ddr_datapath_pack.auk_ddr_datapath_pack.vhd or .v</code></td>
<td>A VHDL package, which contains a component that the IP functional simulation model uses.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_ddr_sdram_vsimsim.tcl</code></td>
<td>The ModelSim simulation script.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_example_driver.vhd or .v</code></td>
<td>The example driver.</td>
</tr>
<tr>
<td><code>&lt;variation name&gt;_example_settings.txt</code></td>
<td>The settings file for your variation, which the add constraints and the verify timing scripts use.</td>
</tr>
<tr>
<td><code>auto_add_ddr_constraints.tcl</code></td>
<td>The add constraints script, which calls the variation-specific add constraints scripts.</td>
</tr>
<tr>
<td><code>auto_verify_ddr_timing_constraints.tcl</code></td>
<td>The auto verify timing script, which calls the variation-specific verify timing scripts.</td>
</tr>
<tr>
<td><code>ddr_lib_path.tcl</code></td>
<td>The Tcl library path file.</td>
</tr>
<tr>
<td><code>ddr_pll_fb_stratixii.vhd or .v</code></td>
<td>Design file for the Stratix II feedback PLL.</td>
</tr>
<tr>
<td><code>ddr_pll_&lt;device name&gt;.vhd or .v</code></td>
<td>Design file for the system PLL.</td>
</tr>
<tr>
<td><code>generic_ddr_dimm_model.vhd</code></td>
<td>VHDL simulation file.</td>
</tr>
<tr>
<td><code>generic_ddr_sdram.vhd</code></td>
<td>VHDL simulation file.</td>
</tr>
</tbody>
</table>


**Affected Configurations**

This issue affects all configurations.

**Design Impact**

There is no design impact.

**Workaround**

There is no workaround.

**Solution Status**

This issue may be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

### Table 1. IP Toolbench Missing Generated Files (Part 2 of 2)

<table>
<thead>
<tr>
<th>Filename</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>generic_ddr2_sdram.vhd</td>
<td>VHDL simulation file.</td>
</tr>
<tr>
<td>remove_constraints_for_&lt;variation name&gt;.tcl</td>
<td>The remove constraints script for the variation.</td>
</tr>
</tbody>
</table>

**Contact Information**

For more information, contact Altera’s mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.
Revision History

Table 2 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler v3.3.0.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Errata Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>November 2005</td>
<td>Added the following issues:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>● “Quartus II Timing Analyzer Reports Incorrect Capture Cycles For Postamble Control and Resynchronization”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>● “Using Regional Clocks”</td>
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<td></td>
<td>● “DDR SDRAM in the Nios II Processor version 5.1”</td>
</tr>
<tr>
<td>1.0</td>
<td>October 2005</td>
<td>First release.</td>
</tr>
</tbody>
</table>