Notes:

1. FPGA Schematic Symbol Breakdown:
   (a) Bank 1 - I/O
   (b) Bank 2 - I/O
   (c) Bank 3 - I/O
   (d) Bank 4 - I/O
   (e) Bank 5 - I/O
   (f) Bank 6 - I/O
   (g) Bank 7 - I/O
   (h) Bank 8 - I/O
   (i) Configuration
   (j) Clocks
   (k) VCCint, GND
   (l) VCCio, GND

2. PCB Supports 2C70 - 2C50 - 2C70 Migration

   No additional I/O of 2C70 or 2C50 used, as
   the 2C70 has the most I/O of the group
   due to additional VCCINT, GND, and VREF
   pins on the larger 2C50 and 2C70 devices.

3. Some I/O pins are connected to 1.2V or GND.
   These are the additional VCC and GND pins of
   the larger 2C50 and 2C70 devices.

   **WARNING**

   **DO NOT DRIVE UNUSED I/O TO GND IN QUARTUS**

   Leaving 1.2V connected I/O pins as outputs
   driving GND can cause high I current and increased
   temperature which can lead to device damage
   left over a long period of time.

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Bank 2

**VCCIO = 3.3V**

Proto Bus
Video DAC
DAC Channel 1

Bank 1

**VCCIO = 3.3V**

DAC Channel 1
DAC Channel 2
Video DAC

Bank 3

**VCCIO = 1.8V**

DDR2 DIMM DATA LANES
ADC Channel 2
DAC Channel 1

Bank 4

**VCCIO = 1.8V**

DDR2 DIMM DATA LANES
ADC Channel 2
DAC Channel 1

Bank 5

**VCCIO = 3.3V**

Shared Bus
DAC Channel 2

Bank 6

**VCCIO = 3.3V**

Shared Bus
DAC Channel 1
DAC Channel 2
Video DAC

Bank 8

**VCCIO = 1.8V**

DDR2 DIMM DATA LANES, ADDRESS Pushbuttons

Bank 7

**VCCIO = 1.8V**

DDR2 DIMM DATA LANES, CTRL, CLOCK Pushbuttons

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These pins are connected to VCCINT on 2C70.

VGA_CLK 15

These pins are connected to VCCINT on 2C70.

VCCIO = 3.3V

1.2V

These pins are GND pins on 2C70.
Place near DIMM back-side on component side of PCB
**DDR2 SDRAM DIMM Terminations**

**Cyclone II-Side Termination Resistors**

**DIMM-Side Termination Resistors**

The following resistors can be installed for Class II Termination:

- RN24, RN25, RN26, RN27, RN28, RN29, RN30, RN31, RN32, RN33, RN34, R15, R16

**DIMM Memory Decoupling**

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