Enpirion® Power Datasheet
EN6310QA 1A PowerSoC
Voltage Mode Synchronous
PWM Buck with Integrated Inductor

Description
The EN6310QA is a member of Altera Enpirion’s high efficiency EN6300 family of PowerSoCs. The EN6310QA is a 1A PowerSoC that is AEC-Q100 qualified for automotive applications. The EN6310QA employs Altera Enpirion’s EDMOS MOSFET technology for monolithic integration and very low switching loss. The device switches at 2.2MHz in fixed PWM operation to eliminate the low frequency noise that is created by pulse frequency modulation operating modes. The MOSFET ratios are optimized to offer high conversion efficiency for lower VOUT settings.

Output voltage settings are programmable via a simple resistor divider circuit. Output voltage can be programmed from as low as 0.6V to 3.3V. The device has a programmable soft-start ramp rate to accommodate sequencing and to prevent un-wanted current inrush at start up. A Power OK (POK) flag is provided to indicate a fault condition.

The Altera Enpirion power solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Altera Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Features
- Integrated inductor, MOSFET and Controller
- -40°C to 105°C Ambient Temperature Range
- AEC-Q100 Qualified for Automotive Applications
- Small 4mm x 5mm x 1.85mm QFN
- High Efficiency up to 96%
- Solution Footprint Less than 65mm²
- 1A Continuous Output Current
- VIN Range of 2.7V to 5.5V
- VOUT Range from 0.6V to 3.3V
- Programmable Soft Start and Power OK Flag
- Fast Transient Response and Recovery Time
- Low Noise and Low Output Ripple; 4mV Typical
- 2.2MHz Switching Frequency
- Under Voltage Lock-out (UVLO), Short Circuit, Over Current and Thermal Protection

Applications
- Automotive Applications
- Altera FPGAs (MAX, ARRIA, CYCLONE, STRATIX)
- Low Power FPGA Applications
- Noise Sensitive Wireless and RF Applications

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**Figure 1. Simplified Applications Circuit**

**Figure 2. Highest Efficiency in Smallest Solution Size**

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**Ordering Information**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Markings</th>
<th>T_A (°C)</th>
<th>Package Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN6310QA</td>
<td>6310A</td>
<td>-40 to +105</td>
<td>30-pin (4mm x 5mm x 1.85mm) QFN T&amp;R</td>
</tr>
<tr>
<td>EVB-EN6310QA</td>
<td>6310A</td>
<td></td>
<td>QFN Evaluation Board</td>
</tr>
</tbody>
</table>


**Pin Assignments (Top View)**

**Figure 3:** Pin Out Diagram (Top View)

**NOTE A:** NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

**NOTE B:** White 'dot' on top left is pin 1 indicator on top of the device package.

**NOTE C:** The Keep Out pin is the exposed metal below the package that is not to be mechanically or electrically connected to the PCB.
## Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2, 24-30</td>
<td>NC(SW)</td>
<td>NO CONNECT. Do not connect to any signal, voltage, or ground. These pins are connected internally to the MOSFET common switch node.</td>
</tr>
<tr>
<td>3, 4</td>
<td>PGND</td>
<td>Power ground. The output filter capacitor ground terminal should be connected to these pins. Refer to application details for proper layout and ground routing.</td>
</tr>
<tr>
<td>5-11</td>
<td>VOUT</td>
<td>Regulated output. Connect output capacitors from these pins to PGND (pins 3, 4).</td>
</tr>
<tr>
<td>12, 15</td>
<td>NC</td>
<td>NO CONNECT. Do not connect to any signal, voltage, or ground. These pins may be connected internally.</td>
</tr>
<tr>
<td>13</td>
<td>VFB</td>
<td>Output feed-back node. Connect to center of VOUT resistor divider.</td>
</tr>
<tr>
<td>14</td>
<td>AGND</td>
<td>Quiet analog ground for control circuits. Connect to system ground plane.</td>
</tr>
<tr>
<td>16</td>
<td>CSS</td>
<td>Soft Start startup time programming pin. Connect CSS capacitor from this pin to AGND.</td>
</tr>
<tr>
<td>17</td>
<td>POK</td>
<td>Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is above 90% of VOUT nominal. Leave this pin floating if not used.</td>
</tr>
<tr>
<td>18</td>
<td>ENABLE</td>
<td>Output enable; Enable = logic high, Disable = logic low.</td>
</tr>
<tr>
<td>19</td>
<td>AVIN</td>
<td>Quiet input supply for circuitry.</td>
</tr>
<tr>
<td>20, 21</td>
<td>PGND</td>
<td>Power ground. The input filter capacitor ground terminal should be connected to these pins. Refer to application details for proper layout and ground routing.</td>
</tr>
<tr>
<td>22, 23</td>
<td>PVIN</td>
<td>Input supply voltage for high side MOSFET Switch. Connect input filter capacitor from this pin to PGND.</td>
</tr>
<tr>
<td>31</td>
<td>PGND Bottom Pad</td>
<td>Device thermal pad to be connected to the system GND plane. See Layout Recommendations section.</td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings

**CAUTION**: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltages on: PVIN, AVIN, VOUT</td>
<td></td>
<td>-0.3</td>
<td>6.6</td>
<td>V</td>
</tr>
<tr>
<td>Voltages on: ENABLE, POK</td>
<td></td>
<td>-0.3</td>
<td>VIN+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Voltages on: VFB, SS</td>
<td></td>
<td>-0.3</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T&lt;sub&gt;STG&lt;/sub&gt;</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum Operating Junction Temperature</td>
<td>T&lt;sub&gt;J-ABS Max&lt;/sub&gt;</td>
<td>150</td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A</td>
<td></td>
<td></td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>ESD Rating (based on Human Body Model)</td>
<td></td>
<td></td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>ESD Rating (based on CDM)</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>VIN</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>0.60</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td></td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>Operating Ambient Temperature</td>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>-40</td>
<td>+105</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>T&lt;sub&gt;J&lt;/sub&gt;</td>
<td>-40</td>
<td>+125</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Thermal Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TYP</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shutdown</td>
<td>T&lt;sub&gt;SD&lt;/sub&gt;</td>
<td>140</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td>T&lt;sub&gt;SDH&lt;/sub&gt;</td>
<td>20</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Resistance: Junction to Ambient (0 LFM) (Note 1)</td>
<td>θ&lt;sub&gt;JA&lt;/sub&gt;</td>
<td>60</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance: Junction to Case (0 LFM)</td>
<td>θ&lt;sub&gt;JC&lt;/sub&gt;</td>
<td>3</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**Note 1**: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.
## Electrical Characteristics

NOTE: $V_{IN}$ (PVIN and AVIN) = 5.0V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>VIN</td>
<td>$V_{IN} = AVIN = PVIN$</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Under Voltage Lockout VIN Rising</td>
<td>UVLO_R</td>
<td></td>
<td>2.3</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Under Voltage Lockout VIN Falling</td>
<td>UVLO_F</td>
<td></td>
<td>1.9</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>$V_{OUT}$</td>
<td></td>
<td>0.6</td>
<td>3.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>$D_{MAX}$</td>
<td></td>
<td>85</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Feedback Pin Voltage Initial Accuracy</td>
<td>VFB</td>
<td>$T_A = 25^\circ C$, $V_{IN} = 5.0V$, $I_{LOAD} = 100mA$</td>
<td>0.60</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage DC Accuracy</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VIN = 3.3V; $0A \leq I_{OUT} \leq 1.0A$; $-40^\circ C \leq T_A \leq +105^\circ C$</td>
<td>-2.0</td>
<td>+2.25</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VIN = 5.0V; $0A \leq I_{OUT} \leq 1.0A$; $-20^\circ C \leq T_A \leq +105^\circ C$</td>
<td>-2.0</td>
<td>+2.0</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VIN = 5.0V; $0A \leq I_{OUT} \leq 1.0A$; $-40^\circ C \leq T_A \leq +105^\circ C$</td>
<td>-3.0</td>
<td>+2.0</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Feedback Pin Input Current (Note 3)</td>
<td>$I_{VFB}$</td>
<td></td>
<td>100</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Continuous Output Current</td>
<td>$I_{OUT}$</td>
<td></td>
<td>1</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Over Current Trip Point</td>
<td>$I_{OCP}$</td>
<td></td>
<td>1.2</td>
<td>1.8</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>AVIN Shut-Down Current</td>
<td>$I_{SD}$</td>
<td>ENABLE = Low</td>
<td>175</td>
<td></td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>PVIN Shut-Down Current</td>
<td>$I_{SD}$</td>
<td>ENABLE = Low</td>
<td>2.2</td>
<td></td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>OCP Threshold</td>
<td>$I_{OCP}$</td>
<td>$2.7 \leq V_{IN} \leq 5.5V$</td>
<td>1.2</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>ENABLE Pin Logic Threshold</td>
<td>$EN_{LOW}$</td>
<td>Pin = Low</td>
<td>0.0</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EN_{HIGH}$</td>
<td>Pin = High</td>
<td>1.8</td>
<td></td>
<td>VIN</td>
<td>V</td>
</tr>
<tr>
<td>ENABLE Pin Input Current</td>
<td>$I_{ENABLE}$</td>
<td>ENABLE = High</td>
<td>5</td>
<td></td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>ENABLE Lock-out</td>
<td>ENLO</td>
<td>Time before enable will re-assert internally after being pulled low</td>
<td>12.5</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$f_{SW}$</td>
<td></td>
<td>2.2</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Soft Start Time (Note 2) (Note 3)</td>
<td>$T_{SS}$</td>
<td>CSS = 10nF</td>
<td>5.2</td>
<td>6.5</td>
<td>7.8</td>
<td>ms</td>
</tr>
<tr>
<td>Allowable Soft Start Capacitor Range (Note 3)</td>
<td>$C_{SS}$</td>
<td></td>
<td>0.47</td>
<td>10</td>
<td>nF</td>
<td></td>
</tr>
</tbody>
</table>

**Note 2**: Soft Start Time range does not include capacitor tolerances.

**Note 3**: Parameter not production tested but is guaranteed by design.
Typical Performance Curves

**Efficiency vs. Output Current**

- **VOUT = 2.5V**
- **VOUT = 1.8V**
- **VOUT = 1.5V**
- **VOUT = 1.2V**
- **VOUT = 1.0V**

**Conditions**

- **VIN = 3.3V**

**Output Voltage vs. Output Current**

- **VIN = 3.3V**
- **VIN = 5V**

**Conditions**

- **VOUT = 1.0V**
- **VOUT = 1.2V**

**Output Voltage vs. Output Current**

- **VIN = 3.3V**
- **VIN = 5.0V**

**Conditions**

- **VOUT = 1.5V**
- **VOUT = 1.8V**
Typical Performance Curves (Continued)

### Output Voltage vs. Output Current

**VIN = 3.3V**

**VIN = 5.0V**

**VOUT = 2.5V**

**VOUT = 3.3V**

### Output Voltage vs. Temperature

**VIN = 3.3V**

**VIN = 5.0V**

**VOUT_NOM = 1.0V**

**VOUT_NOM = 2.5V**

**VOUT_NOM = 3.3V**

**LOAD = 0A**

**LOAD = 0.2A**

**LOAD = 0.4A**

**LOAD = 0.8A**

**LOAD = 1A**

**LOAD = 0A**

**LOAD = 0.2A**

**LOAD = 0.4A**

**LOAD = 0.8A**

**LOAD = 1A**

**LOAD = 0A**

**LOAD = 0.2A**

**LOAD = 0.4A**

**LOAD = 0.8A**

**LOAD = 1A**
Typical Performance Curves (Continued)

Output Voltage vs. Input Voltage

No Thermal Derating

CONDITIONS
VOUT_NOM = 1.8V
TA = 25°C

VIN = 5.0V
VOUT = 1.0V

VIN = 5.0V
VOUT = 3.3V

No Thermal Derating

Conditions
Typical Performance Characteristics

Output Ripple at 20MHz Bandwidth

- CONDITIONS
  - VIN = 3.3V
  - VOUT = 1.2V
  - IOUT = 0A
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (106)

Output Ripple at 20MHz Bandwidth

- CONDITIONS
  - VIN = 3.3V
  - VOUT = 1.2V
  - IOUT = 1A
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)

Output Ripple at 500MHz Bandwidth

- CONDITIONS
  - VIN = 3.3V
  - VOUT = 1.2V
  - IOUT = 0A
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)

Output Ripple at 500MHz Bandwidth

- CONDITIONS
  - VIN = 3.3V
  - VOUT = 1.2V
  - IOUT = 1A
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)

Output Ripple at 500MHz Bandwidth

- CONDITIONS
  - VIN = 5V
  - VOUT = 1.2V
  - IOUT = 0A
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)

Output Ripple at 500MHz Bandwidth

- CONDITIONS
  - VIN = 5V
  - VOUT = 1.2V
  - IOUT = 1A
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)
Typical Performance Characteristics (Continued)

Output Ripple at 500MHz Bandwidth

- CONDITIONS
  - VIN = 5V
  - VOUT = 3.3V
  - IOUT = 0A
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)

Load Transient from 0A to 1A

- CONDITIONS
  - VIN = 3.3V, VOUT = 1V
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)
  - Using Datasheet Recommended Components

- CONDITIONS
  - VIN = 3.3V, VOUT = 1.8V
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)
  - Using Datasheet Recommended Components

Load Transient from 0A to 1A

- CONDITIONS
  - VIN = 3.3V, VOUT = 2.5V
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)
  - Using Datasheet Recommended Components

- CONDITIONS
  - VIN = 5.0V, VOUT = 1.0V
  - CIN = 4.7µF (0603) + 100pF
  - COUT = 2x22µF (1206)
  - Using Datasheet Recommended Components
Typical Performance Characteristics (Continued)

Load Transient from 0A to 1A

VOUT = 1.8V
(AC Coupled)
50mV / DIV

CONDITIONS
VIN = 5.0V, VOUT = 1.8V
CIN = 4.7µF (0603) + 100pF
COUT = 2x22µF (1206)
Using Datasheet Recommended Components

Load Transient from 0A to 1A

VOUT = 1.8V
(AC Coupled)
50mV / DIV

CONDITIONS
VIN = 5.0V, VOUT = 3.3V
CIN = 4.7µF (0603) + 100pF
COUT = 2x22µF (1206)
Using Datasheet Recommended Components

Enable Startup/Shutdown Waveform (0A)

ENABLE
VOUT
POK

CONDITIONS
VIN = 5V, VOUT = 1.8V, No Load, Css = 10nF
CIN = 4.7µF (0603) + 100pF, COUT = 2x22µF (1206)

Enable Startup/Shutdown Waveform (1A)

ENABLE
VOUT
POK

CONDITIONS
VIN = 5V, VOUT = 1.8V, 1A Load, Css = 10nF
CIN = 4.7µF (0603) + 100pF, COUT = 2x22µF (1206)

Enable Startup Waveform (0A)

ENABLE
VOUT
POK

CONDITIONS
VIN = 5V, VOUT = 1.8V, No Load, Css = 10nF
CIN = 4.7µF (0603) + 100pF, COUT = 2x22µF (1206)

Enable Shutdown Waveform (0A)

ENABLE
VOUT
POK

CONDITIONS
VIN = 5V, VOUT = 1.8V, No Load, Css = 10nF
CIN = 4.7µF (0603) + 100pF, COUT = 2x22µF (1206)
Figure 4: Functional Block Diagram
Functional Description

Functional Overview

The EN6310QA is a synchronous buck converter with integrated MOSFET switches and Inductor. The device can deliver up to 1A of continuous load current. The EN6310QA has a programmable soft start rise time and a power OK (POK) signal. The device operates in a fixed 2.2MHz PWM mode to eliminate noise associated with pulse frequency modulation schemes. The control topology is a low complexity type IV voltage mode providing high noise immunity and stability over the entire operating range. Output voltage is set with a simple resistor divider. The high switching frequency enables the use of small MLCC input and output filter capacitors. Figure 4 shows the EN6310QA block diagram.

Protection Features:

The EN6310QA has the following protection features.

- Over-current protection (to protect the IC from excessive load current)
- Short-Circuit protection
- Thermal shutdown with hysteresis
- Under-voltage lockout circuit to disable the converter output when the input voltage is below a pre-defined level

Additional Features:

- Soft-start circuit, limiting the in-rush current when the converter is initially powered up. The soft start time is programmable with appropriate choice of soft start capacitor value

High Efficiency Technology

The key enabler of this revolutionary integration is Altera Enpirion’s proprietary power MOSFET technology. The advanced MOSFET switches are implemented in deep-submicron CMOS to supply very low switching loss at high switching frequencies and to allow a high level of integration. The semiconductor process allows seamless integration of all switching, control, and compensation circuitry. The proprietary magnetics design provides high-density/high-value magnetics in a very small footprint. Altera Enpirion magnetics are carefully matched to the control and compensation circuitry yielding an optimal solution with assured performance over the entire operating range.

Integration for Low-Noise Low-EMI

The EN6310QA utilizes a proprietary low loss integrated inductor. The integration of the inductor greatly simplifies the power supply design process. The inherent shielding and compact construction of the integrated inductor reduces the conducted and radiated noise that can couple into the traces of the printed circuit board. Furthermore, the package layout is optimized to reduce the electrical path length for the high di/dt input AC ripple currents that are a major source of radiated emissions from DC-DC converters. Careful package and IC design minimize common mode noise that can be difficult to mitigate otherwise. The integrated inductor provides the optimal solution to the complexity, output ripple, and noise that plague low power DCDC converter design.

Control Topology

The EN6310QA utilizes an internal type IV voltage mode compensation scheme. Voltage mode control provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance. The EN6310QA is optimized for fast transient recovery for applications with demanding transient performance. Voltage mode control enables a high degree of stability over the entire operating range.

Enable

The EN6310QA ENABLE pin enables and disables operation of the device. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter and initiate a normal soft start operation. When ENABLE is pulled low, the Power MOSFETs stop switching and the output is discharged in a controlled manner with a soft pull down MOSFET. Once the enable pin is pulled low, there is a lockout period before the device can be re-enabled. The lock out period can be found in the Electrical Characteristics Table. Do not leave ENABLE pin floating or it will be in an unknown random state.

The EN6310QA supports startup into a pre-biased output of up to 1.5V. The output of the EN6310QA can be pre-biased with a voltage up to 1.5V when it is first enabled.
POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed voltage level. If the output voltage is below this point, the POK signal will be a logic low. If the input voltage is in UVLO or if the ENABLE is pulled low, the POK will also be a logic low. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

Programmable Soft Start Operation

Soft start is externally programmable by adjusting the value of the C_SS capacitor, which is placed between the respective C_SS pin and AGND pin. When the enable pin is pulled high, the output will ramp up monotonically at a rate determined by the CSS capacitor.

Soft start ramp time is programmable over a range of 0.5ms to 10ms. The longer ramp times allow startup into very large bulk capacitors that may be present in applications such as wireless broadband or solid state storage, without triggering an Over Current condition. The rise time is given as:

\[ T_{\text{rise}} [\text{ms}] = C_{\text{SS}} [\text{nF}] \times 0.65 \pm 25\% \]

**NOTE:** Rise time does not include capacitor tolerances.

If a 10nF soft-start capacitor is used, then the output voltage rise time will be around 6.5ms. The rise time is measured from when \( V_{\text{IN}} \geq V_{\text{UVLO}} \) and ENABLE pin voltage crosses its logic high threshold to when \( V_{\text{OUT}} \) reaches its programmed value.

Over Current/Short Circuit Protection

The current limit and short-circuit protection is achieved by sensing the current flowing through a sense PFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off and the output is discharged. After 1.6ms the device will be re-enabled and will then go through a normal soft-start cycle. If the over current condition persists, the device will enter a hiccup mode.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold, the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Thermal Shutdown

When excess power is dissipated in the EN6310QA the junction temperature will rise. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases to a safe operating level, the part will go through the normal startup process. The thermal shutdown temperature and hysteresis values can be found in the thermal characteristics table.
Output Voltage Programming

The EN6310QA output voltage is programmed using a simple resistor divider network \( R_A \) and \( R_B \). The feedback voltage at \( V_{FB} \) is nominally 0.6V. \( R_A \) is fixed at 200kΩ and \( R_B \) can be calculated based on Figure 5. The values recommended for \( C_{OUT} \), \( C_A \), and \( R_{CA} \) make up the external compensation of the EN6310QA. It will vary with each \( V_{IN} \) and \( V_{OUT} \) combination to optimize on performance. Please see Table 1 for a list of recommended \( R_A \), \( C_A \), \( R_{CA} \), and \( C_{OUT} \) values for each solution. Since \( V_{FB} \) is a sensitive node, do not touch the \( V_{FB} \) node while the device is in operation as doing so may introduce parasitic capacitance into the control loop that causes the device to behave abnormally and damage may occur.

The output voltage is set by the following formula:

\[
V_{OUT} = V_{REF} \times \left(1 + \frac{R_A}{R_B}\right)
\]

Rearranging to solve for \( R_B \):

\[
R_B = R_A \times \frac{V_{REF}}{V_{OUT} - V_{REF}} \text{kΩ}
\]

Where:

\( R_A = 200\text{kΩ} \)
\( V_{REF} = 0.60\text{V} \)

Then \( R_B \) is given as:

\[
R_B = \frac{\text{120}}{V_{OUT} - 0.6} \text{kΩ}
\]

\( R_A \) is chosen as 200kΩ to provide constant loop gain. The output voltage can be programmed over the range of 0.6V to 3.3V.

\[
\begin{align*}
\text{Table 1}. & \text{ Compensation values. For output voltages in between, use the values from the higher output voltage.}
\end{align*}
\]
Input Filter Capacitor
The EN6310QA requires at least a 4.7µF/0603 and a 100pF input capacitor near the PVIN pins. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Table 2 contains a list of recommended input capacitors.

<table>
<thead>
<tr>
<th>Description</th>
<th>MFG</th>
<th>P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7µF, 6.3V, X7R, 0603</td>
<td>Taiyo Yuden</td>
<td>JMK107BB7475KA-T</td>
</tr>
</tbody>
</table>

Table 2. Recommended Input Capacitors

Output Filter Capacitor
The EN6310QA requires at least two 22µF/1206 output filter capacitors. Low ESR ceramic capacitors are required with X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. Table 3 contains a list of recommended output capacitors.

<table>
<thead>
<tr>
<th>Description</th>
<th>MFG</th>
<th>P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>22µF, 10V, X7R, 1206</td>
<td>Murata</td>
<td>GRM31CR71A226ME15</td>
</tr>
<tr>
<td></td>
<td>Taiyo Yuden</td>
<td>LMK316AB7226KL-TR</td>
</tr>
<tr>
<td></td>
<td>AVX</td>
<td>1206ZC226KAT2A</td>
</tr>
</tbody>
</table>

Table 3. Recommended Output Capacitors
Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Altera Enpirion PowerSoC helps alleviate some of those concerns.

The Altera Enpirion EN6310QA DC-DC converter is packaged in a 4x5x1.85mm 30-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 140°C.

The following example and calculations illustrate the thermal performance of the EN6310QA.

Example:

\[ \eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = 91\% = 0.91 \]

\[ P_{\text{IN}} = \frac{P_{\text{OUT}}}{\eta} \]

\[ P_{\text{IN}} \approx \frac{3.3\text{W}}{0.91} \approx 3.63\text{W} \]

The power dissipation \( P_D \) is the power loss in the system and can be calculated by subtracting the output power from the input power.

\[ P_D = P_{\text{IN}} - P_{\text{OUT}} \]

\[ \approx 3.63\text{W} - 3.3\text{W} \approx 0.33\text{W} \]

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value \( \theta_{JA} \). The \( \theta_{JA} \) parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN6310QA has a \( \theta_{JA} \) value of 60 °C/W without airflow.

Determine the change in temperature \( \Delta T \) based on \( P_D \) and \( \theta_{JA} \).

\[ \Delta T = P_D \times \theta_{JA} \]

\[ \Delta T \approx 0.33\text{W} \times 60\text{°C/W} \approx 19.8\text{°C} \approx 20\text{°C} \]

The junction temperature \( T_J \) of the device is approximately the ambient temperature \( T_A \) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

\[ T_J = T_A + \Delta T \]

\[ T_J \approx 25\text{°C} + 20\text{°C} = 45\text{°C} \]

The maximum operating junction temperature \( T_{J\text{MAX}} \) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature \( T_{A\text{MAX}} \) allowed can be calculated.

\[ T_{A\text{MAX}} = T_{J\text{MAX}} - P_D \times \theta_{JA} \]

\[ \approx 125\text{°C} - 20\text{°C} \times 105\text{°C} \]

The maximum ambient temperature the device can reach is 105°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

![Efficiency vs. Output Current](image)

**Figure 6.** Efficiency vs. Output Current

For \( V_{\text{IN}} = 5\text{V} \), \( V_{\text{OUT}} = 3.3\text{V} \) at 1A, \( \eta \approx 91\% \)
Figure 7. Typical Engineering Schematic
**Recommendation 1:** Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN6310QA package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN6310QA should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

**Recommendation 2:** The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the

**Recommendation 3**: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible.

The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. See Figure 8.

**Recommendation 4**: Multiple small vias (the same size as the thermal vias discussed in recommendation 3) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 8. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C\textsubscript{IN} and C\textsubscript{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

**Recommendation 5**: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. A good location is to place the AVIN connection on the source side of the input capacitor, away from the PVIN pins.

**Recommendation 6**: The layer 1 metal under the device must not be more than shown in Figure 8. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

**Recommendation 7**: The V\textsubscript{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

**Recommendation 8**: Keep R\textsubscript{A}, C\textsubscript{A}, and R\textsubscript{B} close to the VFB pin (see Figures 7 and 8). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R\textsubscript{B} directly to the AGND pin instead of going through the GND plane.
Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall footprint. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 9.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PCB. The PCB top layer under the EN6310QA should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 9 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package.

Figure 9. Lead-Frame exposed metal (Bottom View)
Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.
Recommended PCB Footprint

**Figure 10.** EN6310QA PCB Footprint (Top View)

**Note:** Don’t use the layer underneath the device keep out area as it contains the exposed metal below the package that is not to be mechanically or electrically connected to the PCB.
Figure 11. EN6310QA Package Dimensions (Bottom View)

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

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