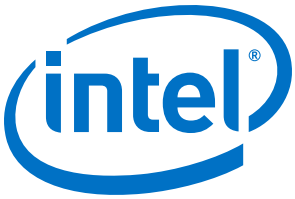

Nios® II Performance Benchmarks

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1. Nios® II Performance Benchmarks

1.1. Performance Benchmarks Overview

This datasheet lists the performance and logic element (LE) usage for a typical implementation of a Nios® II soft processor and peripherals. Nios II processors are configurable and designed for implementation in Intel® FPGAs. The following Nios II processors cores were used for these benchmarks:(1)

- Nios II/f—The Nios II/f "fast" processor is designed for high performance and has the most configuration options, some of which are unavailable in the Nios II/e processor.
- Nios II/e—The Nios II/e "economy" processor is designed for the smallest possible logic size while still providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.

Note: Results may vary slightly depending on the version of the Intel Quartus® Prime software, the version of the Nios II processor, compiler version, target device and the configuration of the processor. Also, any changes to the system logic design might change the performance and LE usage. All results are generated from designs built using the Platform Designer tool.

The Dhrystone MIPS (DMIPS) reports were obtained using the Dhrystone 2.1 benchmark. You can download the Dhrystone 2.1 benchmark software with the **Fast Nios II Hardware Design Example** on the Intel FPGA website. For more information about the Dhrystone 2.1 benchmark software and the Fast design example, refer to the **readme.txt** file which is included in the design example page.

The CoreMark software can be registered and downloaded at *www.eembc.org*.

Note: The Nios II Classic and Nios II benchmark data are very similar. The Nios II processor was used to create the systems which gave the data values reported in this document. Please refer to the older versions of this document for values associated with the Classic cores.

The resource utilization results were generated using moderate Analysis, Synthesis and Fitter settings in the Quartus Prime software. These results represent typical results.

(1) The Nios II/s core is only available with the Nios II Classic soft processor.

Table 1. System Configuration for Nios II Performance Benchmarks

Benchmark	Nios II Processor	I-Cache	D-Cache	Other options	Peripherals
f_{max}	Nios II/f	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer
	Nios II/e	None	None	• JTAG debug module (default)	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer
Logic size	Nios II/f	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer • Avalon UART • SDRAM controller(3)
	Nios II/e	None	None	• JTAG debug module (default)	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer • Avalon UART • SDRAM controller(3)
DMIPS	Nios II/f at 100 MHz	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 128 Kbytes On-chip RAM • JTAG UART • Timer
	Nios II/e at 100 MHz	-	-	• JTAG debug module (default)	• 128 Kbytes On-chip RAM • JTAG UART • Timer
CoreMark(2)	Nios II/f at 100 MHz	32 Kbytes	32 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 128 Kbytes On-chip RAM • JTAG UART • Timer
	Nios II/e at 100 MHz	-	-	• JTAG debug module (default)	• 128 Kbytes On-chip RAM • JTAG UART • Timer

Related Information

- Fast Nios II Hardware Design Example
- CoreMark Software Download

(2) This benchmark is compiled with the gcc -o3 switch for optimised performance.

(3) The RAM controller for the device is based on DDR3 SDRAM Controller with UniPHY. For Intel Cyclone® 10, Intel Arria® 10, and Intel Stratix® 10 devices, the RAM controller is based on the respective device IP.

1.1.1. Nios II Performance Benchmarks

Table 2. f_{max} for Nios II Processor System (MHz)

Device Family	Device used	Nios II/f (4)	Nios II/e (4)
Intel Stratix 10	1SG250LN3F43I2LG	310	320
Stratix V	5SGXEA7N2F45C1	360	410
Stratix IV	EP4S100G5H40I1	240	270
Intel Arria 10	10AX115U3F45I2LG	280	340
Arria V GZ	5AGZME7K2F40C3	280	350
Arria V	5AGXFB5K4F40I3	210	250
Intel Cyclone 10 GX	10CX220YF780E5G	270	320
Intel Cyclone 10 LP	10CL120YF780I7G	140	150
Cyclone V	5CGXFC7D6F31C6	170	210
Cyclone IV	EP4CGX30CF19C6	160	170
Intel MAX® 10	10M50DAF484C6GES	150	160

(4) Results are generated using the analysis, synthesis and fitter settings in Intel Quartus Prime 18.1 software version.

Table 3. Typical Logic Size for Nios II Processor Cores and Peripherals

Device Family	Processor Core / Peripheral						
	Nios II/f	Nios II/e	Nios II JTAG debug module	Avalon UART	JTAG UART	SDRAM Controller (5)	Timer
Intel Stratix 10 (ALM)	1029	420	148	57	74	4403	78
Stratix V (ALM)	725	289	129	61	57	2635	68
Stratix IV (ALUT)	1137	527	169	95	112	3805	92
Intel Arria 10 (ALM)	851	289	113	55	59	4166	57
Arria V GZ (ALM)	728	295	126	56	56	2629	55
Arria V (ALM)	872	301	126	56	56	2485	56
Intel Cyclone 10 GX (ALM)	874	346	115	57	63	2378	55
Intel Cyclone 10 LP (LE)	2395	838	447	141	161	428	145
Cyclone V (ALM)	867	308	125	57	57	2475	54
Cyclone IV GX (ALUT)	2283	773	348	142	159	431	137
Intel MAX 10 (LE)	2268	790	369	143	160	4636	137

Table 4. Nios II Processor Architecture Performance

Performance Metric	Nios II/f	Nios II/e
DMIPS/MHz Ratio	0.9	0.1
CoreMark	224.7	19

Related Information

- AN-440: Accelerating Nios II Networking Applications
  For more information about the Nios II networking applications performance.
- Nios II Custom Instruction User Guide
  For more information about the Nios II floating-point custom instruction performance.
- Embedded Design Handbook
  For more information about the Nios II Configuration and Booting Solutions.

(5) The RAM controller for the device is based on DDR3 SDRAM Controller with UniPHY. For Intel Cyclone 10, Intel Arria 10, and Intel Stratix 10 devices, the RAM controller is based on the respective device IP.

1.2. Document Revision History

Table 5. Document Revision History

Version	Changes
2018.10.15	• Updated for Intel Quartus Prime 18.1 version.
2017.12.18	• Updated for Intel Quartus Prime 17.1 version. • Added the Intel Cyclone 10 GX, and Intel Stratix 10 results.
2017.06.12	• Updated for Intel Quartus Prime 17.0 version. • Added the Intel Cyclone 10 LP results.
2016.06.24	• Updated for Intel Quartus Prime 16.0 version. • Added the Cyclone IV results.
2015.12.16	• Updated for Intel Quartus Prime 15.1 version. • Added the Intel Arria 10 and CoreMark results.