Altera® has two JESD204A reference design modules available—a JESD204A compatible analog-to-digital converter (ADC)-Decoder which is used to interface to JESD204A ADCs, and a JESD204A compatible digital-to-analog converter (DAC)-Encoder which is used to interface JESD204A DACs.

The two reference design modules have a limited range of configuration options and include the following features:

- M.L.F. can be configured to be 1.1.2, 2.2.2, or 2.1.4
  (M=converters per device, L=number of lanes per link, F=number of bytes per frame)
- Optional lane alignment (for the ADC-Decoder)
- 16-bit Avalon Streaming data path interfaces
- 8-bit Avalon memory-mapped configuration interface

This data sheet gives an overview of how the ADC-Decoder reference design module is used to demonstrate high-speed interoperability between an Altera Arria® II GX FPGA development board and an NXP ADC1413D evaluation board.

For more information on the Arria II GX FPGA development board, refer to the Arria II GX Development Kit web page.
The ADC1413D is a dual 125 million sample per second (MSPS) ADC with two JESD204A output lanes. The demonstration connects the ADC1413D evaluation board to the high-speed mezzanine card (HSMC) connector on the Arria II GX development board.

![Arria II GX Development Board](image)

The demonstration has the following features:

- Single link of two lanes at 2.5 Gbps per lane
- JESD204A configuration $M.L.F = 2.2.2$
- Host control of the Altera JESD204A ADC controller using System Console
- SOPC Builder support
- Serial peripheral interface (SPI) control of the AD1413D using NXP software
- 125-MHz frame clock supplied to the FPGA from the ADC1413D evaluation board

The system runs with a frame clock of 125 MHz to the ADC1413D and the JESD204A controller in the FPGA. You can configure the JES204A decoder at compile time to one of a limited range of JESD204A modes. For this demonstration, the JESD204A mode is fixed at $M.L.F = 2.2.2$. This mode represents two ADC converters ($M=2$) using one JES204A link consisting of two lanes ($L=2$). The JESD204A controller in the FPGA performs the necessary lane alignment.

The demonstration shows data capture of digitized analog input to the ADC. In data capture mode, a signal generator provides analog input to the ADC board and a block of data is captured into RAM from the Avalon® Streaming (Avalon-ST) output of the JESD204A controller. System console then loads this data to the host for analysis.
The demonstration requires the following hardware:

- Arria II GX FPGA Development Kit
- NXP ADC1413D125 Evaluation Board
- Short SMA cable

The demonstration requires the following software:

- Quartus® II software version 9.1 SP2
- MATLAB 2010a 32-bit
- NXP software support package for ADC1413D

MATLAB is only used to analyze the captured data, such as performing FFTs.

For a copy of this reference design, contact your local Altera sales representative.

**Document Revision History**

Table 1 lists the revision history for this application note.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>January 2011</td>
<td>1.0</td>
<td>Initial release.</td>
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</tbody>
</table>