Intel® Programmable Acceleration Card (PAC) with Intel® Arria® 10 GX FPGA Datasheet
Contents

1. Introduction ................................................................................................................... 3

2. Overview ........................................................................................................................ 5
   2.1. Views of the Arria 10 PAC ....................................................................................... 5
   2.2. Overview of Product Features .................................................................................. 6
       2.2.1. Intel Arria 10 GX FPGA ............................................................................. 6
       2.2.2. On-Board Memory ..................................................................................... 6
       2.2.3. Interfaces and Dimensions .......................................................................... 6
       2.2.4. Software .................................................................................................. 7
       2.2.5. Power ...................................................................................................... 7
       2.2.6. CPLD ....................................................................................................... 7
       2.2.7. QSFP+ ..................................................................................................... 7
       2.2.8. Control and Support ................................................................................. 8

3. System Compatibility .................................................................................................... 10

4. Mechanical Information ................................................................................................. 12

5. Thermal Specifications .................................................................................................. 15
   5.1. Thermal Test Performance Results .......................................................................... 16

6. FPGA Interface Manager ............................................................................................... 17
   6.1. Updating the FIM ................................................................................................. 17

7. Board Management Controller ...................................................................................... 18
   7.1. Features ............................................................................................................. 18
       7.1.1. BMC Voltage and Thermal Handling ............................................................ 19
   7.2. BMC Tools ........................................................................................................... 20
       7.2.1. BWConfig ................................................................................................ 20
       7.2.2. BwMonitor .............................................................................................. 20
   7.3. Updating the BMC Configuration and Firmware ......................................................... 25

A. Regulatory Information ................................................................................................ 26
   A.1. Japan VCCI-A Statement ...................................................................................... 26
   A.2. Korea EMI Statement ............................................................................................ 26
   A.3. United States FCC Statement .............................................................................. 26
   A.4. Canada EMC Statement ...................................................................................... 27
   A.5. Product Ecology .................................................................................................. 27
   A.6. Contact Intel Corporation ..................................................................................... 28

B. References .................................................................................................................... 29

C. Document Revision History for Intel Programmable Acceleration Card (PAC) with
   Intel Arria 10 GX FPGA Datasheet ............................................................................. 30
1. Introduction

Figure 1. Intel® PAC with Intel® Arria® 10 GX FPGA

This datasheet for the Intel® Programmable Acceleration Card (PAC) with Intel Arria® 10 GX FPGA shows electrical, mechanical, compliance, and other key specifications. This datasheet assists data center operators and system integrators to properly deploy this PAC into their servers. It also documents the FPGA power envelope, connectivity speeds to memory, and network connectivity, so that accelerator function unit (AFU) developers can properly design and test their IP.

The PAC is supported by the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs. The Intel Acceleration Stack provides a common developer interface to both application and acceleration function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA Interface Manager (FIM).

Along with acceleration libraries and development tools, the Acceleration Stack saves development time and enables code re-use across multiple Intel FPGA form-factor products, allowing the developer to focus on the unique value-additon of their solution. Developers can use the Accelerator Functional Unit (AFU) User Guide to get started.

Intel validates each Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA to support large scale deployments requiring FPGA acceleration. This platform is targeted for market-specific acceleration in applications such as:

- Big Data Analytics
- Artificial Intelligence
- Video Transcoding
- Cyber Security

*Other names and brands may be claimed as the property of others.*
1. Introduction

- Genomics
- High-Performance Computing
- Finance

Related Information

Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Arria 10 GX FPGA
2. Overview

This chapter provides an overview of the programmable acceleration card and describes the board architecture and its components.

2.1. Views of the Arria 10 PAC

Figure 2. Intel PAC Internals

Figure 3. Intel PAC Conceptual View

*Other names and brands may be claimed as the property of others.*
2.2. Overview of Product Features

2.2.1. Intel Arria 10 GX FPGA

The Intel Arria 10 FPGAs feature industry-leading programmable logic built on 20 nm process technology that integrate a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers and IP protocol controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Intel Arria 10 FPGAs to deliver floating point performance of up to 1.5 TFLOPS. Arria 10 FPGAs have a comprehensive set of power-saving features. Combined, these features allow developers to build versatile set of acceleration solutions.

When developing the accelerator function for the Intel PAC, select the 10AX11SN2F40E2LG device.

Related Information

- Intel FPGA Devices
  Detailed information about features of the Intel Arria 10 GX FPGA family

- Intel Arria 10 Device Datasheet
  This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel Arria 10 devices.

- Intel Arria 10 Device Overview
  This device overview provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

2.2.2. On-Board Memory

- 8 GB Double Data Rate 4 (DDR-4) memory
  - With error correction code (ECC)
  - 2133 Mbps
  - Two 4 GB DDR-4 memory banks, part number MT40A512M16JY-083E:B
  - Width: 64 data bits plus 8 ECC bits

  Note: Refer to the Accelerator Functional Unit (AFU) Developer’s Guide for access within the FIM to this memory link.

- One 1 GB (128 MB) Flash – for use with the FIM

Related Information

Accelerator Functional Unit (AFU) Developer’s Guide

2.2.3. Interfaces and Dimensions

- PCI Express (PCIe) x8 Gen3 electrical, x16 mechanical for stability

  Note: The PAC with Intel Arria 10 GX does not support PCIe Gen4.

- USB 2.0 interface for debugging. Also available as an alternative to PCIe for programming FPGA and flash.

- 1x Quad Small Form Factor Pluggable+ (QSFP+) with 4x 10GbE or 40GbE support.
• Conforms to 1 Rack Unit.
• ½ Length, full height card with air duct installed (default)
• ½ Length, ½ height card with air duct removed and low profile bracket installed
• Standard bracket available with air duct addition available.

Note: One rack unit is 44.5 mm (1.75 inches) high. One rack unit is commonly designated as "1U".

2.2.4. Software

• Acceleration Stack for Intel Xeon CPU with FPGAs
• FIM Installed
  Note: Certain engineering sample boards may be supplied without the FIM installed.
• Board Management Controller firmware

Related Information
Intel FPGA Acceleration Hub
Information about the Intel Acceleration Stack.

2.2.5. Power

• 66W TDP
  — The TDP is based on the max current, per the PCIe specification, of 5.5A on the 12V rail.
  — As the developers or solution provider, you must ensure that the AFU does not exceed this limit or the limit provided by the qualified server vendor. Functionality and reliability of the server is not supported for AFUs that exceed the specification.
• Up to 45 W FPGA power consumption
• The PAC source power is from the 12V rail of the PCIe* edge connector. The PAC does not draw power from the 3.3V rail.

2.2.6. CPLD

The CPLD is an Intel FPGA Download Cable. JTAG is used for debug and instances where the FIM image is corrupted or needs to be updated.

2.2.7. QSFP+

The Intel PAC with Intel Arria 10 GX FPGA has a QSFP+ cage on the front panel which supports 40GbE or four 10GbE.

The table below details the Intel -supported connectors. For volume deployment, you must use Intel-validated QSFP+ cables.

Successful functioning of 40GbE and 10GbE requires appropriate physical medium attachment (PMA) settings. Run the provided PMA settings script as detailed in the 10Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide or 40Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide.
Note: You must run the PMA settings script after every hot plug of a cable and reboot or power cycle of the server.

Table 1. QSFP+ Support for the Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

<table>
<thead>
<tr>
<th>Model Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Ethernet QSFP+ 1-meter direct attach cable (DAC) twinaxial cables</td>
</tr>
<tr>
<td>XLDACBL1</td>
</tr>
<tr>
<td>Intel Ethernet QSFP+ 3-meter direct attach cable (DAC) twinaxial cables</td>
</tr>
<tr>
<td>XLDACBL3</td>
</tr>
<tr>
<td>Intel Ethernet QSFP+ short reach (SR) optic module</td>
</tr>
<tr>
<td>E40GQSFPSR</td>
</tr>
<tr>
<td>Intel Ethernet QSFP+ 1-meter Passive Breakout Cable</td>
</tr>
<tr>
<td>X4DACBL1</td>
</tr>
<tr>
<td>Intel Ethernet QSFP+ 3-meter Passive Breakout Cable</td>
</tr>
<tr>
<td>X4DACBL3</td>
</tr>
</tbody>
</table>

Switches

Intel has validated the following switches:

Table 2. Intel-Validated Switches

<table>
<thead>
<tr>
<th>Ethernet AFU</th>
<th>Switch Brand</th>
<th>Switch Model Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 Gbps Ethernet</td>
<td>Dell*</td>
<td>Z9100-ON</td>
</tr>
<tr>
<td></td>
<td>Extreme*</td>
<td>x870-32C</td>
</tr>
<tr>
<td>10 Gbps Ethernet</td>
<td>Cisco*</td>
<td>Nexus N9K-C93180YCY-EX</td>
</tr>
<tr>
<td></td>
<td>Lenovo*</td>
<td>8272</td>
</tr>
</tbody>
</table>

QSFP+ SerDes

The QSFP+ interface has four Serializer/Deserializer (SerDes) lanes connected directly to the FPGA.

Related Information

- *Running 10GbE PAC-to-PAC Test between two connected PACs in the 10Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide*
- *Running 40GbE PAC-to-PAC Test between two connected PACs in the 40Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide*

2.2.8. Control and Support

The following features are available on this acceleration card for configuration, control and support:

- USB
- Board Management Controller (BMC)

2.2.8.1. USB Overview

This acceleration card has a USB 2.0 port for (J1) for debug and configuration in select cases. The USB interface is used for the following:
- Read/write Intel Arria 10 FPGA configuration in Flash
- Read manufacturing data via USB
- Monitor on-board temperature and power
- Update the board's BMC firmware
- JTAG access to the Intel Arria 10 FPGA through the board's embedded USB Blaster

Note: The specification of the inbound hub is USB 2.0 but it auto-negotiates from a USB 3.0 host PC.

2.2.8.2. Board Management Controller Overview

The Board Management Controller (BMC) is responsible for controlling, monitoring and giving access to low-level access to board features. The BMC microcontroller interfaces with on-board sensors, the FPGA and the flash, and it controls power and resets. The microcontroller communicates using the Intelligent Platform Management Interface (IPMI) 2.0 protocol. The firmware that runs on the BMC microcontroller is field upgradeable over USB.

You can use a BittWorks ToolKit to access utilities and libraries for communicating to devices on the platform at a higher, more abstract level.

For more details refer to the Board Management Controller section.

Related Information
Board Management Controller on page 18
3. System Compatibility

This section describes the platforms and Linux distribution targeted for the acceleration card validation.

Note: This section will be updated as Intel validates more server platforms.

Platforms

Table 3. Platform Validation

<table>
<thead>
<tr>
<th>Servers/Systems</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel</td>
<td>Neon City (NC)</td>
</tr>
<tr>
<td>Dell</td>
<td>R740, R640</td>
</tr>
</tbody>
</table>

Intel platforms have Skylake-EP and Cannonlake-EP processors in combination with the Lewisburg chipset.

Operating System Validation

Table 4. Operating System Validation

<table>
<thead>
<tr>
<th>Operating Systems (OS)</th>
<th>OS Family</th>
</tr>
</thead>
<tbody>
<tr>
<td>RHEL™ 7.4</td>
<td>RHEL</td>
</tr>
<tr>
<td>CentOS 7.4</td>
<td>CentOS</td>
</tr>
</tbody>
</table>

Note: The above mentioned Operating Systems are Linux™ Kernel 3.10

Adapters must have the following PCIe ID and power/thermal budget.

Note:
- VID - Vendor ID
- SVID - Sub Vendor ID
- DID - Device ID
- SDID - Sub Device ID

Table 5. PCIe ID and Power/Thermal Budget

<table>
<thead>
<tr>
<th>PAC</th>
<th>PCIe VID</th>
<th>PCIe DID</th>
<th>PCIe SVID</th>
<th>PCIe SDID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel PAC with Intel</td>
<td>0x8086</td>
<td>0x09C4</td>
<td>0x8086</td>
<td>0x0000</td>
</tr>
<tr>
<td>Arria 10 GX FPGA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 6. Ordering Code vs. Intel Acceleration Stack Version Compatibility

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>Intel Acceleration Stack Version</th>
<th>1.0</th>
<th>1.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>DK-ACB-10AX1151AES</td>
<td>1.0</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>DK-ACB-10AX1152AES</td>
<td>Not validated</td>
<td></td>
<td>Yes</td>
</tr>
</tbody>
</table>

*Note:* If you purchased a board from a qualified OEM, please contact the OEM to confirm which version(s) of the Acceleration Stack it supports.

### Table 7. Validated BMC and Intel Acceleration Stack Versions

<table>
<thead>
<tr>
<th>Intel Acceleration Stack Version</th>
<th>BMC Firmware Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>26815</td>
</tr>
<tr>
<td>1.1 Alpha</td>
<td>26819</td>
</tr>
<tr>
<td>1.1 Beta and Production</td>
<td>26822</td>
</tr>
</tbody>
</table>

PACs ordered under the following codes are engineering samples and should not be used for volume deployment.

### Table 8. Engineering Samples

<table>
<thead>
<tr>
<th>OPN</th>
<th>MM#</th>
</tr>
</thead>
<tbody>
<tr>
<td>DK-ACB-10AX1151AES</td>
<td>980016</td>
</tr>
<tr>
<td>DK-ACB-10AX1152AES</td>
<td>980017</td>
</tr>
</tbody>
</table>
4. Mechanical Information

**PAC Dimensions**

- Standard height, half length PCIe card
- Low profile option available
- Card Weight with Airduct: 255 g
- Maximum component height: 14.47 mm
- PCIe x16 mechanical

**Figure 4. Acceleration Card - Standard Profile Bracket with Airduct**
4. Mechanical Information

Figure 5. Air Duct Assembly

Figure 6. Acceleration Card - Low Profile Bracket
You can assemble or disassemble the air duct. Three screws hold the air duct in place. Two screws hold the bracket to the card and heat sink.

*Note:* Removal of air duct requires a different bracket to be used. Additional bracket options to support PAC without airduct available in Engineering Sample only.
5. Thermal Specifications

This acceleration card is thermally limited to dissipate no more than 45 W on the FPGA. FPGA junction temperature must not exceed 95°C. Make sure the temperature of the QSFP+ module is within the vendor specification, usually 70°C or 85°C.

- Operating Temperature: 95 °C
- Shutdown Temperature: 100 °C

**Note:** Refer to the Power Estimator Guide to avoid exceeding 95 °C.

**Note:** Intel PAC with Arria 10 GX Verification and Power Estimator User Guide describes how to verify and ensure that the AFU operates within the power supported by this card. The link to the user guide is not available and shall be provided in a future release.

**Note:** AFU Developers should use the *Arria 10 PowerPlay Early Power Estimator* and the Quartus Prime Power Analyzer to estimate power consumption.

**Figure 8.** Airflow Pattern

**Related Information**

*Power Analysis and Optimization User Guide: Intel Quartus® Prime Pro Edition*

### 5.1. Thermal Test Performance Results

#### Table 9. Terms and Descriptions

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear Feet per Minute (LFM)</td>
<td>Air velocity is calculated by dividing the volumetric flow rate by the cross-sectional area of the flow passage.</td>
</tr>
<tr>
<td>$T_{LA}$</td>
<td>The measured ambient temperature locally surrounding the FPGA. The ambient temperature should be measured just upstream of a passive heatsink or at fan inlet for an active heatsink.</td>
</tr>
</tbody>
</table>

#### Table 10. $T_{LA}$ vs. Velocity Profile with Air Duct

<table>
<thead>
<tr>
<th>$T_{LA}$ (°C)</th>
<th>Velocity (LFM) (85 °C QSFP spec)</th>
<th>Velocity (LFM) (70 °C QSFP spec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>270</td>
<td>270</td>
</tr>
<tr>
<td>35</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>40</td>
<td>360</td>
<td>360</td>
</tr>
<tr>
<td>45</td>
<td>420</td>
<td>420</td>
</tr>
<tr>
<td>50</td>
<td>510</td>
<td>510</td>
</tr>
<tr>
<td>55</td>
<td>660</td>
<td>690</td>
</tr>
</tbody>
</table>

#### Table 11. $T_{LA}$ vs. Velocity Profile without Air Duct

<table>
<thead>
<tr>
<th>$T_{LA}$ (°C)</th>
<th>Velocity (LFM) (85 °C QSFP spec)</th>
<th>Velocity (LFM) (70 °C QSFP spec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>330</td>
<td>330</td>
</tr>
<tr>
<td>35</td>
<td>390</td>
<td>390</td>
</tr>
<tr>
<td>40</td>
<td>420</td>
<td>420</td>
</tr>
<tr>
<td>45</td>
<td>510</td>
<td>510</td>
</tr>
<tr>
<td>50</td>
<td>600</td>
<td>630</td>
</tr>
<tr>
<td>55</td>
<td>810</td>
<td>870</td>
</tr>
</tbody>
</table>
6. FPGA Interface Manager

The FPGA Interface Manager (FIM) contains the FPGA logic to support the accelerators, including the PCIe IP core, the Core Cache Interface protocol (CCI-P) fabric, the onboard DDR memory interface, and management engine. Specific features of the FIM are listed in the following documents:

- Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
- OPAE Intel FPGA Linux Device Driver Architecture Guide

The 1024 Mb flash memory stores the FPGA Interface Manager (FIM) which provides a common user interface for placement of accelerator functions. In addition, the FIM allows dynamic downloading of new accelerator functions and updates to the FIM.

The FIM can read the FPGA temperature through the Intel Acceleration Stack. Use the following command:

```
sudo fpgainfo temp
```

6.1. Updating the FIM

The FIM image in flash memory can be updated using the following methods:

- The primary method is for the FIM to be updated over PCIe via the Acceleration Stack program `fpgaflash`. This loads the FIM image into the onboard flash memory. Upon power up, the board loads the image from flash onto the FPGA.

- Directly configure the FPGA via JTAG through the USB port. This use case should only be used if the FIM image gets corrupted or erased.

**Note:** Please refer to the Intel Acceleration Stack Quick Start Guide for the Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA for instructions on updating the FIM.
7. Board Management Controller

A board management controller (BMC) resides on the Intel PAC with Intel Arria 10 GX FPGA.

7.1. Features

The on-board microcontroller:

- Provides low-level access to board features.
- Interfaces with sensors, FPGA, flash and QSFP.
- Controls power and resets on the board.
- Monitors temperatures, voltages and currents and provides protective action when readings are outside of critical thresholds.
- Provides PLDM extensions for PCIe I²C communication. The I²C slave address is 0xCE.
- Supports field upgrades of BMC firmware.
7.1.1. BMC Voltage and Thermal Handling

The BMC powers down the Intel PAC with Intel Arria 10 GX FPGA and reboots the server if the power, temperature or voltage reaches a certain threshold. This response prevents damage to the server or Intel PAC with Intel Arria 10 GX FPGA.

For threshold limits refer to the Device Peripheral Table section. This table shows the upper non-recoverable (UNR) value, which specifies the shutdown condition. The BMC will shut down power to the board under conditions that include the following:

- Total board power is approximately 80W (based on the 12V backplane current and the UNR of 6.66A)
- FPGA junction temperature reaches 100°C

Note: To avoid unintended shutdown and loss of data:

- Use an Intel validated server.
- Perform extensive power validation and consumption analysis on worst-case workloads.
- Use a qualified solution that is stress-tested across multiple servers and long durations.
You can identify whether the BMC has detected a board failure from the two on-board LEDs. Looking into the bracket of the Intel PAC through the venting holes on the back side of the server, you can see four steadily ON green LEDs. Behind them (further into the board), there is either a green LED or red LED that is on. The green LED blinks whenever the BMC is operating and is steadily on if the BMC is being initialized. When the BMC detects a failure condition and holds off board power, a red LED (next to the green LED) will be steadily on. Board failure conditions may occur because of an overheated FPGA or too much power draw from the board.

Related Information
Device Peripheral Table on page 23

7.2. BMC Tools

The BittWare Toolkit features several utilities that allow you to configure your device in the system, interact with FPGA and debug the FPGA, control the BMC on your board, and access the board from a remote system.

To use the BWConfig and BwMonitor tools, you need a Micro-USB cable to connect the acceleration card to any USB port on host server.

Before using BwMonitor to get telemetry data from Acceleration card, you need to run BWConfig, scan the USB bus, find the card being tested, and map it as device 0.

7.2.1. BWConfig

BwConfig is a utility for configuring the BMC in a system. BwConfig:

- Controls BMC hardware on the platform
- Scans and maps new devices through PCIe or USB
- Views device properties
- Controls FPGA boot and flash loading
- Can backup flash to restore a factory default image over PCIe
- Supports resetting and loading FPGA images without the need to attach additional cables or hardware

7.2.2. BwMonitor

BwMonitor provides a view into the board management capabilities of your Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA. You can use BwMonitor through a GUI or console. Bwmonitor allows you to:

- View board health
- Read and log sensors
- Control sensor thresholds that determine when the board will shut down
- Load programmable clocks
- Override voltages
- Access devices via I²C
- Upgrade the BMC firmware
- Monitor the board over PCIe or USB
7.2.2.1. bwmonitor --read Command

Use the --read command in the console to read any combination or number of the available peripheral devices. The following table describes the additional arguments that can be used with the --read command.

<table>
<thead>
<tr>
<th>Available Arguments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--type</td>
<td>Narrows results to a certain type of peripheral device, for example sensors.</td>
</tr>
<tr>
<td>--id</td>
<td>Use in conjunction with the --type argument to read only one device.</td>
</tr>
<tr>
<td>--loop</td>
<td>Continues reading sensors in a loop.</td>
</tr>
<tr>
<td>--read_every</td>
<td>Controls how often the sensors are read.</td>
</tr>
</tbody>
</table>

### Example: Read all peripheral devices

```
bwmonitor --dev=0 --read
```

**Board Management Controller (BMC)**

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(0)</td>
<td>cPLD</td>
<td>Version 3</td>
</tr>
<tr>
<td>(1)</td>
<td>MCU</td>
<td>Version 14952</td>
</tr>
</tbody>
</table>

**SDR Sensors**

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(2)</td>
<td>12v Backplane</td>
<td>OK</td>
</tr>
<tr>
<td>(3)</td>
<td>Backplane Current</td>
<td>OK</td>
</tr>
<tr>
<td>(4)</td>
<td>12v Connector</td>
<td>Warning-lo</td>
</tr>
<tr>
<td>(5)</td>
<td>Connector Current</td>
<td>Warning-lo</td>
</tr>
<tr>
<td>(6)</td>
<td>Inlet</td>
<td>OK</td>
</tr>
<tr>
<td>(7)</td>
<td>FPGA Local</td>
<td>OK</td>
</tr>
<tr>
<td>(8)</td>
<td>FPGA Core</td>
<td>OK</td>
</tr>
</tbody>
</table>

**Pluggable Transceivers (SFP)**

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(0)</td>
<td>QSFP-1</td>
<td>Not present</td>
</tr>
<tr>
<td>(1)</td>
<td>QSFP-2</td>
<td>Not present</td>
</tr>
</tbody>
</table>

**Programmable Clocks (PLL)**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(0)</td>
<td>Si5338-A</td>
</tr>
<tr>
<td>(1)</td>
<td>Si5338-B</td>
</tr>
<tr>
<td>(2)</td>
<td>AD9518</td>
</tr>
</tbody>
</table>

### Example: Read all sensors

```
bwmonitor --dev=0 --read --type=sensor
```

**SDR Sensors**

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(2)</td>
<td>12v Backplane</td>
<td>OK</td>
</tr>
<tr>
<td>(3)</td>
<td>Backplane Current</td>
<td>OK</td>
</tr>
<tr>
<td>(4)</td>
<td>12v Connector</td>
<td>Warning-lo</td>
</tr>
<tr>
<td>(5)</td>
<td>Connector Current</td>
<td>Warning-lo</td>
</tr>
<tr>
<td>(6)</td>
<td>Inlet</td>
<td>OK</td>
</tr>
<tr>
<td>(7)</td>
<td>FPGA Local</td>
<td>OK</td>
</tr>
<tr>
<td>(8)</td>
<td>FPGA Core</td>
<td>OK</td>
</tr>
</tbody>
</table>

### Example: Read the FPGA Core Temperature Sensor

```
bwmonitor --dev=0 --read=8 --type=sensor
```

**SDR Sensors**

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(8)</td>
<td>FPGA Core</td>
<td>OK</td>
</tr>
</tbody>
</table>
7.2.2.2. How to Invoke the BMC GUI

1. Type the following command:
   
   `bwmonitor -gui &`

2. Click `connect`
7.2.2.3. BMC Settings

Right-click any sensor with a green icon to open the Sensor Thresholds dialog box.

Figure 10. Board Power Sensor Threshold Window

7.2.2.4. Device Peripheral Table

The following table describes the peripherals, currents or voltages that you can monitor on the Intel PAC with Intel Arria 10 GX FPGA:

- **Type**: Indicates the origin of measurement
- **Channel and Address columns**: Indicate the virtual I²C channel and address that are used to access the peripheral through the microcontroller.
- **SRD/ID**: Indicate the sensor data record (sdr) index; otherwise, the SDR/ID column indicates the device number (dev), if any, to be passed to the relevant IPMI command or BMC library functions.
- **UNC**: Upper non-critical value
- **UC**: Upper critical value
- **UNR**: Upper non-recoverable value: the threshold for power shutdown (1)

(1) For a detailed discussion of UNR, refer to BMC Voltage and Thermal Handling
### Table 13. Device Peripheral Table

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Channel</th>
<th>Address</th>
<th>ID (dev/sdr)</th>
<th>UNC</th>
<th>UC</th>
<th>UNR</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board Power</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>75</td>
<td>100</td>
<td>113</td>
<td></td>
</tr>
<tr>
<td>12v Backplane Current</td>
<td>Sensor</td>
<td>5</td>
<td>0xD4</td>
<td>1</td>
<td>5.5</td>
<td>6</td>
<td>6.66</td>
<td>LTC4151 Input Current</td>
</tr>
<tr>
<td>12v Backplane Voltage</td>
<td>Sensor</td>
<td>5</td>
<td>0xD4</td>
<td>2</td>
<td>13.5</td>
<td>14</td>
<td>14</td>
<td>LTC4151 Input Voltage</td>
</tr>
<tr>
<td>1.2v Current</td>
<td>Sensor</td>
<td>6</td>
<td>0xD0</td>
<td>3</td>
<td>12</td>
<td>13</td>
<td>15</td>
<td>LTC4151 Output Current</td>
</tr>
<tr>
<td>1.2v Voltage</td>
<td>Sensor</td>
<td>6</td>
<td>0xD0</td>
<td>4</td>
<td>1.26</td>
<td>1.3</td>
<td>1.4</td>
<td>LTC4151 Output Voltage</td>
</tr>
<tr>
<td>1.8v Current</td>
<td>Sensor</td>
<td>6</td>
<td>0xD2</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>LTC4151 Output Current</td>
</tr>
<tr>
<td>1.8v Voltage</td>
<td>Sensor</td>
<td>6</td>
<td>0xD2</td>
<td>6</td>
<td>1.9</td>
<td>2</td>
<td>2.04</td>
<td>LTC4151 Output Voltage</td>
</tr>
<tr>
<td>3.3v Current</td>
<td>Sensor</td>
<td>6</td>
<td>0xD4</td>
<td>7</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>LTC4151 Output Current</td>
</tr>
<tr>
<td>3.3v Voltage</td>
<td>Sensor</td>
<td>6</td>
<td>0xD4</td>
<td>8</td>
<td>3.47</td>
<td>3.6</td>
<td>3.96</td>
<td>LTC4151 Output Voltage</td>
</tr>
<tr>
<td>FPGA Core Voltage</td>
<td>Sensor</td>
<td>6</td>
<td>0xDA</td>
<td>9</td>
<td>0.95</td>
<td>1</td>
<td>1.08</td>
<td>LTC4151 Output Voltage</td>
</tr>
<tr>
<td>FPGA Core Current</td>
<td>Sensor</td>
<td>6</td>
<td>0xDA</td>
<td>10</td>
<td>50</td>
<td>55</td>
<td>60</td>
<td>LTC4151 Output Current</td>
</tr>
<tr>
<td>FPGA Core Temperature</td>
<td>Sensor</td>
<td>0</td>
<td>0x98</td>
<td>11</td>
<td>90</td>
<td>95</td>
<td>100</td>
<td>NCT72CMTR2G External</td>
</tr>
<tr>
<td>Core Supply Temperature</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>12</td>
<td>100</td>
<td>110</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>Board Temperature</td>
<td>Sensor</td>
<td>0</td>
<td>0x98</td>
<td>13</td>
<td>70</td>
<td>75</td>
<td>80</td>
<td>NCT72CMTR2G Local</td>
</tr>
<tr>
<td>QSFP Temperature</td>
<td>Sensor</td>
<td>3</td>
<td>0xA0</td>
<td>14</td>
<td>70</td>
<td>80</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>QSFP Voltage</td>
<td>Sensor</td>
<td>3</td>
<td>0xA0</td>
<td>15</td>
<td>3.4</td>
<td>3.5</td>
<td>3.7</td>
<td></td>
</tr>
<tr>
<td>VCCR Voltage</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCT Voltage</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>17</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>VCCR Current</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>VCCT Current</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VPP Voltage</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>VTT Voltage</td>
<td>Sensor</td>
<td>-</td>
<td>-</td>
<td>21</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>QSFP</td>
<td>SFP/QSFP</td>
<td>-</td>
<td>0xA0</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Si5338</td>
<td>Programmable Clock</td>
<td>0</td>
<td>0xE0</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Defaults to 125, 125, 266.666667, 266.666667</td>
</tr>
<tr>
<td>MAC Prom</td>
<td>Network</td>
<td>4</td>
<td>0xA0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>AT24CS04</td>
</tr>
</tbody>
</table>

**Related Information**

BMC Voltage and Thermal Handling on page 19
7.3. Updating the BMC Configuration and Firmware

The BMC contains an in-system programmable USB boot loader for upgrading the firmware over USB. Intel provides the firmware for image upgrades. The upgrade process takes seconds and the board is reset when the upgrade is complete. For directions on how to update the BMC configuration and firmware, you must refer to the *Updating the Board Management Controller (BMC) Configuration and Firmware* section in the Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA.

*Note:* You must use a local USB cable to update any BMC firmware provided by Intel, an OEM, or an ODM.

**Related Information**

Intel Acceleration Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
A. Regulatory Information

A.1. Japan VCCI-A Statement

この装置は、クラスA情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されます。

VCCI-A

A.2. Korea EMI Statement

사용자 안내문 : A 급 기기

이 기기는 업무용으로 전자파적합등록을 받은 기기이오니, 판매자 또는 사용자는 이 절을 주의 하시기 바라며, 만약 잘못 구입 하셨을 때에는 구입한 곳에서 비업무용으로 교환 하시키 바랍니다.

A.3. United States FCC Statement

This device complies with Part 15 of the United States Federal Communications Commission (FCC) Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment, does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

• Reorient or relocate the receiving antenna
• Increase the separation between the equipment and receiver
• Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
• Consult the dealer or an experienced radio/TV technician for help
A.4. Canada EMC Statement

Class A: CAN ICES-3 (A)/NMB-3(A)

A.5. Product Ecology
A.6. Contact Intel Corporation

Intel Corporation
ATTN: Corporate Quality
2200 Mission College Blvd.
Santa Clara, CA 95054
USA
B. References

Related Information

Intel Arria 10 GX/GT Device Errata and Design Recommendations

This errata sheet provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.
## C. Document Revision History for Intel Programmable Acceleration Card (PAC) with Intel Arria 10 GX FPGA Datasheet

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018.08.16</td>
<td>Corrected broken link in FPGA Interface Manager.</td>
</tr>
</tbody>
</table>
| 2018.08.06       | Updated the following sections:  
|                  | • Introduction  
|                  | • Block Diagram  
|                  | • QSFP+  
|                  | • System Compatibility  
|                  | • Interfaces and Dimensions  
|                  | Added substantial content to the Board Management Controller chapter |
| 2018.04.11       | Updated the following sections:  
|                  | • On-Board Memory on page 6  
|                  | • QSFP+ on page 7  
|                  | • Power on page 7  
|                  | • Board Management Controller on page 18  
|                  | • System Compatibility on page 10  
|                  | • Mechanical Information on page 12  
|                  | • Thermal Specifications on page 15 |
| 2018.01.22       | Updated the following sections:  
|                  | • Introduction on page 3  
|                  | • On-Board Memory on page 6  
|                  | • Interfaces and Dimensions on page 6  
|                  | • Power on page 7  
|                  | • CPLD on page 7  
|                  | • Board Management Controller on page 18  
|                  | • Mechanical Information on page 12  
|                  | • Thermal Test Performance Results on page 16  
|                  | • Regulatory Information on page 26 |
| 2017.11.03       | Engineering Sample (ES) Release |