Digital Channelizer

Reference Design Datasheet

Description

Electronic Warfare Jammers need to analyze wide bandwidths with low signal-to-noise ratios (SNR) to detect critical, time sensitive threats. One way to achieve this is to channelize the wide bandwidth to separate signals of interest from noise and interferers through a filter bank and Fast Fourier Transform (FFT).

To streamline this effort, Altera has developed a highly parameterizable and efficient super- sample rate FFT IP. This allows the designer to select the number of phases and size of the FFT for DSP Builder Advanced Blockset to output an efficient implementation for GHz sample rate ADC's. To demonstrate this capability, Altera has teamed with Bittware to channelize a 2.5GHz ADC into various channels which is then displayed in Matlab via Altera's system-in-the-loop feature.

For additional information, please contact us at *mil@altera.com* or *contact your local Altera sales representative*.

Features

- Programmable super sample rate FFT IP
- Programmable filter bank IP
- Floating point and fixed point implementation
- Altera's System-in-the-Loop with MATLAB®
- Bittware COTS S56X VPX platform with FMC high speed ADC, up to 5Gsps at 10-bits
- Push button 0.5 Million point FFT in A10 designed with Simulink®/Advanced DSP Builder

Applications

- Digital Electronic Warfare Jammer
- Digital Multirate Filter Bank

Figure 1: General Electronic Warfare System Block Diagram

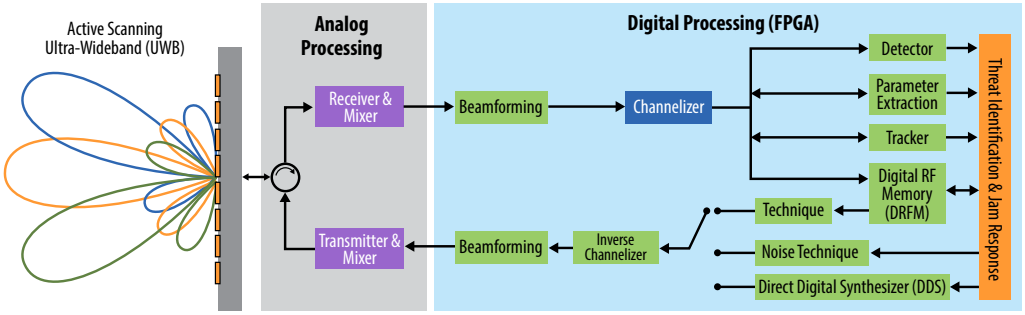

Figure 2: Bittware VPX board supporting the Altera EW ultra-wideband channelizer reference design

Figure 3: Bittware detailed discussion on how the Bittware VPX board works in context of EW systems and the Altera EW ultra-wideband channelizer reference design; Military Embedded Systems, January 29, 2014

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