Pin Information For The Stratix™ GX EP1SGX40G Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		VCCA_PLL7			J27		
		GND					
		GNDA_PLL7			K27		
		VCCG_PLL7			J26		
		GNDG_PLL7			K26		
B2	VREF0B2	FPLL7CLKp			E29		
B2	VREF0B2	FPLL7CLKn			E30		
B2	VREF0B2	INPUT	DIFFIO_RX44p		D29		
B2	VREF0B2	INPUT	DIFFIO_RX44n		D30		
B2	VREF0B2	IO	DIFFIO_TX44p		F27		
B2	VREF0B2	IO	DIFFIO_TX44n		F28		
B2	VREF0B2	INPUT	DIFFIO_RX43p		D31		
B2	VREF0B2	INPUT	DIFFIO_RX43n		D32		
B2	VREF0B2	IO	DIFFIO_TX43p		G27		
B2	VREF0B2	IO	DIFFIO_TX43n		G28		
B2	VREF0B2	INPUT	DIFFIO_RX42p		F29		
B2	VREF0B2	INPUT	DIFFIO_RX42n		F30		
B2	VREF0B2	IO	DIFFIO_TX42p		G25		
B2	VREF0B2	IO	DIFFIO_TX42n		G26		
B2	VREF0B2	VREF0B2			M24		
B2	VREF0B2	INPUT	DIFFIO_RX41p		E31		
B2	VREF0B2	INPUT	DIFFIO_RX41n		E32		
B2	VREF0B2	IO	DIFFIO_TX41p		J28		
B2	VREF0B2	IO	DIFFIO_TX41n		H28		
B2	VREF0B2	INPUT	DIFFIO_RX40p		F31		
B2	VREF0B2	INPUT	DIFFIO_RX40n		F32		
B2	VREF0B2	IO	DIFFIO_TX40p		H26		
B2	VREF0B2	IO	DIFFIO_TX40n		H27		
B2	VREF0B2	INPUT	DIFFIO_RX39p		G29		
B2	VREF0B2	INPUT	DIFFIO_RX39n		G30		
B2	VREF0B2	IO	DIFFIO_TX39p		H24		
B2	VREF0B2	IO	DIFFIO_TX39n		H25		
B2	VREF0B2	INPUT	DIFFIO_RX38p		G31		
B2	VREF0B2	INPUT	DIFFIO_RX38n		G32		
B2	VREF0B2	IO	DIFFIO_TX38p		L28		
B2	VREF0B2	IO	DIFFIO_TX38n		K28		
B2	VREF1B2	INPUT	DIFFIO_RX37p		H29		
B2	VREF1B2	INPUT	DIFFIO_RX37n		H30		
B2	VREF1B2	IO	DIFFIO_TX37p		J24		
B2	VREF1B2	IO	DIFFIO_TX37n		J25		
B2	VREF1B2	INPUT	DIFFIO_RX36p		K29		
B2	VREF1B2	INPUT	DIFFIO_RX36n		K30		
B2	VREF1B2	IO	DIFFIO_TX36p		K24		
B2	VREF1B2	IO	DIFFIO_TX36n		K25		
B2	VREF1B2	INPUT	DIFFIO_RX35p		H31		
B2	VREF1B2	INPUT	DIFFIO_RX35n		H32		
B2	VREF1B2	IO	DIFFIO_TX35p		L24		
B2	VREF1B2	IO	DIFFIO_TX35n		L25		
B2	VREF1B2	INPUT	DIFFIO_RX34p		J31		
B2	VREF1B2	INPUT	DIFFIO_RX34n		J32		
B2	VREF1B2	IO	DIFFIO_TX34p		L26		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B2	VREF1B2	IO	DIFFIO_TX34n		L27		
B2	VREF1B2	VREF1B2			P23		
B2	VREF1B2	INPUT	DIFFIO_RX33p		J29		
B2	VREF1B2	INPUT	DIFFIO_RX33n		J30		
B2	VREF1B2	IO	DIFFIO_TX33p		M25		
B2	VREF1B2	IO	DIFFIO_TX33n		M26		
B2	VREF1B2	INPUT	DIFFIO_RX32p/RUP2		L29		
B2	VREF1B2	INPUT	DIFFIO_RX32n/RDN2		L30		
B2	VREF1B2	IO	DIFFIO_TX32p		M27		
B2	VREF1B2	IO	DIFFIO_TX32n		M28		
B2	VREF1B2	INPUT	DIFFIO_RX31p		L31		
B2	VREF1B2	INPUT	DIFFIO_RX31n		L32		
B2	VREF1B2	IO	DIFFIO_TX31p		N25		
B2	VREF1B2	IO	DIFFIO_TX31n		N26		
B2	VREF1B2	INPUT	DIFFIO_RX30p		M29		
B2	VREF1B2	INPUT	DIFFIO_RX30n		M30		
B2	VREF1B2	IO	DIFFIO_TX30p		N27		
B2	VREF1B2	IO	DIFFIO_TX30n		N28		
B2	VREF2B2	INPUT	DIFFIO_RX29p		N29		
B2	VREF2B2	INPUT	DIFFIO_RX29n		N30		
B2	VREF2B2	IO	DIFFIO_TX29p		P25		
B2	VREF2B2	IO	DIFFIO_TX29n		P26		
B2	VREF2B2	INPUT	DIFFIO_RX28p		K31		
B2	VREF2B2	INPUT	DIFFIO_RX28n		K32		
B2	VREF2B2	IO	DIFFIO_TX28p		P24		
B2	VREF2B2	IO	DIFFIO_TX28n		R24		
B2	VREF2B2	INPUT	DIFFIO_RX27p		M31		
B2	VREF2B2	INPUT	DIFFIO_RX27n		M32		
B2	VREF2B2	IO	DIFFIO_TX27p		P27		
B2	VREF2B2	IO	DIFFIO_TX27n		P28		
B2	VREF2B2	INPUT	DIFFIO_RX26p		P29		
B2	VREF2B2	INPUT	DIFFIO_RX26n		P30		
B2	VREF2B2	IO	DIFFIO_TX26p		R27		
B2	VREF2B2	IO	DIFFIO_TX26n		R28		
B2	VREF2B2	VREF2B2			R23		
B2	VREF2B2	INPUT	DIFFIO_RX25p		N31		
B2	VREF2B2	INPUT	DIFFIO_RX25n		N32		
B2	VREF2B2	IO	DIFFIO_TX25p		R25		
B2	VREF2B2	IO	DIFFIO_TX25n		R26		
B2	VREF2B2	INPUT	DIFFIO_RX24p		P31		
B2	VREF2B2	INPUT	DIFFIO_RX24n		R31		
B2	VREF2B2	IO	DIFFIO_TX24p		K23		
B2	VREF2B2	IO	DIFFIO_TX24n		J23		
B2	VREF2B2	INPUT	DIFFIO_RX23p		R29		
B2	VREF2B2	INPUT	DIFFIO_RX23n		R30		
B2	VREF2B2	IO	DIFFIO_TX23p		M23		
B2	VREF2B2	IO	DIFFIO_TX23n		L23		
B2	VREF2B2	CLK0n			T32		
B2	VREF2B2	CLK0p			T31		
B2	VREF2B2	IO	CLK1n		T30		
B2	VREF2B2	CLK1p			T29		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		VCCA_PLL1			T27		
		GND					
		GNDA_PLL1			T28		
		VCCG_PLL1			T25		
		GNDG_PLL1			T26		
		VCCA_PLL2			U27		
		GND					
		GNDA_PLL2			U28		
		VCCG_PLL2			U25		
		GNDG_PLL2			U26		
B1	VREF0B1	CLK2p			U31		
B1	VREF0B1	CLK2n			U32		
B1	VREF0B1	CLK3p			U29		
B1	VREF0B1	IO	CLK3n		U30		
B1	VREF0B1	INPUT	DIFFIO_RX22p		V29		
B1	VREF0B1	INPUT	DIFFIO_RX22n		V30		
B1	VREF0B1	IO	DIFFIO_TX22p		T23		
B1	VREF0B1	IO	DIFFIO_TX22n		U24		
B1	VREF0B1	INPUT	DIFFIO_RX21p		V31		
B1	VREF0B1	INPUT	DIFFIO_RX21n		W31		
B1	VREF0B1	IO	DIFFIO_TX21p		AA23		
B1	VREF0B1	IO	DIFFIO_TX21n		AB23		
B1	VREF0B1	INPUT	DIFFIO_RX20p		Y31		
B1	VREF0B1	INPUT	DIFFIO_RX20n		Y32		
B1	VREF0B1	IO	DIFFIO_TX20p		AC23		
B1	VREF0B1	IO	DIFFIO_TX20n		AD23		
B1	VREF0B1	VREF0B1			V23		
B1	VREF0B1	INPUT	DIFFIO_RX19p		W29		
B1	VREF0B1	INPUT	DIFFIO_RX19n		W30		
B1	VREF0B1	IO	DIFFIO_TX19p		V27		
B1	VREF0B1	IO	DIFFIO_TX19n		V28		
B1	VREF0B1	INPUT	DIFFIO_RX18p		AA31		
B1	VREF0B1	INPUT	DIFFIO_RX18n		AA32		
B1	VREF0B1	IO	DIFFIO_TX18p		V25		
B1	VREF0B1	IO	DIFFIO_TX18n		V26		
B1	VREF0B1	INPUT	DIFFIO_RX17p		AC31		
B1	VREF0B1	INPUT	DIFFIO_RX17n		AC32		
B1	VREF0B1	IO	DIFFIO_TX17p		V24		
B1	VREF0B1	IO	DIFFIO_TX17n		W24		
B1	VREF0B1	INPUT	DIFFIO_RX16p		Y29		
B1	VREF0B1	INPUT	DIFFIO_RX16n		Y30		
B1	VREF0B1	IO	DIFFIO_TX16p		W27		
B1	VREF0B1	IO	DIFFIO_TX16n		W28		
B1	VREF1B1	INPUT	DIFFIO_RX15p		AB31		
B1	VREF1B1	INPUT	DIFFIO_RX15n		AB32		
B1	VREF1B1	IO	DIFFIO_TX15p		W25		
B1	VREF1B1	IO	DIFFIO_TX15n		W26		
B1	VREF1B1	INPUT	DIFFIO_RX14p		AA29		
B1	VREF1B1	INPUT	DIFFIO_RX14n		AA30		
B1	VREF1B1	IO	DIFFIO_TX14p		Y25		
B1	VREF1B1	IO	DIFFIO_TX14n		Y26		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B1	VREF1B1	INPUT	DIFFIO_RX13p/RUP1		AB29		
B1	VREF1B1	INPUT	DIFFIO_RX13n/RDN1		AB30		
B1	VREF1B1	IO	DIFFIO_TX13p		Y27		
B1	VREF1B1	IO	DIFFIO_TX13n		Y28		
B1	VREF1B1	INPUT	DIFFIO_RX12p		AC29		
B1	VREF1B1	INPUT	DIFFIO_RX12n		AC30		
B1	VREF1B1	IO	DIFFIO_TX12p		AA25		
B1	VREF1B1	IO	DIFFIO_TX12n		AA26		
B1	VREF1B1	VREF1B1			W23		
B1	VREF1B1	INPUT	DIFFIO_RX11p		AD31		
B1	VREF1B1	INPUT	DIFFIO_RX11n		AD32		
B1	VREF1B1	IO	DIFFIO_TX11p		AA27		
B1	VREF1B1	IO	DIFFIO_TX11n		AA28		
B1	VREF1B1	INPUT	DIFFIO_RX10p		AE31		
B1	VREF1B1	INPUT	DIFFIO_RX10n		AE32		
B1	VREF1B1	IO	DIFFIO_TX10p		AB26		
B1	VREF1B1	IO	DIFFIO_TX10n		AB27		
B1	VREF1B1	INPUT	DIFFIO_RX9p		AE29		
B1	VREF1B1	INPUT	DIFFIO_RX9n		AE30		
B1	VREF1B1	IO	DIFFIO_TX9p		AB24		
B1	VREF1B1	IO	DIFFIO_TX9n		AB25		
B1	VREF1B1	INPUT	DIFFIO_RX8p		AD29		
B1	VREF1B1	INPUT	DIFFIO_RX8n		AD30		
B1	VREF1B1	IO	DIFFIO_TX8p		AC24		
B1	VREF1B1	IO	DIFFIO_TX8n		AC25		
B1	VREF1B1	INPUT	DIFFIO_RX7p		AF29		
B1	VREF1B1	INPUT	DIFFIO_RX7n		AF30		
B1	VREF2B1	IO	DIFFIO_TX7p		AD24		
B1	VREF2B1	IO	DIFFIO_TX7n		AD25		
B1	VREF2B1	INPUT	DIFFIO_RX6p		AF31		
B1	VREF2B1	INPUT	DIFFIO_RX6n		AF32		
B1	VREF2B1	IO	DIFFIO_TX6p		AB28		
B1	VREF2B1	IO	DIFFIO_TX6n		AC28		
B1	VREF2B1	INPUT	DIFFIO_RX5p		AG31		
B1	VREF2B1	INPUT	DIFFIO_RX5n		AG32		
B1	VREF2B1	IO	DIFFIO_TX5p		AE24		
B1	VREF2B1	IO	DIFFIO_TX5n		AE25		
B1	VREF2B1	INPUT	DIFFIO_RX4p		AG29		
B1	VREF2B1	INPUT	DIFFIO_RX4n		AG30		
B1	VREF2B1	IO	DIFFIO_TX4p		AE26		
B1	VREF2B1	IO	DIFFIO_TX4n		AE27		
B1	VREF2B1	VREF2B1			AA24		
B1	VREF2B1	INPUT	DIFFIO_RX3p		AH31		
B1	VREF2B1	INPUT	DIFFIO_RX3n		AH32		
B1	VREF2B1	IO	DIFFIO_TX3p		AD28		
B1	VREF2B1	IO	DIFFIO_TX3n		AE28		
B1	VREF2B1	INPUT	DIFFIO_RX2p		AJ31		
B1	VREF2B1	INPUT	DIFFIO_RX2n		AJ32		
B1	VREF2B1	IO	DIFFIO_TX2p		AF25		
B1	VREF2B1	IO	DIFFIO_TX2n		AF26		
B1	VREF2B1	INPUT	DIFFIO_RX1p		AJ29		

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Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B1	VREF2B1	INPUT	DIFFIO_RX1n		AJ30		
B1	VREF2B1	IO	DIFFIO_TX1p		AF27		
B1	VREF2B1	IO	DIFFIO_TX1n		AF28		
B1	VREF2B1	INPUT	DIFFIO_RX0p		AH27		
B1	VREF2B1	INPUT	DIFFIO_RX0n		AH28		
B1	VREF2B1	IO	DIFFIO_TX0p		AG27		
B1	VREF2B1	IO	DIFFIO_TX0n		AG28		
B1	VREF2B1	FPLL8CLKn			AH30		
B1	VREF2B1	FPLL8CLKp			AH29		
B1	VREF2B1	IO			AG25		
B1	VREF2B1	IO			AG26		
		VCCA_PLL8			AD27		
		GND					
		GNDA_PLL8			AC27		
		VCCG_PLL8			AD26		
		GNDG_PLL8			AC26		
B8	VREF0B8	IO	DQ9B7		AK29	DQ3B15	DQ1B31
B8	VREF0B8	IO			AK31		
B8	VREF0B8	IO	DQ9B6		AL29	DQ3B14	DQ1B30
B8	VREF0B8	IO			AL30		
B8	VREF0B8	IO	DQ9B5		AM29	DQ3B13	DQ1B29
B8	VREF0B8	IO	DQ9B4		AK28	DQ3B12	DQ1B28
B8	VREF0B8	IO			AL31		
B8	VREF0B8	IO	DQ9B3		AL28	DQ3B11	DQ1B27
B8	VREF0B8	IO			AJ28		
B8	VREF0B8	IO	DQS9B		AM28		
B8	VREF0B8	VREF0B8			AA22		
B8	VREF0B8	IO			AK30		
B8	VREF0B8	IO	DQ9B2		AK27	DQ3B10	DQ1B26
B8	VREF0B8	IO			AJ27		
B8	VREF0B8	IO	DQ9B1		AL27	DQ3B9	DQ1B25
B8	VREF0B8	IO			AH26		
B8	VREF0B8	IO	DQ9B0		AM27	DQ3B8	DQ1B24
B8	VREF0B8	IO			AG24		
B8	VREF0B8	IO	DQ8B7		AJ26	DQ3B7	DQ1B23
B8	VREF0B8	IO			AF24		
B8	VREF0B8	IO	DQ8B6		AK26	DQ3B6	DQ1B22
B8	VREF0B8	IO			AH24		
B8	VREF0B8	IO	DQ8B5		AL26	DQ3B5	DQ1B21
B8	VREF0B8	IO			AB22		
B8	VREF0B8	IO	DQ8B4		AH25	DQ3B4	DQ1B20
B8	VREF0B8	IO	DQ8B3		AM26	DQ3B3	DQ1B19
B8	VREF0B8	IO			AG23		
B8	VREF1B8	IO	DQS8B		AJ25	DQS3B	
B8	VREF1B8	IO	DQ8B0		AM25	DQ3B0	DQ1B16
B8	VREF1B8	IO	DQ8B2		AK25	DQ3B2	DQ1B18
B8	VREF1B8	IO			AE23		
B8	VREF1B8	IO	DQ8B1		AL25	DQ3B1	DQ1B17
B8	VREF1B8	IO			AF23		
B8	VREF1B8	IO			AC22		
B8	VREF1B8	IO	DQ7B7		AJ24	DQ2B15	DQ1B15

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Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B8	VREF1B8	IO			AG22		
B8	VREF1B8	IO	DQ7B6		AK24	DQ2B14	DQ1B14
B8	VREF1B8	VREF1B8			AA21		
B8	VREF1B8	IO	DQ7B5		AL24	DQ2B13	DQ1B13
B8	VREF1B8	IO			AD22		
B8	VREF1B8	IO	DQ7B4		AM24	DQ2B12	DQ1B12
B8	VREF1B8	IO			AG21		
B8	VREF1B8	IO	DQ7B3		AH23	DQ2B11	DQ1B11
B8	VREF1B8	IO	DQS7B		AJ23		DQS1B
B8	VREF1B8	IO	DQ7B2		AK23	DQ2B10	DQ1B10
B8	VREF1B8	IO	DQ7B1		AL23	DQ2B9	DQ1B9
B8	VREF1B8	IO	DQ7B0		AM23	DQ2B8	DQ1B8
B8	VREF1B8	IO	FCLK3		AE22		
B8	VREF1B8	IO	FCLK2		AF22		
B8	VREF2B8	IO	DQ6B7		AH22	DQ2B7	DQ1B7
B8	VREF2B8	IO	DQ6B6		AL22	DQ2B6	DQ1B6
B8	VREF2B8	IO	DQ6B5		AJ22	DQ2B5	DQ1B5
B8	VREF2B8	IO	DQ6B4		AK22	DQ2B4	DQ1B4
B8	VREF2B8	IO		PGM2	AF21		
B8	VREF2B8	IO	DQ6B3		AM22	DQ2B3	DQ1B3
B8	VREF2B8	IO	DQS6B		AL21	DQS2B	
B8	VREF2B8	IO	DQ6B2		AM21	DQ2B2	DQ1B2
B8	VREF2B8	IO		CRC_ERROR	AE21		
B8	VREF2B8	VREF2B8			AA20		
B8	VREF2B8	IO	DQ6B1		AJ21	DQ2B1	DQ1B1
B8	VREF2B8	IO	DQ6B0		AK21	DQ2B0	DQ1B0
B8	VREF2B8	IO	RDN8		AD21		
B8	VREF2B8	IO	RUP8		AF20		
B8	VREF2B8	IO	DQ5B7		AH21		
B8	VREF2B8	IO	DQ5B6		AJ20		
B8	VREF2B8	IO	DQ5B5		AK20		
B8	VREF2B8	IO	DQ5B4		AL20		
B8	VREF2B8	IO		RDYnBSY	AC21		
B8	VREF2B8	IO	DQ5B3		AJ19		
B8	VREF2B8	IO	DQS5B		AG20		
B8	VREF2B8	IO	DQ5B2		AH20		
B8	VREF3B8	IO		nCS	AB21		
B8	VREF3B8	IO	DQ5B1		AG19		
B8	VREF3B8	IO	DQ5B0		AH19		
B8	VREF3B8	IO		CS	AE20		
B8	VREF3B8	VREF3B8			AA19		
B8	VREF3B8	IO	CLK5n		AL19		
B8	VREF3B8	CLK5p			AK19		
B8	VREF3B8	IO	CLK4n		AM18		
B8	VREF3B8	CLK4p			AL18		
B8	VREF3B8	PLL_ENA		PLL_ENA	AC20		
B8	VREF3B8	MSEL0		MSEL0	AD20		
B8	VREF3B8	MSEL1		MSEL1	AB20		
B8	VREF3B8	MSEL2		MSEL2	AB19		
B12	VREF3B8	IO	PLL6_OUT3n		AH18		
B12	VREF3B8	IO	PLL6_OUT3p		AG18		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B12	VREF3B8	IO	PLL6_OUT2n		AK18		
B12	VREF3B8	IO	PLL6_OUT2p		AJ18		
B11	VREF3B8	IO	PLL6_FBn		AH17		
B11	VREF3B8	IO	PLL6_FBp		AG17		
B11	VREF3B8	IO	PLL6_OUT1n		AK17		
B11	VREF3B8	IO	PLL6_OUT1p		AJ17		
B11	VREF3B8	IO	PLL6_OUT0n		AM17		
B11	VREF3B8	IO	PLL6_OUT0p		AL17		
B12		VCC_PLL6_OUTB			AA18		
B11		VCC_PLL6_OUTA			AB18		
		VCCA_PLL6			AC18		
		GND					
		GNDA_PLL6			AB17		
		VCCG_PLL6			AC17		
		GNDG_PLL6			AA17		
		VCCA_PLL12			AC16		
		GND					
		GNDA_PLL12			AB16		
		VCCG_PLL12			AD17		
		GNDG_PLL12			AA16		
B7	VREF0B7	CLK7p			AG16		
B7	VREF0B7	IO	CLK7n		AH16		
B7	VREF0B7	CLK6p			AJ16		
B7	VREF0B7	IO	CLK6n/PLL12_OUT		AK16		
B7	VREF0B7	nCE		nCE	AD16		
B7	VREF0B7	nCEO		nCEO	AE16		
B7	VREF0B7	IO		PGM0	AD18		
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	AB15		
B7	VREF0B7	VCCSEL		VCCSEL	AA15		
B7	VREF0B7	PORSEL		PORSEL	AC15		
B7	VREF0B7	VREF0B7			Y16		
B7	VREF0B7	IO		INIT_DONE	AD19		
B7	VREF0B7	IO			AC19		
B7	VREF0B7	IO	DQ4B7		AG15		
B7	VREF0B7	IO			AE19		
B7	VREF0B7	IO	DQ4B6		AJ15		
B7	VREF0B7	IO		nRS	AE17		
B7	VREF0B7	IO	DQ4B5		AH15		
B7	VREF0B7	IO			Y18		
B7	VREF0B7	IO	DQ4B4		AK15		
B7	VREF0B7	IO			AD15		
B7	VREF0B7	IO	DQ4B3		AL15		
B7	VREF0B7	IO		RUnLU	AF18		
B7	VREF1B7	IO	DQS4B		AL14		
B7	VREF1B7	IO			Y17		
B7	VREF1B7	IO	DQ4B2		AM14		
B7	VREF1B7	IO			AE18		
B7	VREF1B7	IO	DQ4B1		AM15		
B7	VREF1B7	IO		PGM1	AF17		
B7	VREF1B7	IO	DQ4B0		AK14		
B7	VREF1B7	IO	RDN7		AC14		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B7	VREF1B7	IO	RUP7		AF19		
B7	VREF1B7	IO	DQ3B7		AG14	DQ1B15	DQ0B31
B7	VREF1B7	IO			AE15		
B7	VREF1B7	IO	DQ3B6		AH14	DQ1B14	DQ0B30
B7	VREF1B7	IO			AB14		
B7	VREF1B7	IO	DQ3B5		AL13	DQ1B13	DQ0B29
B7	VREF1B7	IO	DEV_CLRn		AD14		
B7	VREF1B7	IO	DQ3B4		AM13	DQ1B12	DQ0B28
B7	VREF1B7	IO			AF16		
B7	VREF1B7	IO	DQ3B3		AJ14	DQ1B11	DQ0B27
B7	VREF1B7	VREF1B7			Y15		
B7	VREF1B7	IO			Y14		
B7	VREF1B7	IO	DQS3B		AH13	DQS1B	
B7	VREF1B7	IO			AA14		
B7	VREF1B7	IO	DQ3B2		AJ13	DQ1B10	DQ0B26
B7	VREF1B7	IO			AE14		
B7	VREF1B7	IO	DQ3B1		AK13	DQ1B9	DQ0B25
B7	VREF1B7	IO			V14		
B7	VREF1B7	IO	DQ3B0		AG13	DQ1B8	DQ0B24
B7	VREF1B7	IO			W14		
B7	VREF1B7	IO	FCLK5		AF15		
B7	VREF1B7	IO	FCLK4		U14		
B7	VREF2B7	IO	DQ2B7		AD13	DQ1B7	DQ0B23
B7	VREF2B7	IO	DQ2B6		AC13	DQ1B6	DQ0B22
B7	VREF2B7	IO	DQ2B5		AE13	DQ1B5	DQ0B21
B7	VREF2B7	IO			W13		
B7	VREF2B7	IO	DQ2B4		AF13	DQ1B4	DQ0B20
B7	VREF2B7	IO			AA13		
B7	VREF2B7	IO	DQ2B3		AB13	DQ1B3	DQ0B19
B7	VREF2B7	IO			V13		
B7	VREF2B7	IO	DQS2B		AE12		DQS0B
B7	VREF2B7	IO			U13		
B7	VREF2B7	IO	DQ2B2		AF12	DQ1B2	DQ0B18
B7	VREF2B7	IO			W12		
B7	VREF2B7	IO	DQ2B1		AC12	DQ1B1	DQ0B17
B7	VREF2B7	IO			AA12		
B7	VREF2B7	IO	DQ2B0		AD12	DQ1B0	DQ0B16
B7	VREF2B7	IO			AF14		
B7	VREF2B7	IO			W11		
B7	VREF2B7	VREF2B7			Y13		
B7	VREF2B7	IO			V11		
B7	VREF2B7	IO	DQ1B6		AB11	DQ0B14	DQ0B14
B7	VREF2B7	IO			V12		
B7	VREF2B7	IO	DQ1B5		AB12	DQ0B13	DQ0B13
B7	VREF2B7	IO	DQ1B7		AF11	DQ0B15	DQ0B15
B7	VREF2B7	IO	DQ1B4		AE11	DQ0B12	DQ0B12
B7	VREF2B7	IO			Y11		
B7	VREF2B7	IO	DQ1B3		AC11	DQ0B11	DQ0B11
B7	VREF2B7	IO			AA11		
B7	VREF2B7	IO	DQS1B		AD11	DQS0B	
B7	VREF2B7	IO			V10		

Pin Information For The Stratix™ GX EP1SGX40G Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B7	VREF2B7	IO	DQ1B2		AE10	DQ0B10	DQ0B10
B7	VREF3B7	IO			W10		
B7	VREF3B7	IO	DQ1B1		AC10	DQ0B9	DQ0B9
B7	VREF3B7	IO			Y10		
B7	VREF3B7	IO	DQ1B0		AD10	DQ0B8	DQ0B8
B7	VREF3B7	IO			AD7		
B7	VREF3B7	IO	DQ0B7		AC9	DQ0B7	DQ0B7
B7	VREF3B7	IO			AA10		
B7	VREF3B7	IO	DQ0B6		AF8	DQ0B6	DQ0B6
B7	VREF3B7	IO			AB10		
B7	VREF3B7	IO	DQ0B5		AF10	DQ0B5	DQ0B5
B7	VREF3B7	VREF3B7			Y12		
B7	VREF3B7	IO	DQ0B4		AC8	DQ0B4	DQ0B4
B7	VREF3B7	IO	DQ0B3		AE8	DQ0B3	DQ0B3
B7	VREF3B7	IO	DQS0B		AF9		
B7	VREF3B7	IO	DQ0B2		AD8	DQ0B2	DQ0B2
B7	VREF3B7	IO	DQ0B1		AD9	DQ0B1	DQ0B1
B7	VREF3B7	IO	DQ0B0		AE9	DQ0B0	DQ0B0
B16		GXB_RX15n			AL11		
B16		GXB_RX15p			AM11		
B16		GXB_TX15n			AH11		
B16		GXB_TX15p			AJ11		
B16		GXB_RX14n			AL9		
B16		GXB_RX14p			AM9		
B16		GXB_TX14n			AH9		
B16		GXB_TX14p			AJ9		
B16		VCCA_B16			AD6		
B16		REFCLKB16n			AL7		
B16		REFCLKB16p			AM7		
		VCCG_B16			AC6		
		GND			AB6		
B16		RREFB16			AC7		
B16		GXB_RX12n			AL5		
B16		GXB_RX12p			AM5		
B16		GXB_TX12n			AH7		
B16		GXB_TX12p			AJ7		
B16		GXB_RX13n			AM3		
B16		GXB_RX13p			AM2		
B16		GXB_TX13n			AJ5		
B16		GXB_TX13p			AJ4		
B15		GXB_RX11n			AK2		
B15		GXB_RX11p			AK1		
B15		GXB_TX11n			AG5		
B15		GXB_TX11p			AG4		
B15		GXB_RX10n			AH2		
B15		GXB_RX10p			AH1		
B15		GXB_TX10n			AE5		
B15		GXB_TX10p			AE4		
B15		VCCA_B15			AA6		
B15		REFCLKB15n			AF2		
B15		REFCLKB15p			AF1		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		VCCG_B15			W6		
		GND			Y6		
B15		RREFB15			T8		
B15		GXB_RX8n			AD2		
B15		GXB_RX8p			AD1		
B15		GXB_TX8n			AC5		
B15		GXB_TX8p			AC4		
B15		GXB_RX9n			AB2		
B15		GXB_RX9p			AB1		
B15		GXB_TX9n			AA5		
B15		GXB_TX9p			AA4		
B17		GXB_RX19n			Y2		
B17		GXB_RX19p			Y1		
B17		GXB_TX19n			W5		
B17		GXB_TX19p			W4		
B17		GXB_RX18n			V2		
B17		GXB_RX18p			V1		
B17		GXB_TX18n			U5		
B17		GXB_TX18p			U4		
B17		VCCA_B17			V6		
B17		REFCLKB17n			T2		
B17		REFCLKB17p			T1		
		VCCG_B17			T6		
		GND			U6		
B17		RREFB17			T7		
B17		GXB_RX16n			P2		
B17		GXB_RX16p			P1		
B17		GXB_TX16n			R5		
B17		GXB_TX16p			R4		
B17		GXB_RX17n			M2		
B17		GXB_RX17p			M1		
B17		GXB_TX17n			N5		
B17		GXB_TX17p			N4		
B14		GXB_RX7n			K2		
B14		GXB_RX7p			K1		
B14		GXB_TX7n			L5		
B14		GXB_TX7p			L4		
B14		GXB_RX6n			H2		
B14		GXB_RX6p			H1		
B14		GXB_TX6n			J5		
B14		GXB_TX6p			J4		
B14		VCCA_B14			R6		
B14		REFCLKB14n			F2		
B14		REFCLKB14p			F1		
		VCCG_B14			N6		
		GND			P6		
B14		RREFB14			L7		
B14		GXB_RX4n			D2		
B14		GXB_RX4p			D1		
B14		GXB_TX4n			G5		
B14		GXB_TX4p			G4		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B14		GXB_RX5n			B2		
B14		GXB_RX5p			B1		
B14		GXB_TX5n			E4		
B14		GXB_TX5p			D4		
B13		GXB_RX3n			B4		
B13		GXB_RX3p			A4		
B13		GXB_TX3n			E6		
B13		GXB_TX3p			D6		
B13		GXB_RX2n			B6		
B13		GXB_RX2p			A6		
B13		GXB_TX2n			E8		
B13		GXB_TX2p			D8		
B13		VCCA_B13			M6		
B13		REFCLKB13n			B8		
B13		REFCLKB13p			A8		
		VCCG_B13			K6		
		GND			L6		
B13		RREFB13			J7		
B13		GXB_RX0n			B10		
B13		GXB_RX0p			A10		
B13		GXB_TX0n			E10		
B13		GXB_TX0p			D10		
B13		GXB_RX1n			B12		
B13		GXB_RX1p			A12		
B13		GXB_TX1n			E12		
B13		GXB_TX1p			D12		
B4	VREF0B4	IO	DQ0T0		H9	DQ0T0	DQ0T0
B4	VREF0B4	IO	DQ0T1		J8	DQ0T1	DQ0T1
B4	VREF0B4	IO	DQ0T2		K8	DQ0T2	DQ0T2
B4	VREF0B4	IO	DQS0T		G8		
B4	VREF0B4	IO	DQ0T3		J9	DQ0T3	DQ0T3
B4	VREF0B4	IO	DQ0T4		K9	DQ0T4	DQ0T4
B4	VREF0B4	VREF0B4			N12		
B4	VREF0B4	IO	DQ0T5		G9	DQ0T5	DQ0T5
B4	VREF0B4	IO			K7		
B4	VREF0B4	IO	DQ0T6		H8	DQ0T6	DQ0T6
B4	VREF0B4	IO			L8		
B4	VREF0B4	IO	DQ0T7		L9	DQ0T7	DQ0T7
B4	VREF0B4	IO			H7		
B4	VREF0B4	IO	DQ1T0		J10	DQ0T8	DQ0T8
B4	VREF0B4	IO			L10		
B4	VREF0B4	IO	DQ1T1		K10	DQ0T9	DQ0T9
B4	VREF0B4	IO			M10		
B4	VREF1B4	IO	DQ1T2		G10	DQ0T10	DQ0T10
B4	VREF1B4	IO			N10		
B4	VREF1B4	IO	DQS1T		H10	DQS0T	
B4	VREF1B4	IO			P10		
B4	VREF1B4	IO	DQ1T3		K11	DQ0T11	DQ0T11
B4	VREF1B4	IO			R10		
B4	VREF1B4	IO	DQ1T4		H11	DQ0T12	DQ0T12
B4	VREF1B4	IO	DQ1T7		G11	DQ0T15	DQ0T15

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B4	VREF1B4	IO	DQ1T5		J11	DQ0T13	DQ0T13
B4	VREF1B4	IO			N11		
B4	VREF1B4	IO	DQ1T6		L11	DQ0T14	DQ0T14
B4	VREF1B4	IO			P11		
B4	VREF1B4	VREF1B4			N13		
B4	VREF1B4	IO			M11		
B4	VREF1B4	IO			R11		
B4	VREF1B4	IO	DQ2T0		J12	DQ1T0	DQ0T16
B4	VREF1B4	IO			M12		
B4	VREF1B4	IO	DQ2T1		K12	DQ1T1	DQ0T17
B4	VREF1B4	IO			P12		
B4	VREF1B4	IO	DQ2T2		G12	DQ1T2	DQ0T18
B4	VREF1B4	IO			R12		
B4	VREF1B4	IO	DQS2T		H12		DQS0T
B4	VREF1B4	IO			T12		
B4	VREF1B4	IO	DQ2T3		L12	DQ1T3	DQ0T19
B4	VREF1B4	IO			U12		
B4	VREF1B4	IO	DQ2T4		H13	DQ1T4	DQ0T20
B4	VREF1B4	IO			R13		
B4	VREF1B4	IO	DQ2T5		J13	DQ1T5	DQ0T21
B4	VREF1B4	IO	DQ2T6		L13	DQ1T6	DQ0T22
B4	VREF1B4	IO	DQ2T7		K13	DQ1T7	DQ0T23
B4	VREF2B4	IO	FCLK6		M13		
B4	VREF2B4	IO	FCLK7		T14		
B4	VREF2B4	IO			P13		
B4	VREF2B4	IO	DQ3T0		G13	DQ1T8	DQ0T24
B4	VREF2B4	IO			T13		
B4	VREF2B4	IO	DQ3T1		D14	DQ1T9	DQ0T25
B4	VREF2B4	IO			N14		
B4	VREF2B4	IO	DQ3T2		F14	DQ1T10	DQ0T26
B4	VREF2B4	IO			P14		
B4	VREF2B4	IO	DQS3T		G14	DQS1T	
B4	VREF2B4	IO			R14		
B4	VREF2B4	VREF2B4			N15		
B4	VREF2B4	IO	DQ3T3		E14	DQ1T11	DQ0T27
B4	VREF2B4	IO			G17		
B4	VREF2B4	IO	DQ3T4		H14	DQ1T12	DQ0T28
B4	VREF2B4	IO			L14		
B4	VREF2B4	IO	DQ3T5		J14	DQ1T13	DQ0T29
B4	VREF2B4	IO	DEV_OE		M14		
B4	VREF2B4	IO	DQ3T6		G15	DQ1T14	DQ0T30
B4	VREF2B4	IO			G18		
B4	VREF2B4	IO	DQ3T7		H15	DQ1T15	DQ0T31
B4	VREF2B4	IO	RUP4		H19		
B4	VREF2B4	IO	RDN4		K14		
B4	VREF2B4	IO	DQ4T0		C14		
B4	VREF2B4	IO		nWS	G19		
B4	VREF2B4	IO	DQ4T1		A15		
B4	VREF2B4	IO			L15		
B4	VREF2B4	IO	DQ4T2		A14		
B4	VREF2B4	IO			M15		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B4	VREF2B4	IO	DQS4T		B14		
B4	VREF3B4	IO		DATA0	H17		
B4	VREF3B4	IO	DQ4T3		B15		
B4	VREF3B4	IO			K19		
B4	VREF3B4	IO	DQ4T4		C15		
B4	VREF3B4	IO			N17		
B4	VREF3B4	IO	DQ4T5		F15		
B4	VREF3B4	IO		DATA1	H18		
B4	VREF3B4	IO	DQ4T6		D15		
B4	VREF3B4	IO			J18		
B4	VREF3B4	IO	DQ4T7		E15		
B4	VREF3B4	IO			N18		
B4	VREF3B4	IO		DATA2	L19		
B4	VREF3B4	VREF3B4			N16		
B4	VREF3B4	TMS		TMS	G16		
B4	VREF3B4	TRST		TRST	J15		
B4	VREF3B4	TCK		TCK	K15		
B4	VREF3B4	IO		DATA3	J19		
B4	VREF3B4	TDI		TDI	H16		
B4	VREF3B4	TDO		TDO	J16		
B4	VREF3B4	IO	CLK12n		C16		
B4	VREF3B4	CLK12p			D16		
B4	VREF3B4	IO	CLK13n/PLL11_OUT		E16		
B4	VREF3B4	CLK13p			F16		
		VCCA_PLL11			K16		
		GND					
		GNDA_PLL11			L16		
		VCCG_PLL11			J17		
		GNDG_PLL11			M16		
		TEMPDIODEp			L21		
		TEMPDIODEn			L20		
		VCCA_PLL5			L18		
		GND					
		GNDA_PLL5			L17		
		VCCG_PLL5			K17		
		GNDG_PLL5			M17		
B9		VCC_PLL5_OUTA			K18		
B10		VCC_PLL5_OUTB			M18		
B9	VREF0B3	IO	PLL5_OUT0p		F18		
B9	VREF0B3	IO	PLL5_OUT0n		E18		
B9	VREF0B3	IO	PLL5_OUT1p		D17		
B9	VREF0B3	IO	PLL5_OUT1n		C17		
B9	VREF0B3	IO	PLL5_FBp		F17		
B9	VREF0B3	IO	PLL5_FBn		E17		
B10	VREF0B3	IO	PLL5_OUT2p		B17		
B10	VREF0B3	IO	PLL5_OUT2n		A17		
B10	VREF0B3	IO	PLL5_OUT3p		D18		
B10	VREF0B3	IO	PLL5_OUT3n		C18		
B3	VREF0B3	nSTATUS		nSTATUS	L22		
B3	VREF0B3	nCONFIG		nCONFIG	K20		
B3	VREF0B3	DCLK		DCLK	J20		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B3	VREF0B3	CONF_DONE		CONF_DONE	K21		
B3	VREF0B3	CLK14p			B18		
B3	VREF0B3	IO	CLK14n		A18		
B3	VREF0B3	CLK15p			C19		
B3	VREF0B3	IO	CLK15n		B19		
B3	VREF0B3	VREF0B3			M19		
B3	VREF0B3	IO		DATA4	G20		
B3	VREF0B3	IO	DQ5T0		E19		
B3	VREF0B3	IO	DQ5T1		F19		
B3	VREF0B3	IO		DATA5	H20		
B3	VREF1B3	IO	DQ5T2		E20		
B3	VREF1B3	IO	DQS5T		F20		
B3	VREF1B3	IO	DQ5T3		D19		
B3	VREF1B3	IO		DATA6	J21		
B3	VREF1B3	IO	DQ5T4		B20		
B3	VREF1B3	IO	DQ5T5		C20		
B3	VREF1B3	IO	DQ5T6		D20		
B3	VREF1B3	IO	DQ5T7		E21		
B3	VREF1B3	IO	RUP3		H21		
B3	VREF1B3	IO	RDN3		G21		
B3	VREF1B3	IO	DQ6T0		C21	DQ2T0	DQ1T0
B3	VREF1B3	IO	DQ6T1		D21	DQ2T1	DQ1T1
B3	VREF1B3	VREF1B3			M20		
B3	VREF1B3	IO		DATA7	F21		
B3	VREF1B3	IO	DQ6T2		A21	DQ2T2	DQ1T2
B3	VREF1B3	IO	DQS6T		B21	DQS2T	
B3	VREF1B3	IO	DQ6T3		A22	DQ2T3	DQ1T3
B3	VREF1B3	IO		CLKUSR	F22		
B3	VREF1B3	IO	DQ6T4		C22	DQ2T4	DQ1T4
B3	VREF1B3	IO	DQ6T5		D22	DQ2T5	DQ1T5
B3	VREF1B3	IO	DQ6T6		B22	DQ2T6	DQ1T6
B3	VREF1B3	IO	DQ6T7		E22	DQ2T7	DQ1T7
B3	VREF2B3	IO	FCLK0		G22		
B3	VREF2B3	IO	FCLK1		H22		
B3	VREF2B3	IO			J22		
B3	VREF2B3	IO	DQ7T0		A23	DQ2T8	DQ1T8
B3	VREF2B3	IO	DQ7T1		B23	DQ2T9	DQ1T9
B3	VREF2B3	IO	DQ7T2		C23	DQ2T10	DQ1T10
B3	VREF2B3	IO	DQS7T		D23		DQS1T
B3	VREF2B3	IO	DQ7T3		E23	DQ2T11	DQ1T11
B3	VREF2B3	IO			F23		
B3	VREF2B3	IO	DQ7T4		A24	DQ2T12	DQ1T12
B3	VREF2B3	IO			G23		
B3	VREF2B3	IO	DQ7T5		B24	DQ2T13	DQ1T13
B3	VREF2B3	VREF2B3			M21		
B3	VREF2B3	IO	DQ7T6		C24	DQ2T14	DQ1T14
B3	VREF2B3	IO	DQ7T7		D24	DQ2T15	DQ1T15
B3	VREF2B3	IO			H23		
B3	VREF2B3	IO			F24		
B3	VREF2B3	IO	DQ8T1		B25	DQ3T1	DQ1T17
B3	VREF2B3	IO			E24		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
B3	VREF2B3	IO	DQ8T2		C25	DQ3T2	DQ1T18
B3	VREF2B3	IO	DQ8T0		A25	DQ3T0	DQ1T16
B3	VREF2B3	IO	DQS8T		D25	DQS3T	
B3		GND			K22		
B3	VREF3B3	IO			G24		
B3	VREF3B3	IO	DQ8T3		A26	DQ3T3	DQ1T19
B3	VREF3B3	IO			F25		
B3	VREF3B3	IO	DQ8T4		E25	DQ3T4	DQ1T20
B3	VREF3B3	IO			E26		
B3	VREF3B3	IO	DQ8T5		B26	DQ3T5	DQ1T21
B3	VREF3B3	IO	DQ8T6		C26	DQ3T6	DQ1T22
B3	VREF3B3	IO			D27		
B3	VREF3B3	IO	DQ8T7		D26	DQ3T7	DQ1T23
B3	VREF3B3	IO			F26		
B3	VREF3B3	IO	DQ9T0		A27	DQ3T8	DQ1T24
B3	VREF3B3	IO	DQ9T1		B27	DQ3T9	DQ1T25
B3	VREF3B3	IO			E27		
B3	VREF3B3	IO	DQ9T2		C27	DQ3T10	DQ1T26
B3	VREF3B3	IO			B30		
B3	VREF3B3	VREF3B3			M22		
B3	VREF3B3	IO	DQS9T		A28		
B3	VREF3B3	IO			D28		
B3	VREF3B3	IO	DQ9T3		B28	DQ3T11	DQ1T27
B3	VREF3B3	IO			E28		
B3	VREF3B3	IO	DQ9T4		C28	DQ3T12	DQ1T28
B3	VREF3B3	IO			B31		
B3	VREF3B3	IO	DQ9T5		A29	DQ3T13	DQ1T29
B3	VREF3B3	IO	DQ9T6		B29	DQ3T14	DQ1T30
B3	VREF3B3	IO			C30		
B3	VREF3B3	IO	DQ9T7		C29	DQ3T15	DQ1T31
B3	VREF3B3	IO			C31		
		GXB_GND					
		GND					
		VCCIO2			C32		
		VCCIO2			N23		
		VCCIO2			R32		
		VCCIO2			T24		
		VCCIO1			AK32		
		VCCIO1			V32		
		VCCIO1			U23		
		VCCIO1			Y23		
		VCCIO8			AM19		
		VCCIO8			Y19		
		VCCIO8			AM30		
		VCCIO8			Y21		
		VCCIO7			AF7		
		VCCIO7			AM16		
		VCCIO7			AM12		
		VCCIO7			U11		
		VCCIO4			A13		
		VCCIO4			A16		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		VCCIO4			G7		
		VCCIO4			T11		
		VCCIO3			A19		
		VCCIO3			A30		
		VCCIO3			N19		
		VCCIO3			N21		
		VCCP_B13			M9		
		VCCP_B13			N9		
		VCCP_B14			P9		
		VCCP_B14			R9		
		VCCP_B15			W9		
		VCCP_B15			Y9		
		VCCP_B16			AA9		
		VCCP_B16			AB9		
		VCCP_B17			U9		
		VCCP_B17			V9		
		VCCR_B13			M8		
		VCCR_B13			N8		
		VCCR_B14			P8		
		VCCR_B14			R8		
		VCCR_B15			W8		
		VCCR_B15			Y8		
		VCCR_B16			AA8		
		VCCR_B16			AB8		
		VCCR_B17			U8		
		VCCR_B17			V8		
		VCCT_B13			M7		
		VCCT_B13			N7		
		VCCT_B14			P7		
		VCCT_B14			R7		
		VCCT_B15			W7		
		VCCT_B15			Y7		
		VCCT_B16			AA7		
		VCCT_B16			AB7		
		VCCT_B17			U7		
		VCCT_B17			V7		
		VCCINT			R15		
		VCCINT			P19		
		VCCINT			U15		
		VCCINT			V15		
		VCCINT			W22		
		VCCINT			AG12		
		VCCINT			P22		
		VCCINT			T17		
		VCCINT			V21		
		VCCINT			P15		
		VCCINT			R21		
		VCCINT			U18		
		VCCINT			W20		
		VCCINT			F11		
		VCCINT			R18		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		VCCINT			T21		
		VCCINT			W16		
		VCCINT			AG10		
		VCCINT			P21		
		VCCINT			T15		
		VCCINT			V19		
		VCCINT			F13		
		VCCINT			R20		
		VCCINT			U16		
		VCCINT			W18		
		VCCINT			W15		
		VCCINT			P20		
		VCCINT			T9		
		VCCINT			V17		
		VCCINT			U21		
		VCCINT			F9		
		VCCINT			R16		
		VCCINT			T19		
		VCCINT			V22		
		VCCINT			P17		
		VCCINT			R22		
		VCCINT			U20		
		VCCINT			W21		
		GXB_GND			A2		
		GXB_GND			AB4		
		GXB_GND			AE2		
		GXB_GND			AH3		
		GXB_GND			AJ6		
		GXB_GND			AK9		
		GXB_GND			AL10		
		GXB_GND			C1		
		GXB_GND			C12		
		GXB_GND			E9		
		GXB_GND			H4		
		GXB_GND			L2		
		GXB_GND			R1		
		GXB_GND			V5		
		GXB_GND			A11		
		GXB_GND			AD3		
		GXB_GND			AF5		
		GXB_GND			AH10		
		GXB_GND			AK5		
		GXB_GND			AL3		
		GXB_GND			B3		
		GXB_GND			C6		
		GXB_GND			D11		
		GXB_GND			F6		
		GXB_GND			J3		
		GXB_GND			N1		
		GXB_GND			T5		
		GXB_GND			Y4		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		GXB_GND			A7		
		GXB_GND			AC2		
		GXB_GND			AF3		
		GXB_GND			AH6		
		GXB_GND			AK3		
		GXB_GND			AL1		
		GXB_GND			AM8		
		GXB_GND			C4		
		GXB_GND			D7		
		GXB_GND			F4		
		GXB_GND			J1		
		GXB_GND			M4		
		GXB_GND			T3		
		GXB_GND			W3		
		GXB_GND			AA3		
		GXB_GND			AE1		
		GXB_GND			AG3		
		GXB_GND			AJ3		
		GXB_GND			AK8		
		GXB_GND			AL8		
		GXB_GND			B9		
		GXB_GND			C9		
		GXB_GND			E3		
		GXB_GND			G3		
		GXB_GND			K4		
		GXB_GND			P3		
		GXB_GND			U3		
		GXB_GND			A5		
		GXB_GND			AC1		
		GXB_GND			AE6		
		GXB_GND			AH5		
		GXB_GND			AJ10		
		GXB_GND			AK11		
		GXB_GND			AM6		
		GXB_GND			C3		
		GXB_GND			D5		
		GXB_GND			F3		
		GXB_GND			H6		
		GXB_GND			M3		
		GXB_GND			R3		
		GXB_GND			W2		
		GXB_GND			AA2		
		GXB_GND			AD5		
		GXB_GND			AG2		
		GXB_GND			AJ2		
		GXB_GND			AK7		
		GXB_GND			AL6		
		GXB_GND			B7		
		GXB_GND			C8		
		GXB_GND			E2		
		GXB_GND			G2		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		GXB_GND			K3		
		GXB_GND			N3		
		GXB_GND			U2		
		GXB_GND			V4		
		GXB_GND			A3		
		GXB_GND			AB5		
		GXB_GND			AE3		
		GXB_GND			AH4		
		GXB_GND			AJ8		
		GXB_GND			AK10		
		GXB_GND			AM4		
		GXB_GND			C2		
		GXB_GND			D3		
		GXB_GND			E11		
		GXB_GND			H5		
		GXB_GND			L3		
		GXB_GND			R2		
		GXB_GND			W1		
		GXB_GND			AA1		
		GXB_GND			AD4		
		GXB_GND			AG1		
		GXB_GND			AJ1		
		GXB_GND			AK6		
		GXB_GND			AL4		
		GXB_GND			B5		
		GXB_GND			C7		
		GXB_GND			E1		
		GXB_GND			G1		
		GXB_GND			J6		
		GXB_GND			N2		
		GXB_GND			U1		
		GXB_GND			Y5		
		GXB_GND			A9		
		GXB_GND			AC3		
		GXB_GND			AF4		
		GXB_GND			AH8		
		GXB_GND			AK4		
		GXB_GND			AL2		
		GXB_GND			AM10		
		GXB_GND			C5		
		GXB_GND			D9		
		GXB_GND			F5		
		GXB_GND			J2		
		GXB_GND			M5		
		GXB_GND			T4		
		GXB_GND			Y3		
		GXB_GND			AB3		
		GXB_GND			B11		
		GXB_GND			C10		
		GXB_GND			E5		
		GXB_GND			G6		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		GXB_GND			K5		
		GXB_GND			P4		
		GXB_GND			V3		
		GXB_GND			C11		
		GXB_GND			E7		
		GXB_GND			H3		
		GXB_GND			L1		
		GXB_GND			P5		
		GND			A20		
		GND			AL12		
		GND			D13		
		GND			P18		
		GND			T22		
		GND			AG8		
		GND			AG9		
		GND			AM31		
		GND			F10		
		GND			R19		
		GND			U19		
		GND			Y20		
		GND			AG6		
		GND			AL32		
		GND			F7		
		GND			AF6		
		GND			AE7		
		GND			W19		
		GND			AH12		
		GND			B16		
		GND			N20		
		GND			T16		
		GND			V16		
		GND			Y24		
		GND			A31		
		GND			AL16		
		GND			E13		
		GND			P32		
		GND			U10		
		GND			W17		
		GND			AG11		
		GND			B13		
		GND			F12		
		GND			T10		
		GND			U22		
		GND			Y22		
		GND			AG7		
		GND			AM20		
		GND			F8		
		GND			R17		
		GND			U17		
		GND			W32		
		GND			AJ12		

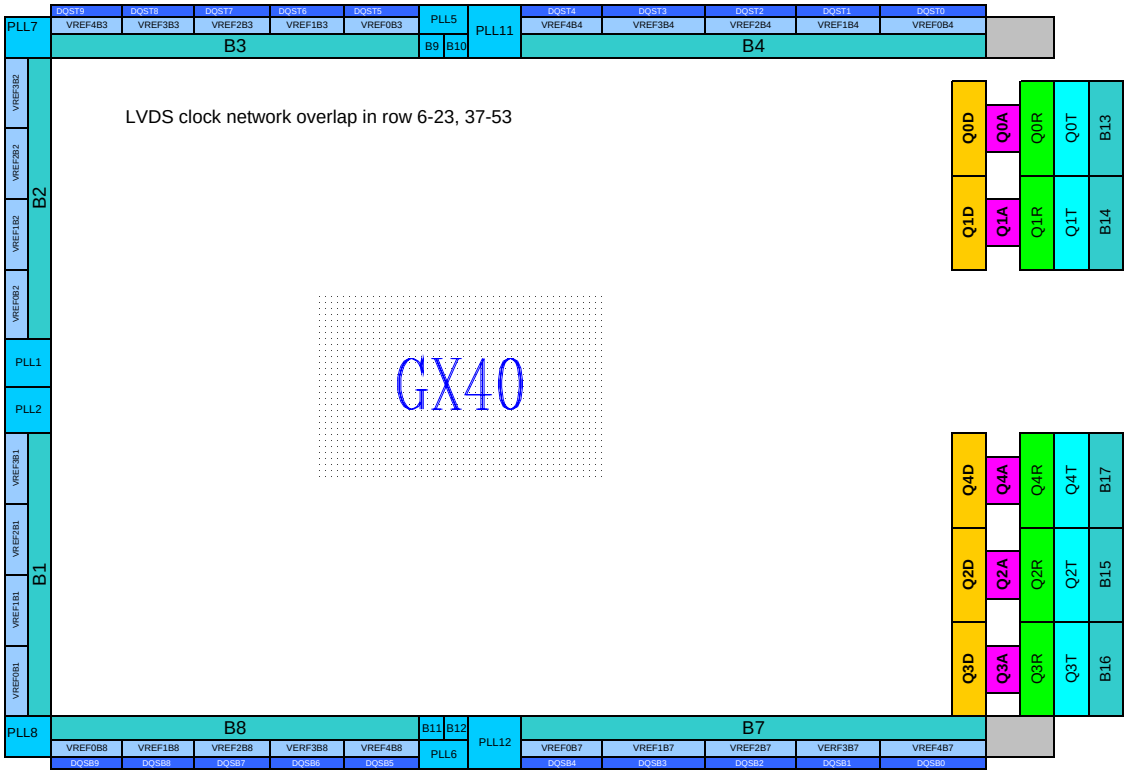
Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F1020	DQS for x16	DQS for x32
		GND			B32		
		GND			N22		
		GND			T18		
		GND			V18		
		GND			P16		
		GND			AK12		
		GND			C13		
		GND			N24		
		GND			T20		
		GND			V20		

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..4,7,8]	Input	Input reference voltage for banks. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, they should be connected to Gnd.
VCCIO[1..4]B[1..4,7,8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These power pins are supplied with a 1.5V source. These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1,2,5,..,8,11,12]	Power	Analog power for PLLs[1,2,5,..,8,11,12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1,2,5,..,8,11,12]	Ground	Analog ground for PLLs[1,2,5,..,8,11,12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1,2,5,..,8,11,12]	Power	Guard ring power for PLLs[1,2,5,..,8,11,12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1,2,5,..,8,11,12]	Ground	Guard ring ground for PLLs[1,2,5,..,8,11,12]. The designer can connect this pin to the GND plane on the board.
GXB_GND	Ground	Transceiver Power Ground. These ground pins need to be connected to a ground island plane isolated from noisy digital ground.
GND	Ground	These ground pins need to be connected to digital ground. The digital ground is used for VCCINT and VCCIO return current.
NC	No Connect	These pins should be left unconnected.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
		Clock and PLL Pins
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Dedicated fast regional clock pins. FCLK pins can also be used as input, output, or bidirectional pins.
CLK[15..12]p	Input	Dedicated global clock inputs 12 to 15.
CLK[15..12]n	I/O, Input	Negative terminal input for differential global clock input. May also be used as regular I/O
CLK[7..0]p	Input	Dedicated global clock inputs 0 to 7.
CLK[7, 6, 5, 4, 3, 1]n	I/O, Input	Negative terminal input for differential global clock input. Or may be used as a regular I/O pin.
CLK[2, 0]n	Input	Dedicated negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	External clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). May also be used as regular I/O
PLL6_OUT[3..0]n	I/O, Output	Negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. May also be used as regular I/O
PLL5_OUT[3..0]p	I/O, Output	External clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). May also be used as regular I/O
PLL5_OUT[3..0]n	I/O, Output	Negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. May also be used as regular I/O
		Optional/Dual-Purpose Pins
DIFFIO_RX[44..0]p	Input	High speed source synchronous differential I/O receiver channels 0 to 44. Pins with an p suffix carry the positive signal for the differential channel If not used, these pins are dedicated input pins.
DIFFIO_RX[44..0]n	Input	This pin is the complementary signal of the differential inputs. If not used for the differential pair, these pins are dedicated input pins. Pins with an n suffix carry the negative signal for the differential channel.
DIFFIO_TX[44..0]p	I/O, Output	Dual-purpose source synchronous high speed differential I/O transmitter channels 0 to 44. Pins with an p suffix carry the positive signal for the differential channel. If not used, these pins are regular I/O pins.
DIFFIO_TX[44..0]n	I/O, Output	This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
DATA[7..0]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..7],RUP[4..1]	I/O, Input	Reference pins for banks 8,7,4,3,2,1 The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..7],RDN[4..1]	I/O, Input	Reference pins for banks 8,7,4,3,2,1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Pin Definitions Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/ O pin.
		GX (I/O banks 13 to 17) Pins
VCCP_B[17..13]	VCC	GX bank [17..13] digital power. This power is connected to 1.5V.
VCCR_B[17..13]	VCC	GX bank [17..13] receiver power. This power is connected to 1.5V.
VCCT_B[17..13]	VCC	GX bank [17..13] transmitter power. This power is connected to 1.5V.
VCCG_B[17..13]	VCC	GX bank[17..13] guard ring power. This power is connected to 1.5V.
VCCA_B[17..13]	VCC	GX bank [17..13] analog power. This power is connected to 3.3V.
GXB_RX[19..0]n	I, Input	High speed differential I/O receiver channels negative. Connect any of these unused pins to ground through a 10K ohm resistor.
GXB_RX[19..0]p	I, Input	High speed differential I/O receiver channels positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
GXB_TX[19..0]n	O,Output	High speed differential I/O transmitter channels negative. Connect any of these unused pins to ground through a 10K ohm resistor.
GXB_TX[19..0]p	O,Output	High speed differential I/O transmitter channels positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
REFCLKB[17..13]n	I, Input	High speed differential I/O reference clock negative. Connect any of these unused pins to ground through a 10K ohm resistor.
REFCLKB[17..13]p	I, Input	High speed differential I/O reference clock positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
RREFB[17..13]	I, Input	Reference resistor for Gx side banks. Should be connected to a 2K of a tolerance of 1% to ground. In the PCB layout the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
RREFB[15,14]A	I, Input	Reference resistor for Gx side banks. Should be connected to a 2K of a tolerance of 1% to ground. In the PCB layout the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Notes:
1.This is a top view of the silicon die.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.



Device Name	GX Bank # Utilized
EP1SGX40D	14 & 15
EP1SGX40G	13,14,15,16,17

Power

Power Description	Flip Chip		Notes
	Global Power on Die	Pkg route	
Left, Top, and Bottom Power and Ground are the same as Stratix Devices			
EPLL clock output power	VCC_CLKOUT[0:7]	isolated	
EPLL clock output power			
EPLL clock output ground	VSSN	VSSN plane	VSSN
EPLL clock output ground	VCCN[4,7]	VCCN[4,7]plane	
EPLL clock output ground	VSSN	VSSN plane	
PLL analog power	VCCA[1:2, 5:8, 11:12]	isolated	VCCA[3:4,9:10]
PLL analog ground	VSSA[1:2, 5:8, 11:12]	isolated	VSSA[3:4,9:10]
PLL digital power	VCC[1:2, 5:8, 11:12]	VCC plane	It is shorted to VCC in the package of the flip chip.
PLL digital ground	VSS[1:2, 5:8, 11:12]	VSS plane	It is shorted to VSS in the package of the flip chip.
PLL guard ring power	VCCG[1:2, 5:8, 11:12]	isolated	
PLL guard ring ground	VSSG[1:2, 5:8, 11:12]	isolated	
Noisy power	VCCN[1:4,7:8]	VCCN[1:4,7:8] plane	
Noisy ground	VSSN	VSS plane	
Quiet power	VCC	VCC plane	
Quiet ground	VSS	VSS plane	
HSSI Global Power: Power and Ground are grouped in QUAD. Quad Order is 0,1,4,2,3			
	Marketing		
HSSI digital power (1.5 v)	VCCP0		Each Quad has 5 bumps connected to 2 isolated digital power balls
	VCCP1		
	VCCP4		
	VCCP2		
	VCCP3		
HSSI RX power (1.5 v)	VCCR[0:3]		Each Quad has 4 bumps connected to 1 isolated RX power ball
	VCCR[4:7]		
	VCCR[16:19]		
	VCCR[8:11]		
	VCCR[12:15]		
HSSI TX power (1.5 v)	VCCT[0:3]		Each Quad has 4 bumps connected to 1 isolated TX power ball
	VCCT[4:7]		
	VCCT[16:19]		
	VCCT[8:11]		
	VCCT[12:15]		
HSSI CMU power (1.5 v)	VCCM0		VCCM# bump shares power with VCCT# of the same QUAD There are no pin associated with this pin name since they share the same bump power with VCCT# of the same Quad
	VCCM1		
	VCCM4		
	VCCM2		
	VCCM3		
HSSI Analog power (3.3 v)	VCCAQ0		Each Quad has its own analog power. One bump--> one ball Provides power to Tx PLL and some biasing circuit
	VCCAQ1		
	VCCAQ4		
	VCCAQ2		
	VCCAQ3		
HSSI VCCG (1.5 v)	VCCGQ0		Each Quad has its own VCCG power. One bump--> one ball Guard ring for TX PLL should be used to isolate noise to TX pll
	VCCGQ1		
	VCCGQ4		
	VCCGQ2		
	VCCGQ3		
HSSI substrate ground	VSSASUB0		Each Quad has its own substrate ground. One bump--> one ball
	VSSASUB1		
	VSSASUB4		
	VSSASUB2		
	VSSASUB3		
HSSI digital ground	DGND		All digital grounds are connected to the HSSI ground plane at package level
	DGND		
	DGND		
	DGND		
	DGND		
HSSI TX/RX ground	HGND		All TX/RX grounds are connected to the HSSI ground plane at package level
	HGND		
	HGND		
	HGND		
	HGND		
HSSI CMU ground	CGND		All CMU grounds are connected to the HSSI ground plane at package level

	CGND		
	CGND		
	CGND		
	CGND		
Global Power on Die is the signal name that the schematics and layout use for this power or ground			
Pkg Route: 1) plane = indicates the power plane the bump/pad routes to in the pkg;			
2) isolated = indicates the bump/pad is routed to the pkg ball without connect to any other pkg route or plane.			
Plane: A plane has multiple bump/pads connected to it which in turn connect to multiple balls. It does not			
necessarily imply a complete sheet of conductor; it may look be more like Swiss cheese.			
Net: Multiple bumps/balls can share the same net bus			

Non-Migratable IO Pins

Non-Migratable IO Pins	
1020FBGA (EP1SGX40 <--> EP1SGX25)	672FBGA (EP1SGX25 <-->EP1SGX10)
AA23	
AB23	
AC23	
AD23	
AG25	
AG26	
AH27	
AH28	
AH29	
AH30	
AJ29	
AJ30	
D29	
D30	
E29	
E30	
F27	
F28	
F29	
F30	
J23	
K23	
L23	
M23	

Device Part Numbers					
Name	Number of Fast PLL	Device Pin Count	# of Receiver Chs	# of Transmitter Chs	Speed (Mbps)
EP1SGX10C	2	672	22	22	1000
EP1SGX10D	2	672	22	22	1000
EP1SGX25C	2	672	39	39	1000
EP1SGX25D	2	672 / 1020	39	39	1000
EP1SGX25F	2	1020	39	39	1000
EP1SGX40D	4	1020	45	45	1000
EP1SGX40G	4	1020	45	45	1000

Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mpbs

Device Part Numbers	I/O Count [1]	
Name	672-Pin FineLine BGA	1,020 Pin FineLine BGA
EP1SGX10C	330	
EP1SGX10D	330	
EP1SGX25C	426	
EP1SGX25D	426	542
EP1SGX25F		542
EP1SGX40D		548
EP1SGX40G		548

Note 1 : The total number of I/O pins for each package described above include dedicated clock pins, and dedicated fast I/O pins. However it does not include High-Speed or the Clock Referance pins for High Speed I/O.

What	Comment	Date
Added voltage value to power pins	rev 1.2	10/15/2002
Added information to the VCCM , they share the same bump with VCCT.	rev 1.3	12/17/2002
Added Non-Migrateble pins	rev 1.3	12/17/2002
Added I/O pin count	rev 1.3	12/17/200
Added info regarding RREF pin	rev 1.3	1/10/2003
Sent to Product Marketing	rev 1.3	2/19/2003
Connected NC pins to RREF pins(NOTE 1)	rev 1.4	5/30/2003
Connected NC pins to VCCx_Bxx (NOTE 1)	rev 1.4	5/30/2003
Connected unused NC pins on the HSSI side to GND. These pins are listed as NC/GND in this document and are listed as GND* in Quartus II software (NOTE 1 and 2)	rev 1.4	5/30/2003
Added pin status change information from rev 1.3 to rev 1.4. Pin changes are for EP1SGX10C, EP1SGX25C,EP1SGX25D,EP1SGX40 D only.	rev 1.4	5/30/2003
Added section for 1SGX25C missing from 1.4. Changed DATA0 to be an IO after configuration.	rev 1.42	7/30/2003
Note 1: Modifications in Rev 1.4 are recommendations for noise reduction. Do NOT make modifications to the board already laid out based on pin table Rev 1.3 . It is recommended that the pin table Rev 1.4 be implemented for new designs or re-designed boards only.		
NOTE 2 : GND/NC is shown as GND* in Quartus II software		
Add HSSI_GND to the pin list	rev 1.43	9/10/2003
Wrong Bank was referenced in the GX25C device	rev 1.44	9/11/2003
Update non-migration table	rev 1.45	9/17/2003
change all references of GX_TX, GX_RX to GXB_TX, GXB_RX		
Change all references of HSSI_GND to GXB_GND		
Change pin description data[7..1] to include data0		
Changed false references of RUP/RDN to different banks		
Updated pin description so only CLK0n and CLK2n were		
dedicated clock inputs. While the rest were also I/Os		
Updated pin description of VCCINT to expliciltly say it needs a		
1.5V supply		
Updated the pin description for PLLENA		
Update pin description to explain what to do with unused pins	rev 1.46	9/19/2003
for the transceivers and REFCLKB.		
Definition for RUnLU needed to be updated to correctly indicate poarity of signal for remote and local update. Also the pin definitions for GND and NC were added to the pin definition.	rev 1.47	10/21/2003
Updated pin descriptions for items 74 though 78 of the pin descriptions. These describe the VCC voltages and the pin description was updated with more specific information as to what voltage to connect them to.		
Item 42 in the pin desription was updated to specify that the CLK[15..12]p pins are dedicated input clock pins		
Item 43 in the pin desription was updated to specify that the CLK[15..12]n pins are either clock inputs or regular I/O	rev 1.48	12/11/2003
Item 47 through 50 which describe the PLL_OUT pins are updated to specify that they can be used as either I/O or Output		
Items 80 through 83 was updated to describe the termination of the unused pins for GX_RX and GX_TX.		

Items 85 and 86 was updated to describe the termination of the unused pins for REFCLK.		
Updated description for unused VREF pins so the it reads the same description as Quartus II	rev 1.49	3/17/2004
Updated description for RREFB. Layout guidelines were added.	rev 1.50	6/2/2004
Updated RREFB pins to address new Quartus change (please refer to the "RREFB pin change in 1.6" worksheet)		
Deleted DQS for x16 column in EP1SGX10C & EP1SGX10D pin-list	rev 1.60	4/27/2005
Created pin definition for RREFB[15,14]A		
Added CRC_ERROR pins in pin list	rev 1.70	2/22/2006

RREFB pin change in 1.6				
	Device	Status in Rev 1.5	Pin name	Status in Rev 1.6
	EP1SGX10CF672	RREFB15	U7	RREFB15A
		RREFB15	K7	RREFB15
	EP1SGX25CF672	RREFB15	U7	RREFB15
		RREFB15	K7	RREFB15A
	EP1SGX25DF1020	RREFB14	L7	RREFB14
		RREFB14	J7	RREFB14A
		RREFB15	AC7	RREFB15A
		RREFB15	T8	RREFB15
	EP1SGX40DF1020	RREFB14	J7	RREFB13
		RREFB15	AC7	RREFB16
		RREFB15	T7	GND/NC
		RREFB15	T8	RREFB15
		RREFB14	L7	RREFB14