Pin Information For The Stratix™ GX EP1SGX25D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B2	VREF0B2	INPUT	DIFFIO_RX38p		D23	E31		
B2	VREF0B2	INPUT	DIFFIO_RX38n		D24	E32		
B2	VREF0B2	IO	DIFFIO_TX38p		D21	G27		
B2	VREF0B2	IO	DIFFIO_TX38n		D22	G28		
B2	VREF0B2	INPUT	DIFFIO_RX37p		C23	F31		
B2	VREF0B2	INPUT	DIFFIO_RX37n		C24	F32		
B2	VREF0B2	IO	DIFFIO_TX37p		E21	G25		
B2	VREF0B2	IO	DIFFIO_TX37n		E22	G26		
B2	VREF0B2	INPUT	DIFFIO_RX36p		C25	G29		
B2	VREF0B2	INPUT	DIFFIO_RX36n		B25	G30		
B2	VREF0B2	IO	DIFFIO_TX36p		E19	J28		
B2	VREF0B2	IO	DIFFIO_TX36n		E20	H28		
B2	VREF0B2	INPUT	DIFFIO_RX35p		E23	G31		
B2	VREF0B2	INPUT	DIFFIO_RX35n		E24	G32		
B2	VREF0B2	IO	DIFFIO_TX35p		F21	H26		
B2	VREF0B2	IO	DIFFIO_TX35n		F22	H27		
B2	VREF0B2	INPUT	DIFFIO_RX34p		F23	H29		
B2	VREF0B2	INPUT	DIFFIO_RX34n		F24	H30		
B2	VREF0B2	IO	DIFFIO_TX34p		F19	H24		
B2	VREF0B2	IO	DIFFIO_TX34n		F20	H25		
B2	VREF0B2	VREF0B2			L17	M24		
B2	VREF0B2	INPUT	DIFFIO_RX33p		D25	K29		
B2	VREF0B2	INPUT	DIFFIO_RX33n		D26	K30		
B2	VREF0B2	IO	DIFFIO_TX33p		G19	L28		
B2	VREF0B2	IO	DIFFIO_TX33n		G20	K28		
B2	VREF0B2	INPUT	DIFFIO_RX32p		G23	H31		
B2	VREF0B2	INPUT	DIFFIO_RX32n		G24	H32		
B2	VREF0B2	IO	DIFFIO_TX32p		G21	J24		
B2	VREF0B2	IO	DIFFIO_TX32n		G22	J25		
B2	VREF0B2	INPUT	DIFFIO_RX31p		E25	J31		
B2	VREF0B2	INPUT	DIFFIO_RX31n		E26	J32		
B2	VREF0B2	IO	DIFFIO_TX31p		H21	K24		
B2	VREF0B2	IO	DIFFIO_TX31n		H22	K25		
B2	VREF0B2	INPUT	DIFFIO_RX30p		F25	J29		
B2	VREF0B2	INPUT	DIFFIO_RX30n		F26	J30		
B2	VREF0B2	IO	DIFFIO_TX30p		H19	L24		
B2	VREF0B2	IO	DIFFIO_TX30n		H20	L25		
B2	VREF0B2	INPUT	DIFFIO_RX29p/RUP2		G25	L29		
B2	VREF0B2	INPUT	DIFFIO_RX29n/RDN2		G26	L30		
B2	VREF0B2	IO	DIFFIO_TX29p		J21	L26		
B2	VREF0B2	IO	DIFFIO_TX29n		J22	L27		
B2	VREF1B2	INPUT	DIFFIO_RX28p		H25	L31		
B2	VREF1B2	INPUT	DIFFIO_RX28n		H26	L32		
B2	VREF1B2	IO	DIFFIO_TX28p		K21	M25		
B2	VREF1B2	IO	DIFFIO_TX28n		K22	M26		
B2	VREF1B2	INPUT	DIFFIO_RX27p		J23	M29		
B2	VREF1B2	INPUT	DIFFIO_RX27n		J24	M30		
B2	VREF1B2	IO	DIFFIO_TX27p		J19	M27		
B2	VREF1B2	IO	DIFFIO_TX27n		J20	M28		
B2	VREF1B2	INPUT	DIFFIO_RX26p		H23	N29		
B2	VREF1B2	INPUT	DIFFIO_RX26n		H24	N30		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B2	VREF1B2	IO	DIFFIO_TX26p		K19	N25		
B2	VREF1B2	IO	DIFFIO_TX26n		K20	N26		
B2	VREF1B2	INPUT	DIFFIO_RX25p		J25	K31		
B2	VREF1B2	INPUT	DIFFIO_RX25n		J26	K32		
B2	VREF1B2	IO	DIFFIO_TX25p		L21	N27		
B2	VREF1B2	IO	DIFFIO_TX25n		L22	N28		
B2	VREF1B2	INPUT	DIFFIO_RX24p		K25	M31		
B2	VREF1B2	INPUT	DIFFIO_RX24n		K26	M32		
B2	VREF1B2	IO	DIFFIO_TX24p		K17	P25		
B2	VREF1B2	IO	DIFFIO_TX24n		K18	P26		
B2	VREF1B2	VREF1B2			L18	P23		
B2	VREF1B2	INPUT	DIFFIO_RX23p		K23	P29		
B2	VREF1B2	INPUT	DIFFIO_RX23n		K24	P30		
B2	VREF1B2	IO	DIFFIO_TX23p		L19	P24		
B2	VREF1B2	IO	DIFFIO_TX23n		L20	R24		
B2	VREF1B2	INPUT	DIFFIO_RX22p		L23	N31		
B2	VREF1B2	INPUT	DIFFIO_RX22n		L24	N32		
B2	VREF1B2	IO	DIFFIO_TX22p		M21	P27		
B2	VREF1B2	IO	DIFFIO_TX22n		M22	P28		
B2	VREF1B2	INPUT	DIFFIO_RX21p		M23	P31		
B2	VREF1B2	INPUT	DIFFIO_RX21n		M24	R31		
B2	VREF1B2	IO	DIFFIO_TX21p		M19	R27		
B2	VREF1B2	IO	DIFFIO_TX21n		M20	R28		
B2	VREF1B2	INPUT	DIFFIO_RX20p		L25	R29		
B2	VREF1B2	INPUT	DIFFIO_RX20n		M25	R30		
B2	VREF1B2	IO	DIFFIO_TX20p		M17	R25		
B2	VREF1B2	IO	DIFFIO_TX20n		M18	R26		
B2	VREF1B2	CLK0n			N26	T32		
B2	VREF1B2	CLK0p			N25	T31		
B2	VREF1B2	IO	CLK1n		N24	T30		
B2	VREF1B2	CLK1p			N23	T29		
		VCCA_PLL1			N20	T27		
		GND						
		GNDA_PLL1			N22	T28		
		VCCG_PLL1			N21	T25		
		GNDG_PLL1			N19	T26		
		VCCA_PLL2			P21	U27		
		GND						
		GNDA_PLL2			P22	U28		
		VCCG_PLL2			P20	U25		
		GNDG_PLL2			P19	U26		
B1	VREF0B1	CLK2p			P25	U31		
B1	VREF0B1	CLK2n			P26	U32		
B1	VREF0B1	CLK3p			P23	U29		
B1	VREF0B1	IO	CLK3n		P24	U30		
B1	VREF0B1	INPUT	DIFFIO_RX19p		R25	V29		
B1	VREF0B1	INPUT	DIFFIO_RX19n		T25	V30		
B1	VREF0B1	IO	DIFFIO_TX19p		R17	V27		
B1	VREF0B1	IO	DIFFIO_TX19n		R18	V28		
B1	VREF0B1	INPUT	DIFFIO_RX18p		U25	V31		
B1	VREF0B1	INPUT	DIFFIO_RX18n		U26	W31		

Pin Information For The Stratix™ GX EP1SGX25D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B1	VREF0B1	IO	DIFFIO_TX18p		R19	V25		
B1	VREF0B1	IO	DIFFIO_TX18n		R20	V26		
B1	VREF0B1	INPUT	DIFFIO_RX17p		R23	Y31		
B1	VREF0B1	INPUT	DIFFIO_RX17n		R24	Y32		
B1	VREF0B1	IO	DIFFIO_TX17p		R21	V24		
B1	VREF0B1	IO	DIFFIO_TX17n		R22	W24		
B1	VREF0B1	VREF0B1			R16	V23		
B1	VREF0B1	INPUT	DIFFIO_RX16p		V25	W29		
B1	VREF0B1	INPUT	DIFFIO_RX16n		V26	W30		
B1	VREF0B1	IO	DIFFIO_TX16p		T19	W27		
B1	VREF0B1	IO	DIFFIO_TX16n		T20	W28		
B1	VREF0B1	INPUT	DIFFIO_RX15p		T23	AA31		
B1	VREF0B1	INPUT	DIFFIO_RX15n		T24	AA32		
B1	VREF0B1	IO	DIFFIO_TX15p		T21	W25		
B1	VREF0B1	IO	DIFFIO_TX15n		T22	W26		
B1	VREF0B1	INPUT	DIFFIO_RX14p		W25	AC31		
B1	VREF0B1	INPUT	DIFFIO_RX14n		W26	AC32		
B1	VREF0B1	IO	DIFFIO_TX14p		U17	Y25		
B1	VREF0B1	IO	DIFFIO_TX14n		U18	Y26		
B1	VREF1B1	INPUT	DIFFIO_RX13p		U23	Y29		
B1	VREF1B1	INPUT	DIFFIO_RX13n		U24	Y30		
B1	VREF1B1	IO	DIFFIO_TX13p		U19	Y27		
B1	VREF1B1	IO	DIFFIO_TX13n		U20	Y28		
B1	VREF1B1	INPUT	DIFFIO_RX12p		W23	AB31		
B1	VREF1B1	INPUT	DIFFIO_RX12n		W24	AB32		
B1	VREF1B1	IO	DIFFIO_TX12p		V19	AA25		
B1	VREF1B1	IO	DIFFIO_TX12n		V20	AA26		
B1	VREF1B1	INPUT	DIFFIO_RX11p		V23	AA29		
B1	VREF1B1	INPUT	DIFFIO_RX11n		V24	AA30		
B1	VREF1B1	IO	DIFFIO_TX11p		U21	AA27		
B1	VREF1B1	IO	DIFFIO_TX11n		U22	AA28		
B1	VREF1B1	INPUT	DIFFIO_RX10p/RUP1		Y25	AB29		
B1	VREF1B1	INPUT	DIFFIO_RX10n/RDN1		Y26	AB30		
B1	VREF1B1	IO	DIFFIO_TX10p		V21	AB26		
B1	VREF1B1	IO	DIFFIO_TX10n		V22	AB27		
B1	VREF1B1	VREF1B1			T18	W23		
B1	VREF1B1	INPUT	DIFFIO_RX9p		Y23	AC29		
B1	VREF1B1	INPUT	DIFFIO_RX9n		Y24	AC30		
B1	VREF1B1	IO	DIFFIO_TX9p		W19	AB24		
B1	VREF1B1	IO	DIFFIO_TX9n		W20	AB25		
B1	VREF1B1	INPUT	DIFFIO_RX8p		AA25	AD31		
B1	VREF1B1	INPUT	DIFFIO_RX8n		AA26	AD32		
B1	VREF1B1	IO	DIFFIO_TX8p		Y19	AC24		
B1	VREF1B1	IO	DIFFIO_TX8n		Y20	AC25		
B1	VREF1B1	INPUT	DIFFIO_RX7p		AA23	AE31		
B1	VREF1B1	INPUT	DIFFIO_RX7n		AA24	AE32		
B1	VREF1B1	IO	DIFFIO_TX7p		AA19	AD24		
B1	VREF1B1	IO	DIFFIO_TX7n		AA20	AD25		
B1	VREF2B1	INPUT	DIFFIO_RX6p		AB25	AE29		
B1	VREF2B1	INPUT	DIFFIO_RX6n		AB26	AE30		
B1	VREF2B1	IO	DIFFIO_TX6p		AB19	AB28		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B1	VREF2B1	IO	DIFFIO_TX6n		AB20	AC28		
B1	VREF2B1	INPUT	DIFFIO_RX5p		AB23	AD29		
B1	VREF2B1	INPUT	DIFFIO_RX5n		AB24	AD30		
B1	VREF2B1	IO	DIFFIO_TX5p		AC19	AE24		
B1	VREF2B1	IO	DIFFIO_TX5n		AC20	AE25		
B1	VREF2B1	INPUT	DIFFIO_RX4p		AC25	AF29		
B1	VREF2B1	INPUT	DIFFIO_RX4n		AC26	AF30		
B1	VREF2B1	IO	DIFFIO_TX4p		W21	AE26		
B1	VREF2B1	IO	DIFFIO_TX4n		W22	AE27		
B1	VREF2B1	INPUT	DIFFIO_RX3p		AC23	AF31		
B1	VREF2B1	INPUT	DIFFIO_RX3n		AC24	AF32		
B1	VREF2B1	IO	DIFFIO_TX3p		Y21	AD28		
B1	VREF2B1	IO	DIFFIO_TX3n		Y22	AE28		
B1	VREF2B1	VREF2B1			T17	AA24		
B1	VREF2B1	INPUT	DIFFIO_RX2p		AE23	AG31		
B1	VREF2B1	INPUT	DIFFIO_RX2n		AE24	AG32		
B1	VREF2B1	IO	DIFFIO_TX2p		AA21	AF25		
B1	VREF2B1	IO	DIFFIO_TX2n		AA22	AF26		
B1	VREF2B1	INPUT	DIFFIO_RX1p		AD23	AG29		
B1	VREF2B1	INPUT	DIFFIO_RX1n		AD24	AG30		
B1	VREF2B1	IO	DIFFIO_TX1p		AB21	AF27		
B1	VREF2B1	IO	DIFFIO_TX1n		AB22	AF28		
B1	VREF2B1	INPUT	DIFFIO_RX0p		AD25	AH31		
B1	VREF2B1	INPUT	DIFFIO_RX0n		AE25	AH32		
B1	VREF2B1	IO	DIFFIO_TX0p		AC21	AG27		
B1	VREF2B1	IO	DIFFIO_TX0n		AC22	AG28		
B8	VREF0B8	IO				AH30		
B8	VREF0B8	IO	DQ9B7		AF23	AK29	DQ3B15	DQ1B31
B8	VREF0B8	IO				AJ30		
B8	VREF0B8	IO	DQ9B6		AE22	AL29	DQ3B14	DQ1B30
B8	VREF0B8	IO	DQ9B5		AD22	AM29	DQ3B13	DQ1B29
B8	VREF0B8	IO	DQ9B4		AF22	AK28	DQ3B12	DQ1B28
B8	VREF0B8	IO				AK31		
B8	VREF0B8	IO	DQ9B3		AF21	AL28	DQ3B11	DQ1B27
B8	VREF0B8	IO				AH29		
B8	VREF0B8	IO	DQS9B		AE21	AM28		
B8	VREF0B8	IO	DQ9B2		AD21	AK27	DQ3B10	DQ1B26
B8	VREF0B8	IO				AK30		
B8	VREF0B8	IO	DQ9B1		AD20	AL27	DQ3B9	DQ1B25
B8	VREF0B8	IO				AB23		
B8	VREF0B8	IO	DQ9B0		AE20	AM27	DQ3B8	DQ1B24
B8	VREF0B8	IO				AJ29		
B8	VREF0B8	IO				AH28		
B8	VREF0B8	IO	DQ8B7		AF20	AJ26	DQ3B7	DQ1B23
B8	VREF0B8	VREF0B8			V18	AA22		
B8	VREF0B8	IO	DQ8B6		AE19	AK26	DQ3B6	DQ1B22
B8	VREF0B8	IO	DQ8B5		AD18	AL26	DQ3B5	DQ1B21
B8	VREF0B8	IO				AL31		
B8	VREF0B8	IO	DQ8B4		AD19	AH25	DQ3B4	DQ1B20
B8	VREF0B8	IO	DQ8B3		AF19	AM26	DQ3B3	DQ1B19
B8	VREF0B8	IO				AL30		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B8	VREF0B8	IO	DQS8B		AE18	AJ25	DQS3B	
B8	VREF0B8	IO	DQ8B2		AF17	AK25	DQ3B2	DQ1B18
B8	VREF0B8	IO				AC23		
B8	VREF0B8	IO	DQ8B1		AC18	AL25	DQ3B1	DQ1B17
B8	VREF0B8	IO	DQ8B0		AF18	AM25	DQ3B0	DQ1B16
B8	VREF0B8	IO				AG26		
B8	VREF1B8	IO				AB22		
B8	VREF1B8	IO	DQ7B7		Y18	AJ24	DQ2B15	DQ1B15
B8	VREF1B8	IO				AJ28		
B8	VREF1B8	IO	DQ7B6		AA18	AK24	DQ2B14	DQ1B14
B8	VREF1B8	IO	DQ7B5		AB18	AL24	DQ2B13	DQ1B13
B8	VREF1B8	IO				AH27		
B8	VREF1B8	IO	DQ7B4		W18	AM24	DQ2B12	DQ1B12
B8	VREF1B8	IO	DQ7B3		AB16	AH23	DQ2B11	DQ1B11
B8	VREF1B8	IO				AD23		
B8	VREF1B8	IO	DQS7B		AA17	AJ23		DQS1B
B8	VREF1B8	IO	DQ7B2		AB17	AK23	DQ2B10	DQ1B10
B8	VREF1B8	IO				AF24		
B8	VREF1B8	IO	DQ7B1		W17	AL23	DQ2B9	DQ1B9
B8	VREF1B8	IO				AC22		
B8	VREF1B8	IO	DQ7B0		Y17	AM23	DQ2B8	DQ1B8
B8	VREF1B8	IO	DQ6B7		AE17	AH22	DQ2B7	DQ1B7
B8	VREF1B8	IO	FCLK3		T16	AE22		
B8	VREF1B8	IO	FCLK2		U16	AF22		
B8	VREF1B8	VREF1B8			V17	AA21		
B8	VREF1B8	IO	DQ6B6		AD17	AL22	DQ2B6	DQ1B6
B8	VREF1B8	IO	DQ6B5		AD15	AJ22	DQ2B5	DQ1B5
B8	VREF1B8	IO				AD22		
B8	VREF1B8	IO	DQ6B4		AE16	AK22	DQ2B4	DQ1B4
B8	VREF1B8	IO		PGM2	T15	AF21		
B8	VREF1B8	IO	DQ6B3		AC17	AM22	DQ2B3	DQ1B3
B8	VREF1B8	IO				AA23		
B8	VREF1B8	IO	DQS6B		AD16	AL21	DQS2B	
B8	VREF1B8	IO	DQ6B2		AC15	AM21	DQ2B2	DQ1B2
B8	VREF1B8	IO		CRC_ERROR	U15	AE21		
B8	VREF1B8	IO	DQ6B1		AC16	AJ21	DQ2B1	DQ1B1
B8	VREF1B8	IO	DQ6B0		AE15	AK21	DQ2B0	DQ1B0
B8	VREF1B8	IO	RDN8		R15	AD21		
B8	VREF1B8	IO	RUP8		V16	AF20		
B8	VREF1B8	IO	DQ5B7		Y16	AH21		
B8	VREF1B8	IO				AH26		
B8	VREF1B8	IO	DQ5B6		AA16	AJ20		
B8	VREF1B8	IO	DQ5B5		AB15	AK20		
B8	VREF2B8	IO				AE23		
B8	VREF2B8	IO	DQ5B4		W14	AL20		
B8	VREF2B8	IO		RDYnBSY	W16	AC21		
B8	VREF2B8	IO	DQ5B3		Y15	AJ19		
B8	VREF2B8	IO				AF23		
B8	VREF2B8	IO	DQS5B		AA15	AG20		
B8	VREF2B8	IO	DQ5B2		W13	AH20		
B8	VREF2B8	IO		nCS	R13	AB21		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B8	VREF2B8	IO	DQ5B1		Y13	AG19		
B8	VREF2B8	IO	DQ5B0		Y14	AH19		
B8	VREF2B8	IO				AG24		
B8	VREF2B8	IO				AG22		
B8	VREF2B8	IO				AG25		
B8	VREF2B8	IO				AJ27		
B8	VREF2B8	IO		CS	U14	AE20		
B8	VREF2B8	IO				AH24		
B8	VREF2B8	IO				AG23		
B8	VREF2B8	IO				AG21		
B8	VREF2B8	VREF2B8			V15	AA20		
B8	VREF2B8	IO	CLK5n		AD14	AL19		
B8	VREF2B8	CLK5p			AC14	AK19		
B8	VREF2B8	IO	CLK4n		AF14	AM18		
B8	VREF2B8	CLK4p			AE14	AL18		
B8	VREF2B8	PLL_ENA		PLL_ENA	W15	AC20		
B8	VREF2B8	MSEL0		MSEL0	U13	AD20		
B8	VREF2B8	MSEL1		MSEL1	T13	AB20		
B8	VREF2B8	MSEL2		MSEL2	V14	AB19		
B12	VREF2B8	IO	PLL6_OUT3n		AF13	AH18		
B12	VREF2B8	IO	PLL6_OUT3p		AE13	AG18		
B12	VREF2B8	IO	PLL6_OUT2n		AB14	AK18		
B12	VREF2B8	IO	PLL6_OUT2p		AA14	AJ18		
B11	VREF2B8	IO	PLL6_FBn		AE12	AH17		
B11	VREF2B8	IO	PLL6_FBp		AD12	AG17		
B11	VREF2B8	IO	PLL6_OUT1n		AB13	AK17		
B11	VREF2B8	IO	PLL6_OUT1p		AA13	AJ17		
B11	VREF2B8	IO	PLL6_OUT0n		AD13	AM17		
B11	VREF2B8	IO	PLL6_OUT0p		AC13	AL17		
B12		VCC_PLL6_OUTB			R11	AA18		
B11		VCC_PLL6_OUTA			V13	AB18		
		VCCA_PLL6			T11	AC18		
		GND						
		GNDA_PLL6			W12	AB17		
		VCCG_PLL6			V12	AC17		
		GNDG_PLL6			U12	AA17		
B7	VREF0B7	CLK7p			Y12	AG16		
B7	VREF0B7	IO	CLK7n		AA12	AH16		
B7	VREF0B7	CLK6p			AB12	AJ16		
B7	VREF0B7	IO	CLK6n		AC12	AK16		
B7	VREF0B7	nCE		nCE	P9	AD16		
B7	VREF0B7	nCEO		nCEO	T9	AE16		
B7	VREF0B7	IO				Y18		
B7	VREF0B7	IO				AC19		
B7	VREF0B7	IO		PGM0	R10	AD18		
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	T10	AB15		
B7	VREF0B7	VCCSEL		VCCSEL	R9	AA15		
B7	VREF0B7	PORSEL		PORSEL	U10	AC15		
B7	VREF0B7	IO				Y17		
B7	VREF0B7	IO				V14		
B7	VREF0B7	IO				AE19		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B7	VREF0B7	IO				AE15		
B7	VREF0B7	IO				AE18		
B7	VREF0B7	IO				AF16		
B7	VREF0B7	VREF0B7			V11	Y16		
B7	VREF0B7	IO		INIT_DONE	U11	AD19		
B7	VREF0B7	IO				W14		
B7	VREF0B7	IO	DQ4B7		AC11	AG15		
B7	VREF0B7	IO	DQ4B6		AB11	AJ15		
B7	VREF0B7	IO		nRS	U9	AE17		
B7	VREF0B7	IO	DQ4B5		AD11	AH15		
B7	VREF0B7	IO				Y14		
B7	VREF0B7	IO	DQ4B4		AA11	AK15		
B7	VREF0B7	IO	DQ4B3		AD10	AL15		
B7	VREF0B7	IO		RUnLU	W11	AF18		
B7	VREF0B7	IO	DQS4B		AC10	AL14		
B7	VREF0B7	IO			Y11	AD15		
B7	VREF1B7	IO	DQ4B2		AA9	AM14		
B7	VREF1B7	IO	DQ4B1		AA10	AM15		
B7	VREF1B7	IO		PGM1	U8	AF17		
B7	VREF1B7	IO	DQ4B0		AB10	AK14		
B7	VREF1B7	IO	RDN7		V8	AC14		
B7	VREF1B7	IO	RUP7		Y10	AF19		
B7	VREF1B7	IO	DQ3B7		AF8	AG14	DQ1B15	DQ0B31
B7	VREF1B7	IO				AA14		
B7	VREF1B7	IO	DQ3B6		AE11	AH14	DQ1B14	DQ0B30
B7	VREF1B7	IO	DQ3B5		AE10	AL13	DQ1B13	DQ0B29
B7	VREF1B7	IO	DEV_CLRn		W10	AD14		
B7	VREF1B7	IO	DQ3B4		AF10	AM13	DQ1B12	DQ0B28
B7	VREF1B7	IO	DQ3B3		AE8	AJ14	DQ1B11	DQ0B27
B7	VREF1B7	IO				AB14		
B7	VREF1B7	IO	DQS3B		AE9	AH13	DQS1B	
B7	VREF1B7	IO				U13		
B7	VREF1B7	IO	DQ3B2		AF9	AJ13	DQ1B10	DQ0B26
B7	VREF1B7	IO	DQ3B1		AD9	AK13	DQ1B9	DQ0B25
B7	VREF1B7	VREF1B7			V10	Y15		
B7	VREF1B7	IO	DQ3B0		AD8	AG13	DQ1B8	DQ0B24
B7	VREF1B7	IO				AA13		
B7	VREF1B7	IO				V13		
B7	VREF1B7	IO	DQ2B7		AC9	AD13	DQ1B7	DQ0B23
B7	VREF1B7	IO	FCLK5		W9	AF15		
B7	VREF1B7	IO	FCLK4		Y9	U14		
B7	VREF1B7	IO	DQ2B6		Y7	AC13	DQ1B6	DQ0B22
B7	VREF1B7	IO	DQ2B5		AA7	AE13	DQ1B5	DQ0B21
B7	VREF1B7	IO				W13		
B7	VREF1B7	IO	DQ2B4		AC8	AF13	DQ1B4	DQ0B20
B7	VREF1B7	IO	DQ2B3		AB9	AB13	DQ1B3	DQ0B19
B7	VREF1B7	IO				AE14		
B7	VREF2B7	IO	DQS2B		AB7	AE12		DQS0B
B7	VREF2B7	IO	DQ2B2		Y8	AF12	DQ1B2	DQ0B18
B7	VREF2B7	IO			V7	V12		
B7	VREF2B7	IO	DQ2B1		AA8	AC12	DQ1B1	DQ0B17

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B7	VREF2B7	IO	DQ2B0		AB8	AD12	DQ1B0	DQ0B16
B7	VREF2B7	IO				AF14		
B7	VREF2B7	IO				AA12		
B7	VREF2B7	IO	DQ1B7		AF5	AF11	DQ0B15	DQ0B15
B7	VREF2B7	IO	DQ1B6		AD7	AB11	DQ0B14	DQ0B14
B7	VREF2B7	IO				W12		
B7	VREF2B7	IO	DQ1B5		AF7	AB12	DQ0B13	DQ0B13
B7	VREF2B7	IO	DQ1B4		AE7	AE11	DQ0B12	DQ0B12
B7	VREF2B7	IO				V11		
B7	VREF2B7	IO	DQ1B3		AD6	AC11	DQ0B11	DQ0B11
B7	VREF2B7	IO	DQS1B		AE6	AD11	DQS0B	
B7	VREF2B7	IO			W8	W11		
B7	VREF2B7	IO	DQ1B2		AF6	AE10	DQ0B10	DQ0B10
B7	VREF2B7	IO	DQ1B1		AC7	AC10	DQ0B9	DQ0B9
B7	VREF2B7	VREF2B7			V9	Y13		
B7	VREF2B7	IO	DQ1B0		AC6	AD10	DQ0B8	DQ0B8
B7	VREF2B7	IO				AA11		
B7	VREF2B7	IO				Y11		
B7	VREF2B7	IO	DQ0B7		AF4	AC9	DQ0B7	DQ0B7
B7	VREF2B7	IO				V10		
B7	VREF2B7	IO	DQ0B6		AE5	AF8	DQ0B6	DQ0B6
B7	VREF2B7	IO				W10		
B7	VREF2B7	IO	DQ0B5		AC4	AF10	DQ0B5	DQ0B5
B7	VREF2B7	IO	DQ0B4		AD4	AC8	DQ0B4	DQ0B4
B7	VREF2B7	IO				AA10		
B7	VREF2B7	IO	DQ0B3		AD5	AE8	DQ0B3	DQ0B3
B7	VREF2B7	IO	DQS0B		AE4	AF9		
B7	VREF2B7	IO				Y10		
B7	VREF2B7	IO	DQ0B2		AE2	AD8	DQ0B2	DQ0B2
B7	VREF2B7	IO	DQ0B1		AE3	AD9	DQ0B1	DQ0B1
B7	VREF2B7	IO			W7	AB10		
B7	VREF2B7	IO	DQ0B0		AC5	AE9	DQ0B0	DQ0B0
B7	VREF2B7	IO				AD7		
B15		GND/NC				AL11		
B15		GND/NC				AM11		
B15		GND/NC				AH11		
B15		GND/NC				AJ11		
B15		GND/NC				AL9		
B15		GND/NC				AM9		
B15		GND/NC				AH9		
B15		GND/NC				AJ9		
B15		VCCA_B15				AD6		
B15		GND/NC				AL7		
B15		GND/NC				AM7		
		VCCG_B15				AC6		
		GND				AB6		
B15		RREFB15A				AC7		
B15		GND/NC				AL5		
B15		GND/NC				AM5		
B15		GND/NC				AH7		
B15		GND/NC				AJ7		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B15		GND/NC				AM3		
B15		GND/NC				AM2		
B15		GND/NC				AJ5		
B15		GND/NC				AJ4		
B15		GXB_RX11n			AC2	AK2		
B15		GXB_RX11p			AC1	AK1		
B15		GXB_TX11n			AA5	AG5		
B15		GXB_TX11p			AA4	AG4		
B15		GXB_RX10n			AA2	AH2		
B15		GXB_RX10p			AA1	AH1		
B15		GXB_TX10n			W5	AE5		
B15		GXB_TX10p			W4	AE4		
B15		VCCA_B15			P8	AA6		
B15		REFCLKB15n			W2	AF2		
B15		REFCLKB15p			W1	AF1		
		VCCG_B15			P7	W6		
		GND			P6	Y6		
B15		RREFB15			U7	T8		
B15		GXB_RX8n			U2	AD2		
B15		GXB_RX8p			U1	AD1		
B15		GXB_TX8n			U5	AC5		
B15		GXB_TX8p			U4	AC4		
B15		GXB_RX9n			R2	AB2		
B15		GXB_RX9p			R1	AB1		
B15		GXB_TX9n			R5	AA5		
B15		GXB_TX9p			R4	AA4		
B14		GXB_RX7n			N2	K2		
B14		GXB_RX7p			N1	K1		
B14		GXB_TX7n			N5	L5		
B14		GXB_TX7p			N4	L4		
B14		GXB_RX6n			L2	H2		
B14		GXB_RX6p			L1	H1		
B14		GXB_TX6n			L5	J5		
B14		GXB_TX6p			L4	J4		
B14		VCCA_B14			N7	R6		
B14		REFCLKB14n			J2	F2		
B14		REFCLKB14p			J1	F1		
		VCCG_B14			N8	N6		
		GND			N6	P6		
B14		RREFB14			K7	L7		
B14		GXB_RX4n			G2	D2		
B14		GXB_RX4p			G1	D1		
B14		GXB_TX4n			J5	G5		
B14		GXB_TX4p			J4	G4		
B14		GXB_RX5n			E2	B2		
B14		GXB_RX5p			E1	B1		
B14		GXB_TX5n			G5	E4		
B14		GXB_TX5p			G4	D4		
B14		GND/NC				B4		
B14		GND/NC				A4		
B14		GND/NC				E6		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B14		GND/NC				D6		
B14		GND/NC				B6		
B14		GND/NC				A6		
B14		GND/NC				E8		
B14		GND/NC				D8		
B14		VCCA_B14				M6		
B14		GND/NC				B8		
B14		GND/NC				A8		
		VCCG_B14				K6		
		GND				L6		
B14		RREFB14A				J7		
B14		GND/NC				B10		
B14		GND/NC				A10		
B14		GND/NC				E10		
B14		GND/NC				D10		
B14		GND/NC				B12		
B14		GND/NC				A12		
B14		GND/NC				E12		
B14		GND/NC				D12		
B4	VREF0B4	IO				K7		
B4	VREF0B4	IO	DQ0T0		B2	H9	DQ0T0	DQ0T0
B4	VREF0B4	IO				L8		
B4	VREF0B4	IO	DQ0T1		C2	J8	DQ0T1	DQ0T1
B4	VREF0B4	IO	DQ0T2		C1	K8	DQ0T2	DQ0T2
B4	VREF0B4	IO	DQS0T		C3	G8		
B4	VREF0B4	IO			H7	H7		
B4	VREF0B4	IO	DQ0T3		B3	J9	DQ0T3	DQ0T3
B4	VREF0B4	IO				L10		
B4	VREF0B4	IO	DQ0T4		D4	K9	DQ0T4	DQ0T4
B4	VREF0B4	IO	DQ0T5		E4	G9	DQ0T5	DQ0T5
B4	VREF0B4	IO				N10		
B4	VREF0B4	IO	DQ0T6		B4	H8	DQ0T6	DQ0T6
B4	VREF0B4	IO				M10		
B4	VREF0B4	IO	DQ0T7		C4	L9	DQ0T7	DQ0T7
B4	VREF0B4	IO				M11		
B4	VREF0B4	IO				P10		
B4	VREF0B4	IO	DQ1T0		E5	J10	DQ0T8	DQ0T8
B4	VREF0B4	VREF0B4			K9	N12		
B4	VREF0B4	IO	DQ1T1		C6	K10	DQ0T9	DQ0T9
B4	VREF0B4	IO	DQ1T2		B5	G10	DQ0T10	DQ0T10
B4	VREF0B4	IO				R10		
B4	VREF0B4	IO	DQS1T		C5	H10	DQS0T	
B4	VREF0B4	IO				N11		
B4	VREF0B4	IO	DQ1T3		D5	K11	DQ0T11	DQ0T11
B4	VREF0B4	IO	DQ1T4		A5	H11	DQ0T12	DQ0T12
B4	VREF0B4	IO				P11		
B4	VREF0B4	IO	DQ1T5		A4	J11	DQ0T13	DQ0T13
B4	VREF0B4	IO				R11		
B4	VREF0B4	IO	DQ1T6		E6	L11	DQ0T14	DQ0T14
B4	VREF0B4	IO	DQ1T7		D6	G11	DQ0T15	DQ0T15
B4	VREF0B4	IO			G9	M12		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B4	VREF0B4	IO				R12		
B4	VREF0B4	IO	DQ2T0		B6	J12	DQ1T0	DQ0T16
B4	VREF0B4	IO	DQ2T1		E8	K12	DQ1T1	DQ0T17
B4	VREF0B4	IO				P12		
B4	VREF0B4	IO	DQ2T2		F7	G12	DQ1T2	DQ0T18
B4	VREF1B4	IO	DQS2T		C7	H12		DQS0T
B4	VREF1B4	IO				T12		
B4	VREF1B4	IO	DQ2T3		A6	L12	DQ1T3	DQ0T19
B4	VREF1B4	IO	DQ2T4		B7	H13	DQ1T4	DQ0T20
B4	VREF1B4	IO	DQ2T5		D7	J13	DQ1T5	DQ0T21
B4	VREF1B4	IO	DQ2T6		E7	L13	DQ1T6	DQ0T22
B4	VREF1B4	IO	FCLK6		G10	M13		
B4	VREF1B4	IO	FCLK7		G7	T14		
B4	VREF1B4	IO	DQ2T7		A7	K13	DQ1T7	DQ0T23
B4	VREF1B4	IO				P13		
B4	VREF1B4	IO			H8	U12		
B4	VREF1B4	IO	DQ3T0		D8	G13	DQ1T8	DQ0T24
B4	VREF1B4	VREF1B4			K10	N13		
B4	VREF1B4	IO	DQ3T1		A8	D14	DQ1T9	DQ0T25
B4	VREF1B4	IO				L14		
B4	VREF1B4	IO	DQ3T2		C9	F14	DQ1T10	DQ0T26
B4	VREF1B4	IO				R13		
B4	VREF1B4	IO	DQS3T		B8	G14	DQS1T	
B4	VREF1B4	IO	DQ3T3		C8	E14	DQ1T11	DQ0T27
B4	VREF1B4	IO				N14		
B4	VREF1B4	IO	DQ3T4		A10	H14	DQ1T12	DQ0T28
B4	VREF1B4	IO	DQ3T5		A9	J14	DQ1T13	DQ0T29
B4	VREF1B4	IO	DEV_OE		J7	M14		
B4	VREF1B4	IO	DQ3T6		B9	G15	DQ1T14	DQ0T30
B4	VREF1B4	IO	DQ3T7		D9	H15	DQ1T15	DQ0T31
B4	VREF1B4	IO	RUP4		G11	H19		
B4	VREF1B4	IO	RDN4		G8	K14		
B4	VREF1B4	IO	DQ4T0		D10	C14		
B4	VREF1B4	IO		nWS	H11	G19		
B4	VREF1B4	IO	DQ4T1		E9	A15		
B4	VREF1B4	IO	DQ4T2		E10	A14		
B4	VREF2B4	IO				G17		
B4	VREF2B4	IO	DQS4T		B10	B14		
B4	VREF2B4	IO		DATA0	H10	H17		
B4	VREF2B4	IO	DQ4T3		E11	B15		
B4	VREF2B4	IO	DQ4T4		C10	C15		
B4	VREF2B4	IO				T13		
B4	VREF2B4	IO	DQ4T5		B11	F15		
B4	VREF2B4	IO		DATA1	F8	H18		
B4	VREF2B4	IO	DQ4T6		D11	D15		
B4	VREF2B4	IO	DQ4T7		C11	E15		
B4	VREF2B4	IO				P14		
B4	VREF2B4	IO		DATA2	K8	L19		
B4	VREF2B4	VREF2B4			K11	N15		
B4	VREF2B4	IO				G18		
B4	VREF2B4	IO				J18		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B4	VREF2B4	IO				L15		
B4	VREF2B4	IO				K19		
B4	VREF2B4	IO				M15		
B4	VREF2B4	IO				R14		
B4	VREF2B4	TMS		TMS	F9	G16		
B4	VREF2B4	TRST		TRST	H9	J15		
B4	VREF2B4	TCK		TCK	J8	K15		
B4	VREF2B4	IO		DATA3	J9	J19		
B4	VREF2B4	IO				N18		
B4	VREF2B4	IO				N17		
B4	VREF2B4	TDI		TDI	F10	H16		
B4	VREF2B4	TDO		TDO	F11	J16		
B4	VREF2B4	IO	CLK12n		D12	C16		
B4	VREF2B4	CLK12p			E12	D16		
B4	VREF2B4	IO	CLK13n		F12	E16		
B4	VREF2B4	CLK13p			G12	F16		
		TEMPDIODEp			J11	L21		
		TEMPDIODEn			J10	L20		
		VCCA_PLL5			H13	L18		
		GND						
		GNDA_PLL5			G13	L17		
		VCCG_PLL5			H12	K17		
		GNDG_PLL5			J12	M17		
B9		VCC_PLL5_OUTA			J13	K18		
B10		VCC_PLL5_OUTB			K12	M18		
B9	VREF0B3	IO	PLL5_OUT0p		D13	F18		
B9	VREF0B3	IO	PLL5_OUT0n		C13	E18		
B9	VREF0B3	IO	PLL5_OUT1p		C12	D17		
B9	VREF0B3	IO	PLL5_OUT1n		B12	C17		
B9	VREF0B3	IO	PLL5_FBp		F13	F17		
B9	VREF0B3	IO	PLL5_FBn		E13	E17		
B10	VREF0B3	IO	PLL5_OUT2p		F14	B17		
B10	VREF0B3	IO	PLL5_OUT2n		E14	A17		
B10	VREF0B3	IO	PLL5_OUT3p		B13	D18		
B10	VREF0B3	IO	PLL5_OUT3n		A13	C18		
B3	VREF0B3	nSTATUS		nSTATUS	K14	L22		
B3	VREF0B3	nCONFIG		nCONFIG	L14	K20		
B3	VREF0B3	DCLK		DCLK	K13	J20		
B3	VREF0B3	CONF_DONE		CONF_DONE	K15	K21		
B3	VREF0B3	CLK14p			B14	B18		
B3	VREF0B3	IO	CLK14n		A14	A18		
B3	VREF0B3	CLK15p			D14	C19		
B3	VREF0B3	IO	CLK15n		C14	B19		
B3	VREF0B3	VREF0B3			J16	M19		
B3	VREF0B3	IO				E24		
B3	VREF0B3	IO				F24		
B3	VREF0B3	IO		DATA4	L15	G20		
B3	VREF0B3	IO				D27		
B3	VREF0B3	IO				F25		
B3	VREF0B3	IO				H23		
B3	VREF0B3	IO				F23		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B3	VREF0B3	IO				G23		
B3	VREF0B3	IO	DQ5T0		G14	E19		
B3	VREF0B3	IO	DQ5T1		H14	F19		
B3	VREF0B3	IO		DATA5	M15	H20		
B3	VREF0B3	IO	DQ5T2		J14	E20		
B3	VREF0B3	IO	DQS5T		G15	F20		
B3	VREF0B3	IO				D28		
B3	VREF0B3	IO	DQ5T3		G16	D19		
B3	VREF0B3	IO		DATA6	K16	J21		
B3	VREF0B3	IO	DQ5T4		H16	B20		
B3	VREF0B3	IO	DQ5T5		J15	C20		
B3	VREF1B3	IO				E26		
B3	VREF1B3	IO	DQ5T6		F16	D20		
B3	VREF1B3	IO				G24		
B3	VREF1B3	IO	DQ5T7		H15	E21		
B3	VREF1B3	IO	RUP3		L16	H21		
B3	VREF1B3	IO	RDN3		M16	G21		
B3	VREF1B3	IO	DQ6T0		E16	C21	DQ2T0	DQ1T0
B3	VREF1B3	IO	DQ6T1		B15	D21	DQ2T1	DQ1T1
B3	VREF1B3	IO		DATA7	G17	F21		
B3	VREF1B3	IO	DQ6T2		E15	A21	DQ2T2	DQ1T2
B3	VREF1B3	IO	DQS6T		D15	B21	DQS2T	
B3	VREF1B3	IO				D29		
B3	VREF1B3	IO	DQ6T3		C16	A22	DQ2T3	DQ1T3
B3	VREF1B3	IO		CLKUSR	F17	F22		
B3	VREF1B3	IO	DQ6T4		D16	C22	DQ2T4	DQ1T4
B3	VREF1B3	IO				J22		
B3	VREF1B3	IO	DQ6T5		F15	D22	DQ2T5	DQ1T5
B3	VREF1B3	IO	DQ6T6		C15	B22	DQ2T6	DQ1T6
B3	VREF1B3	VREF1B3			J17	M20		
B3	VREF1B3	IO	FCLK0		F18	G22		
B3	VREF1B3	IO	FCLK1		G18	H22		
B3	VREF1B3	IO	DQ6T7		B16	E22	DQ2T7	DQ1T7
B3	VREF1B3	IO				E27		
B3	VREF1B3	IO				F26		
B3	VREF1B3	IO	DQ7T0		E17	A23	DQ2T8	DQ1T8
B3		GND			H17	K22		
B3	VREF1B3	IO	DQ7T1		B17	B23	DQ2T9	DQ1T9
B3	VREF1B3	IO	DQ7T2		A17	C23	DQ2T10	DQ1T10
B3	VREF1B3	IO				J23		
B3	VREF1B3	IO	DQS7T		C17	D23		DQS1T
B3	VREF1B3	IO	DQ7T3		D17	E23	DQ2T11	DQ1T11
B3	VREF1B3	IO				K23		
B3	VREF1B3	IO	DQ7T4		C18	A24	DQ2T12	DQ1T12
B3	VREF1B3	IO	DQ7T5		B18	B24	DQ2T13	DQ1T13
B3	VREF1B3	IO				B30		
B3	VREF1B3	IO	DQ7T6		D18	C24	DQ2T14	DQ1T14
B3	VREF1B3	IO	DQ7T7		E18	D24	DQ2T15	DQ1T15
B3	VREF1B3	IO				M23		
B3	VREF2B3	IO				C30		
B3	VREF2B3	IO	DQ8T0		C19	A25	DQ3T0	DQ1T16

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
B3	VREF2B3	IO	DQ8T1		D19	B25	DQ3T1	DQ1T17
B3	VREF2B3	IO				F27		
B3	VREF2B3	IO	DQ8T2		A18	C25	DQ3T2	DQ1T18
B3	VREF2B3	IO	DQS8T		B19	D25	DQS3T	
B3	VREF2B3	IO				E28		
B3	VREF2B3	IO	DQ8T3		B20	A26	DQ3T3	DQ1T19
B3	VREF2B3	IO	DQ8T4		A20	E25	DQ3T4	DQ1T20
B3	VREF2B3	IO				E29		
B3	VREF2B3	IO	DQ8T5		A19	B26	DQ3T5	DQ1T21
B3	VREF2B3	IO	DQ8T6		C20	C26	DQ3T6	DQ1T22
B3	VREF2B3	VREF2B3			J18	M21		
B3	VREF2B3	IO	DQ8T7		D20	D26	DQ3T7	DQ1T23
B3	VREF2B3	IO			H18	C31		
B3	VREF2B3	IO				D30		
B3	VREF2B3	IO	DQ9T0		A21	A27	DQ3T8	DQ1T24
B3	VREF2B3	IO				L23		
B3	VREF2B3	IO	DQ9T1		B21	B27	DQ3T9	DQ1T25
B3	VREF2B3	IO				B31		
B3	VREF2B3	IO	DQ9T2		C21	C27	DQ3T10	DQ1T26
B3	VREF2B3	IO	DQS9T		B22	A28		
B3	VREF2B3	IO				F28		
B3	VREF2B3	IO	DQ9T3		C22	B28	DQ3T11	DQ1T27
B3	VREF2B3	IO				F29		
B3	VREF2B3	IO	DQ9T4		A22	C28	DQ3T12	DQ1T28
B3	VREF2B3	IO	DQ9T5		B23	A29	DQ3T13	DQ1T29
B3	VREF2B3	IO	DQ9T6		A23	B29	DQ3T14	DQ1T30
B3	VREF2B3	IO				E30		
B3	VREF2B3	IO	DQ9T7		B24	C29	DQ3T15	DQ1T31
B3	VREF2B3	IO				F30		
		GXB_GND						
		GND						
		VCCIO2			C26	C32		
		VCCIO2			M26	N23		
		VCCIO2			N18	R32		
		VCCIO2				T24		
		VCCIO1			AD26	AK32		
		VCCIO1			P18	V32		
		VCCIO1			R26	U23		
		VCCIO1				Y23		
		VCCIO8			AF15	AM19		
		VCCIO8			AF24	Y19		
		VCCIO8			T14	AM30		
		VCCIO8				Y21		
		VCCIO7			AF3	AF7		
		VCCIO7			AF12	AM16		
		VCCIO7			T12	AM12		
		VCCIO7				U11		
		VCCIO4			A3	A13		
		VCCIO4			A12	A16		
		VCCIO4			L12	G7		
		VCCIO4				T11		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
		VCCIO3			A15	A19		
		VCCIO3			A24	A30		
		VCCIO3			L13	N19		
		VCCIO3				N21		
		VCCP_B14				M9		
		VCCP_B14				N9		
		VCCP_B14			L8	P9		
		VCCP_B14			M8	R9		
		VCCP_B15			R8	W9		
		VCCP_B15			T8	Y9		
		VCCP_B15				AA9		
		VCCP_B15				AB9		
		VCCR_B14				M8		
		VCCR_B14				N8		
		VCCR_B14			L7	P8		
		VCCR_B14			M7	R8		
		VCCR_B15			R7	W8		
		VCCR_B15			T7	Y8		
		VCCR_B15				AA8		
		VCCR_B15				AB8		
		VCCT_B14				M7		
		VCCT_B14				N7		
		VCCT_B14			L6	P7		
		VCCT_B14			M6	R7		
		VCCT_B15			R6	W7		
		VCCT_B15			T6	Y7		
		VCCT_B15				AA7		
		VCCT_B15				AB7		
		VCCINT			AB6	R15		
		VCCINT			N9	P19		
		VCCINT			Y6	U15		
		VCCINT			F6	V15		
		VCCINT			N11	W22		
		VCCINT			H6	AG12		
		VCCINT			N13	P22		
		VCCINT			L11	T17		
		VCCINT			P12	V21		
		VCCINT			L9	P15		
		VCCINT			N16	R21		
		VCCINT			M10	U18		
		VCCINT			P16	W20		
		VCCINT			K6	F11		
		VCCINT			N15	R18		
		VCCINT			M9	T21		
		VCCINT			P14	W16		
		VCCINT			L10	AG10		
		VCCINT			P10	P21		
		VCCINT			M14	T15		
		VCCINT			V6	V19		
		VCCINT				F13		
		VCCINT				R20		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
		VCCINT				U16		
		VCCINT				W18		
		VCCINT				W15		
		VCCINT				P20		
		VCCINT				T9		
		VCCINT				V17		
		VCCINT				U21		
		VCCINT				F9		
		VCCINT				R16		
		VCCINT				T19		
		VCCINT				V22		
		VCCINT				P17		
		VCCINT				R22		
		VCCINT				U20		
		VCCINT				W21		
		GXB_GND			AA3	A2		
		GXB_GND			D2	AB4		
		GXB_GND			H4	AE2		
		GXB_GND			M3	AH3		
		GXB_GND			T2	AJ6		
		GXB_GND			Y1	AK9		
		GXB_GND			AB2	AL10		
		GXB_GND			F1	C1		
		GXB_GND			J3	C12		
		GXB_GND			M5	E9		
		GXB_GND			T4	H4		
		GXB_GND			Y3	L2		
		GXB_GND			AB4	R1		
		GXB_GND			F3	V5		
		GXB_GND			K2	A11		
		GXB_GND			P1	AD3		
		GXB_GND			U3	AF5		
		GXB_GND			Y5	AH10		
		GXB_GND			AD1	AK5		
		GXB_GND			F5	AL3		
		GXB_GND			K4	B3		
		GXB_GND			P3	C6		
		GXB_GND			V2	D11		
		GXB_GND			D1	F6		
		GXB_GND			H1	J3		
		GXB_GND			L3	N1		
		GXB_GND			P5	T5		
		GXB_GND			V4	Y4		
		GXB_GND			H3	A7		
		GXB_GND			M2	AC2		
		GXB_GND			T1	AF3		
		GXB_GND			W3	AH6		
		GXB_GND			AB1	AK3		
		GXB_GND			E3	AL1		
		GXB_GND			H5	AM8		
		GXB_GND			M4	C4		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
		GXB_GND			T3	D7		
		GXB_GND			Y2	F4		
		GXB_GND			AB3	J1		
		GXB_GND			F2	M4		
		GXB_GND			K1	T3		
		GXB_GND			N3	W3		
		GXB_GND			T5	AA3		
		GXB_GND			Y4	AE1		
		GXB_GND			AB5	AG3		
		GXB_GND			F4	AJ3		
		GXB_GND			K3	AK8		
		GXB_GND			P2	AL8		
		GXB_GND			V1	B9		
		GXB_GND			AD2	C9		
		GXB_GND			G3	E3		
		GXB_GND			K5	G3		
		GXB_GND			P4	K4		
		GXB_GND			V3	P3		
		GXB_GND			H2	U3		
		GXB_GND			M1	A5		
		GXB_GND			R3	AC1		
		GXB_GND			V5	AE6		
		GXB_GND				AH5		
		GXB_GND				AJ10		
		GXB_GND				AK11		
		GXB_GND				AM6		
		GXB_GND				C3		
		GXB_GND				D5		
		GXB_GND				F3		
		GXB_GND				H6		
		GXB_GND				M3		
		GXB_GND				R3		
		GXB_GND				W2		
		GXB_GND				AA2		
		GXB_GND				AD5		
		GXB_GND				AG2		
		GXB_GND				AJ2		
		GXB_GND				AK7		
		GXB_GND				AL6		
		GXB_GND				B7		
		GXB_GND				C8		
		GXB_GND				E2		
		GXB_GND				G2		
		GXB_GND				K3		
		GXB_GND				N3		
		GXB_GND				U2		
		GXB_GND				V4		
		GXB_GND				A3		
		GXB_GND				AB5		
		GXB_GND				AE3		
		GXB_GND				AH4		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
		GXB_GND				AJ8		
		GXB_GND				AK10		
		GXB_GND				AM4		
		GXB_GND				C2		
		GXB_GND				D3		
		GXB_GND				E11		
		GXB_GND				H5		
		GXB_GND				L3		
		GXB_GND				R2		
		GXB_GND				W1		
		GXB_GND				AA1		
		GXB_GND				AD4		
		GXB_GND				AG1		
		GXB_GND				AJ1		
		GXB_GND				AK6		
		GXB_GND				AL4		
		GXB_GND				B5		
		GXB_GND				C7		
		GXB_GND				E1		
		GXB_GND				G1		
		GXB_GND				J6		
		GXB_GND				N2		
		GXB_GND				U1		
		GXB_GND				Y5		
		GXB_GND				A9		
		GXB_GND				AC3		
		GXB_GND				AF4		
		GXB_GND				AH8		
		GXB_GND				AK4		
		GXB_GND				AL2		
		GXB_GND				AM10		
		GXB_GND				C5		
		GXB_GND				D9		
		GXB_GND				F5		
		GXB_GND				J2		
		GXB_GND				M5		
		GXB_GND				T4		
		GXB_GND				Y3		
		GXB_GND				AB3		
		GXB_GND				B11		
		GXB_GND				C10		
		GXB_GND				E5		
		GXB_GND				G6		
		GXB_GND				K5		
		GXB_GND				P4		
		GXB_GND				V3		
		GXB_GND				C11		
		GXB_GND				E7		
		GXB_GND				H3		
		GXB_GND				L1		
		GXB_GND				P5		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
		GND			A2	A20		
		GND			AF2	AL12		
		GND			L26	D13		
		GND			P13	P18		
		GND			AA6	T22		
		GND			B1	AG8		
		GND			N10	AG9		
		GND			R14	AM31		
		GND			A16	F10		
		GND			AF16	R19		
		GND			M12	U19		
		GND			P17	Y20		
		GND			AD3	AG6		
		GND			D3	AL32		
		GND			N14	F7		
		GND			U6	AF6		
		GND			A11	AE7		
		GND			AF11	W19		
		GND			M11	AH12		
		GND			P15	B16		
		GND			AC3	N20		
		GND			B26	T16		
		GND			N12	V16		
		GND			T26	Y24		
		GND			A25	A31		
		GND			AF25	AL16		
		GND			M13	E13		
		GND			R12	P32		
		GND			AE1	U10		
		GND			G6	W17		
		GND			N17	AG11		
		GND			W6	B13		
		GND			AE26	F12		
		GND			J6	T10		
		GND			P11	U22		
		GND				Y22		
		GND				AG7		
		GND				AM20		
		GND				F8		
		GND				R17		
		GND				U17		
		GND				W32		
		GND				AJ12		
		GND				B32		
		GND				N22		
		GND				T18		
		GND				V18		
		GND				P16		
		GND				AK12		
		GND				C13		
		GND				N24		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
		GND				T20		
		GND				V20		
		NC				AA16		
		NC				AD27		
		NC				K26		
		NC				P1		
		NC				U5		
		NC				V9		
		NC				AB16		
		NC				AJ32		
		NC				L16		
		NC				R4		
		NC				U7		
		NC				W5		
		NC				AC26		
		NC				D32		
		NC				M2		
		NC				R23		
		NC				U9		
		NC				Y2		
		NC				AD17		
		NC				J26		
		NC				M22		
		NC				T2		
		NC				V1		
		NC				AA19		
		NC				AJ31		
		NC				K27		
		NC				P2		
		NC				U6		
		NC				W4		
		NC				AC16		
		NC				D31		
		NC				M1		
		NC				R5		
		NC				U8		
		NC				Y1		
		NC				AC27		
		NC				J17		
		NC				M16		
		NC				T1		
		NC				U24		
		NC				Y12		
		NC				AD26		
		NC				J27		
		NC				N4		
		NC				T6		
		NC				V2		
		NC				U4		
		NC				V8		
		NC				N16		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F672	F1020	DQS for x16	DQS for x32
		NC				T23		
		NC				V7		
		NC				K16		
		NC				N5		
		NC				T7		
		NC				V6		

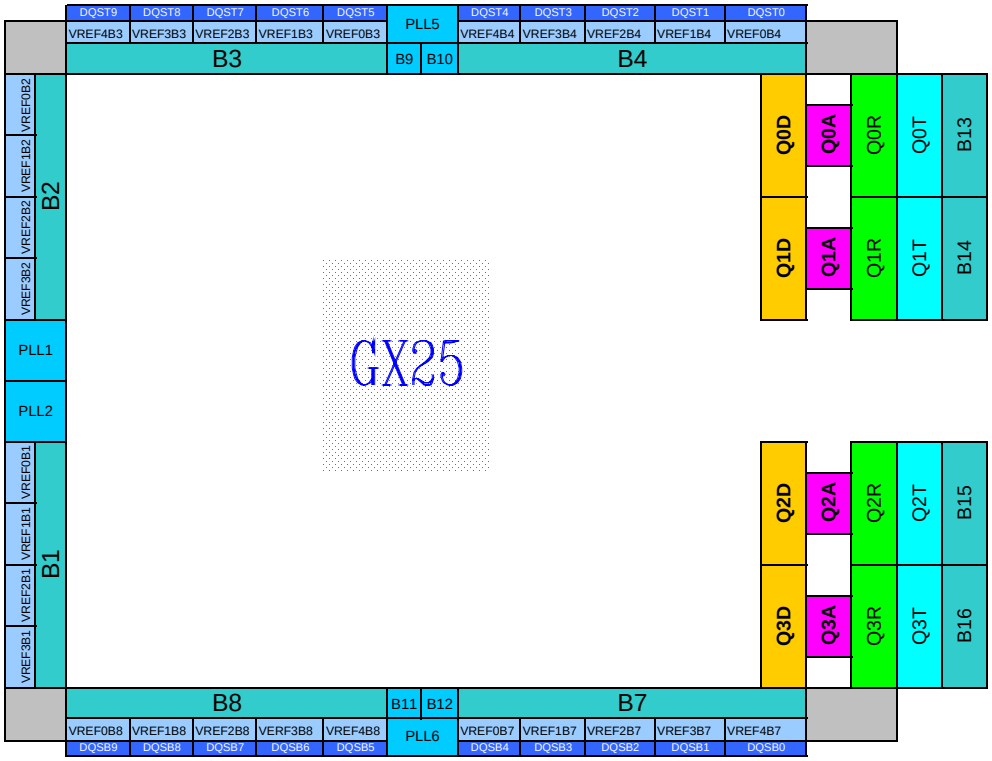
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..4,7,8]	Input	Input reference voltage for banks. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, they should be connected to Gnd.
VCCIO[1..4]B[1..4,7,8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These power pins are supplied with a 1.5V source. These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1,2,5,..,8,11,12]	Power	Analog power for PLLs[1,2,5,..,8,11,12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1,2,5,..,8,11,12]	Ground	Analog ground for PLLs[1,2,5,..,8,11,12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1,2,5,..,8,11,12]	Power	Guard ring power for PLLs[1,2,5,..,8,11,12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1,2,5,..,8,11,12]	Ground	Guard ring ground for PLLs[1,2,5,..,8,11,12]. The designer can connect this pin to the GND plane on the board.
GXB_GND	Ground	Transceiver Power Ground. These ground pins need to be connected to a ground island plane isolated from noisy digital ground.
GND	Ground	These ground pins need to be connected to digital ground. The digital ground is used for VCCINT and VCCIO return current.
NC	No Connect	These pins should be left unconnected.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
		Clock and PLL Pins
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Dedicated fast regional clock pins. FCLK pins can also be used as input, output, or bidirectional pins.
CLK[15..12]p	Input	Dedicated global clock inputs 12 to 15.
CLK[15..12]n	I/O, Input	Negative terminal input for differential global clock input. May also be used as regular I/O
CLK[7..0]p	Input	Dedicated global clock inputs 0 to 7.
CLK[7, 6, 5, 4, 3, 1]n	I/O, Input	Negative terminal input for differential global clock input. Or may be used as a regular I/O pin.
CLK[2, 0]n	Input	Dedicated negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	External clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). May also be used as regular I/O
PLL6_OUT[3..0]n	I/O, Output	Negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. May also be used as regular I/O
PLL5_OUT[3..0]p	I/O, Output	External clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). May also be used as regular I/O
PLL5_OUT[3..0]n	I/O, Output	Negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. May also be used as regular I/O
		Optional/Dual-Purpose Pins
DIFFIO_RX[44..0]p	Input	High speed source synchronous differential I/O receiver channels 0 to 44. Pins with an p suffix carry the positive signal for the differential channel If not used, these pins are dedicated input pins.
DIFFIO_RX[44..0]n	Input	This pin is the complementary signal of the differential inputs. If not used for the differential pair, these pins are dedicated input pins. Pins with an n suffix carry the negative signal for the differential channel.
DIFFIO_TX[44..0]p	I/O, Output	Dual-purpose source synchronous high speed differential I/O transmitter channels 0 to 44. Pins with an p suffix carry the positive signal for the differential channel. If not used, these pins are regular I/O pins.
DIFFIO_TX[44..0]n	I/O, Output	This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
DATA[7..0]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..7],RUP[4..1]	I/O, Input	Reference pins for banks 8,7,4,3,2,1 The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..7],RDN[4..1]	I/O, Input	Reference pins for banks 8,7,4,3,2,1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Pin Definitions Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/ O pin.
		GX (I/O banks 13 to 17) Pins
VCCP_B[17..13]	VCC	GX bank [17..13] digital power. This power is connected to 1.5V.
VCCR_B[17..13]	VCC	GX bank [17..13] receiver power. This power is connected to 1.5V.
VCCT_B[17..13]	VCC	GX bank [17..13] transmitter power. This power is connected to 1.5V.
VCCG_B[17..13]	VCC	GX bank[17..13] guard ring power. This power is connected to 1.5V.
VCCA_B[17..13]	VCC	GX bank [17..13] analog power. This power is connected to 3.3V.
GXB_RX[19..0]n	I, Input	High speed differential I/O receiver channels negative. Connect any of these unused pins to ground through a 10K ohm resistor.
GXB_RX[19..0]p	I, Input	High speed differential I/O receiver channels positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
GXB_TX[19..0]n	O,Output	High speed differential I/O transmitter channels negative. Connect any of these unused pins to ground through a 10K ohm resistor.
GXB_TX[19..0]p	O,Output	High speed differential I/O transmitter channels positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
REFCLKB[17..13]n	I, Input	High speed differential I/O reference clock negative. Connect any of these unused pins to ground through a 10K ohm resistor.
REFCLKB[17..13]p	I, Input	High speed differential I/O reference clock positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
RREFB[17..13]	I, Input	Reference resistor for Gx side banks. Should be connected to a 2K of a tolerance of 1% to ground. In the PCB layout the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
RREFB[15,14]A	I, Input	Reference resistor for Gx side banks. Should be connected to a 2K of a tolerance of 1% to ground. In the PCB layout the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Notes:
1.This is a top view of the silicon die.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

PLL Numbering and PowerBank & Vref Arrangement



Device Name	GX Bank # Utilized
EP1SGX25C	15
EP1SGX25D	14 & 15
EP1SGX25F	13,14,15,16

Power

Power Description	Flip Chip		Notes
	Global Power on Die	Pkg route	
Left, Top, and Bottom Power and Ground are the same as Stratix Devices			
EPLL clock output power	VCC_CLKOUT[0:7]	isolated	
EPLL clock output power			
EPLL clock output ground	VSSN	VSSN plane	VSSN
EPLL clock output ground	VCCN[4,7]	VCCN[4,7]plane	
EPLL clock output ground	VSSN	VSSN plane	
PLL analog power	VCCA[1:2, 5:8, 11:12]	isolated	VCCA[3:4,9:10]
PLL analog ground	VSSA[1:2, 5:8, 11:12]	isolated	VSSA[3:4,9:10]
PLL digital power	VCC[1:2, 5:8, 11:12]	VCC plane	It is shorted to VCC in the package of the flip chip.
PLL digital ground	VSS[1:2, 5:8, 11:12]	VSS plane	It is shorted to VSS in the package of the flip chip.
PLL guard ring power	VCCG[1:2, 5:8, 11:12]	isolated	
PLL guard ring ground	VSSG[1:2, 5:8, 11:12]	isolated	
Noisy power	VCCN[1:4,7:8]	VCCN[1:4,7:8] plane	
Noisy ground	VSSN	VSS plane	
Quiet power	VCC	VCC plane	
Quiet ground	VSS	VSS plane	
HSSI Global Power: Power and Ground are grouped in QUAD. Quad Order is 0,1,4,2,3			
	Marketing		
HSSI digital power (1.5 v)	VCCP0		Each Quad has 5 bumps connected to 2 isolated digital power balls
	VCCP1		
	VCCP4		
	VCCP2		
	VCCP3		
HSSI RX power (1.5 v)	VCCR[0:3]		Each Quad has 4 bumps connected to 1 isolated RX power ball
	VCCR[4:7]		
	VCCR[16:19]		
	VCCR[8:11]		
	VCCR[12:15]		
HSSI TX power (1.5 v)	VCCT[0:3]		Each Quad has 4 bumps connected to 1 isolated TX power ball
	VCCT[4:7]		
	VCCT[16:19]		
	VCCT[8:11]		
	VCCT[12:15]		
HSSI CMU power (1.5 v)	VCCM0		VCCM# bump shares power with VCCT# of the same QUAD There are no pin associated with this pin name since they share the same bump power with VCCT# of the same Quad
	VCCM1		
	VCCM4		
	VCCM2		
	VCCM3		
HSSI Analog power (3.3 v)	VCCAQ0		Each Quad has its own analog power. One bump--> one ball Provides power to Tx PLL and some biasing circuit
	VCCAQ1		
	VCCAQ4		
	VCCAQ2		
	VCCAQ3		
HSSI VCCG (1.5 v)	VCCGQ0		Each Quad has its own VCCG power. One bump--> one ball Guard ring for TX PLL should be used to isolate noise to TX pll
	VCCGQ1		
	VCCGQ4		
	VCCGQ2		
	VCCGQ3		
HSSI substrate ground	VSSASUB0		Each Quad has its own substrate ground. One bump--> one ball
	VSSASUB1		
	VSSASUB4		
	VSSASUB2		
	VSSASUB3		
HSSI digital ground	DGND		All digital grounds are connected to the HSSI ground plane at package level
	DGND		
	DGND		
	DGND		
	DGND		
HSSI TX/RX ground	HGND		All TX/RX grounds are connected to the HSSI ground plane at package level
	HGND		
	HGND		
	HGND		
	HGND		
HSSI CMU ground	CGND		All CMU grounds are connected to the HSSI ground plane at package level

	CGND		
	CGND		
	CGND		
	CGND		
Global Power on Die is the signal name that the schematics and layout use for this power or ground			
Pkg Route: 1) plane = indicates the power plane the bump/pad routes to in the pkg;			
2) isolated = indicates the bump/pad is routed to the pkg ball without connect to any other pkg route or plane.			
Plane: A plane has multiple bump/pads connected to it which in turn connect to multiple balls. It does not			
necessarily imply a complete sheet of conductor; it may look be more like Swiss cheese.			
Net: Multiple bumps/balls can share the same net bus			

Non-Migratable IO Pins

Non-Migratable IO Pins	
1020FBGA (EP1SGX40 <--> EP1SGX25)	672FBGA (EP1SGX25 <-->EP1SGX10)
AA23	
AB23	
AC23	
AD23	
AG25	
AG26	
AH27	
AH28	
AH29	
AH30	
AJ29	
AJ30	
D29	
D30	
E29	
E30	
F27	
F28	
F29	
F30	
J23	
K23	
L23	
M23	

Device Part Numbers					
Name	Number of Fast PLL	Device Pin Count	# of Receiver Chs	# of Transmitter Chs	Speed (Mbps)
EP1SGX10C	2	672	22	22	1000
EP1SGX10D	2	672	22	22	1000
EP1SGX25C	2	672	39	39	1000
EP1SGX25D	2	672 / 1020	39	39	1000
EP1SGX25F	2	1020	39	39	1000
EP1SGX40D	4	1020	45	45	1000
EP1SGX40G	4	1020	45	45	1000

Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mpbs

Device Part Numbers	I/O Count [1]	
Name	672-Pin FineLine BGA	1,020 Pin FineLine BGA
EP1SGX10C	330	
EP1SGX10D	330	
EP1SGX25C	426	
EP1SGX25D	426	542
EP1SGX25F		542
EP1SGX40D		548
EP1SGX40G		548

Note 1 : The total number of I/O pins for each package described above include dedicated clock pins, and dedicated fast I/O pins. However it does not include High-Speed or the Clock Referance pins for High Speed I/O.

What	Comment	Date
Added voltage value to power pins	rev 1.2	10/15/2002
Added information to the VCCM , they share the same bump with VCCT.	rev 1.3	12/17/2002
Added Non-Migrateble pins	rev 1.3	12/17/2002
Added I/O pin count	rev 1.3	12/17/200
Added info regarding RREF pin	rev 1.3	1/10/2003
Sent to Product Marketing	rev 1.3	2/19/2003
Connected NC pins to RREF pins(NOTE 1)	rev 1.4	5/30/2003
Connected NC pins to VCCx_Bxx (NOTE 1)	rev 1.4	5/30/2003
Connected unused NC pins on the HSSI side to GND. These pins are listed as NC/GND in this document and are listed as GND* in Quartus II software (NOTE 1 and 2)	rev 1.4	5/30/2003
Added pin status change information from rev 1.3 to rev 1.4. Pin changes are for EP1SGX10C, EP1SGX25C,EP1SGX25D,EP1SGX40 D only.	rev 1.4	5/30/2003
Added section for 1SGX25C missing from 1.4. Changed DATA0 to be an IO after configuration.	rev 1.42	7/30/2003
Note 1: Modifications in Rev 1.4 are recommendations for noise reduction. Do NOT make modifications to the board already laid out based on pin table Rev 1.3 . It is recommended that the pin table Rev 1.4 be implemented for new designs or re-designed boards only.		
NOTE 2 : GND/NC is shown as GND* in Quartus II software		
Add HSSI_GND to the pin list	rev 1.43	9/10/2003
Wrong Bank was referenced in the GX25C device	rev 1.44	9/11/2003
Update non-migration table	rev 1.45	9/17/2003
change all references of GX_TX, GX_RX to GXB_TX, GXB_RX		
Change all references of HSSI_GND to GXB_GND		
Change pin description data[7..1] to include data0		
Changed false references of RUP/RDN to different banks		
Updated pin description so only CLK0n and CLK2n were		
dedicated clock inputs. While the rest were also I/Os		
Updated pin description of VCCINT to expliciltly say it needs a		
1.5V supply		
Updated the pin description for PLLENA		
Update pin description to explain what to do with unused pins	rev 1.46	9/19/2003
for the transceivers and REFCLKB.		
Definition for RUnLU needed to be updated to correctly indicate poarity of signal for remote and local update. Also the pin definitions for GND and NC were added to the pin definition.	rev 1.47	10/21/2003
Updated pin descriptions for items 74 though 78 of the pin descriptions. These describe the VCC voltages and the pin description was updated with more specific information as to what voltage to connect them to.		
Item 42 in the pin desription was updated to specify that the CLK[15..12]p pins are dedicated input clock pins		
Item 43 in the pin desription was updated to specify that the CLK[15..12]n pins are either clock inputs or regular I/O	rev 1.48	12/11/2003
Item 47 through 50 which describe the PLL_OUT pins are updated to specify that they can be used as either I/O or Output		
Items 80 through 83 was updated to describe the termination of the unused pins for GX_RX and GX_TX.		

Items 85 and 86 was updated to describe the termination of the unused pins for REFCLK.		
Updated description for unused VREF pins so the it reads the same description as Quartus II	rev 1.49	3/17/2004
Updated description for RREFB. Layout guidelines were added.	rev 1.50	6/2/2004
Updated RREFB pins to address new Quartus change (please refer to the "RREFB pin change in 1.6" worksheet)		
Deleted DQS for x16 column in EP1SGX10C & EP1SGX10D pin-list	rev 1.60	4/27/2005
Created pin definition for RREFB[15,14]A		
Added CRC_ERROR pins in pin list	rev 1.70	2/22/2006

EP1SGX25D.Change in 1.4			
1020 Package	Status in Rev 1.3	Pin name	Status in Rev 1.4
No change to 672 pakcage	NC	AL11	GND/NC
	NC	AM11	GND/NC
	NC	AH11	GND/NC
	NC	AJ11	GND/NC
	NC	AL9	GND/NC
	NC	AM9	GND/NC
	NC	AH9	GND/NC
	NC	AJ9	GND/NC
	NC	AD6	VCCA_B15
	NC	AL7	GND/NC
	NC	AM7	GND/NC
	NC	AC6	VCCG_B15
	NC	AB6	GND
	NC	AC7	RREFB15
	NC	AL5	GND/NC
	NC	AM5	GND/NC
	NC	AH7	GND/NC
	NC	AJ7	GND/NC
	NC	AM3	GND/NC
	NC	AM2	GND/NC
	NC	AJ5	GND/NC
	NC	AJ4	GND/NC
	NC	B4	GND/NC
	NC	A4	GND/NC
	NC	E6	GND/NC
	NC	D6	GND/NC
	NC	B6	GND/NC
	NC	A6	GND/NC
	NC	E8	GND/NC
	NC	D8	GND/NC
	NC	M6	VCCA_B14
	NC	B8	GND/NC
	NC	A8	GND/NC
	NC	K6	VCCG_B14
	NC	L6	GND
	NC	J7	RREFB14
	NC	B10	GND/NC
	NC	A10	GND/NC
	NC	E10	GND/NC
	NC	D10	GND/NC
	NC	B12	GND/NC
	NC	A12	GND/NC
	NC	E12	GND/NC
	NC	D12	GND/NC
	NC	M9	VCCP_B14
	NC	N9	VCCP_B14
	NC	AA9	VCCP_B15
	NC	AB9	VCCP_B15
	NC	M8	VCCR_B14
	NC	N8	VCCR_B14
EP1SGX25D.Change in 1.4	NC	AA8	VCCR_B15
	NC	AB8	VCCR_B15
	NC	M7	VCCT_B14
	NC	N7	VCCT_B14

	NC	AA7	VCCT_B15
	NC	AB7	VCCT_B15

RREFB pin change in 1.6				
	Device	Status in Rev 1.5	Pin name	Status in Rev 1.6
	EP1SGX10CF672	RREFB15	U7	RREFB15A
		RREFB15	K7	RREFB15
	EP1SGX25CF672	RREFB15	U7	RREFB15
		RREFB15	K7	RREFB15A
	EP1SGX25DF1020	RREFB14	L7	RREFB14
		RREFB14	J7	RREFB14A
		RREFB15	AC7	RREFB15A
		RREFB15	T8	RREFB15
	EP1SGX40DF1020	RREFB14	J7	RREFB13
		RREFB15	AC7	RREFB16
		RREFB15	T7	GND/NC
		RREFB15	T8	RREFB15
		RREFB14	L7	RREFB14