Stratix® IV GT Device Family Pin Connection Guidelines
PCG-01006-1.8

These pin connection guidelines should only be used as a recommendation, not as a specification.
The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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You should create a Quartus II design, enter your device I/O assignments and compile the design. The Quartus II software will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Stratix IV GT Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins			
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND. See Note 8.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND. See Note 8.
CLK[4:7,12:15]p (CLK[9,11]p are single ended only)	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.	When unused these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.	When unused these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[L4,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L4 and R4 respectively. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND. See Note 8.
PLL_[L4,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L4 and R4 respectively. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND. See Note 8.
PLL_[L1, L2, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND. See Notes 11 and 17.
PLL_[L1, L2, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock		When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND. See Notes 11 and 17.
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	When unused these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock		When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock		When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Configuration/JTAG Pins ***(See Note 12)***			
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[0:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.	The nIO-PULLUP can be tied directly to VCCPGM, use a 1-kΩ pull-up resistor or tied directly to GND depending on the use desired for the device. Refer to the description column.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.	If the temperature sensing diode is not connected to an external temperature sense device, then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.	If the temperature sensing diode is not connected to an external temperature sense device, then connect this pin to GND.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.	These pins are internally connected through a 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to VCCPGM or GND. Refer to the "Configuring Stratix IV Devices" chapter in the Stratix IV Handbook. If only JTAG configuration is used, connect these pins to ground.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the nINIT_CONF pin of the configuration device. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to VCCPGM.

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Stratix IV GT Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin. When using EPC2 devices, only external 10-kΩ pull-up resistor to VCCPGM should be used.
nCEO	Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds the nCE pin of a subsequent device. During single device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	The OE and nCE pins of the enhanced configuration devices and EPC2 devices have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up should not be used on these pins. For EPC2 devices, only external 10-kΩ pull-up resistors to VCCPGM should be used.
PORSEL	Input	Dedicated input which selects between a POR time of 4 - 12 ms or 100 - 300 ms. A logic high (1.8V, 2.5V, 3.0V) selects a POR time of 4 - 12 ms and a logic low selects POR time of 100 - 300 ms.	The PORSEL pin should be tied directly to VCCPGM or GND.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND. See Note 18.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TMS to VCCPD via a 1-kΩ resistor. See Note 18.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TDI to VCCPD via a 1-kΩ resistor. See Note 18.
TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected. See Note 18.
TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When using this pin ensure that TMS is held high or TCK is static when TRST is changed from low to high. If not using TRST, tie this pin to a 1-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry, tie this pin to GND. See Note 18.
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode nCSO is not used. Also, when this pin is not used as an output, you should leave the pin unconnected.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.	When not programming the device in AS mode ASDO is not used. Also, when this pin is not used as an output, then you should leave the pin unconnected.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	I/O, Output open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.
DEV_CLRn	Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	When the dedicated input DEV_CLRn is not used, tie this pin to GND.
DEV_OE	Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used, tie this pin to GND.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	When the dedicated input for DATA[0] is not used and this pin is not used as an I/O, leave this pin unconnected.
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. Except for DATA2, DATA6, and DATA7, these pins can also be used as user I/O pins after configuration.	When the dedicated inputs for DATA[1:7] are not used and these pins are not used as an I/O, leave these pins unconnected. DATA2, DATA6, and DATA7 cannot be used as I/O.

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Stratix IV GT Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.
CLKUSR	Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices.	If the CLKUSR pin is not used as a configuration clock input, you should connect this pin to GND.
Differential I/O Pins (See Note 13)			
DIFFIO_RX[#:#]p, DIFFIO_RX[#:#]n	I/O, RX channel	These are true LVDS receiver channels on row and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. True LVDS receivers on row I/O pins support OCT Rd, and true LVDS receivers on column I/O pins do not support OCT Rd.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DIFFIO_TX[#:#]p, DIFFIO_TX[#:#]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DIFFOUT_[#:#]p, DIFFOUT_[#:#]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
External Memory Interface Pins (Note 9, 12, and 13)			
DQS[#:#][T,B], DQS[#:#][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DQSn[#:#][T,B], DQSn[#:#][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
DQ[#:#][T,B], DQ[#:#][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CQ[#:#][T,B], CQ[#:#][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CQn[#:#][T,B], CQn[#:#][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	When unused, these pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Reference Pins			
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to the VCCIO of the bank in which the RUP pin resides or GND. When using OCT tie these pins to the required banks VCCIO through either a 25 Ω or 50 Ω resistor, depending on the desired I/O standard. Refer to the Stratix IV handbook for the desired resistor value for the I/O standard used. See Note 16.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT tie these pins to GND through either a 25 Ω or 50 Ω resistor depending on the desired I/O standard. Refer to the Stratix IV handbook for the desired resistor value for the I/O standard used. See Note 16.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.	Do not connect to power, ground or any other signal. These pins must be left floating.

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NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
Supply Pins ***(See Notes 7 and 14)***			
VCC	Power	VCC supplies power to the core and periphery.	All VCC pins require a 0.95 V supply. Use the Stratix IV Early Power Estimator to determine the current requirements for VCC and other power supplies. These pins may be tied to the same 0.95V plane as VCCHIP. With a proper isolation filter VCCD_PLL may be sourced from the same regulator as VCC. To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3, 6, and 14.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins even if the PLL is not used.	You are required to connect these pins to 0.95 V, even if the PLL is not used. With a proper isolation filter these pins may be sourced from the same regulator as VCC and/or VCCHIP. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCPT	Power	Power supply for the programmable power technology.	Use an isolated linear 1.5 V power supply for these pins. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.	You are required to connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear supply. With a proper isolation filter these pins may be sourced from the same linear regulator as VCCAUX. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCAUX	Power	Auxiliary supply for the programmable power technology.	Connect these pins to an isolated 2.5 V linear power supply. With a proper isolation filter these pins may be sourced from the same linear regulator as VCCA_PLL. To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.	Connect these pins to 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.0 V supplies, depending on the I/O standard connected to the specified bank. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCPD, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCPD as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCPGM	Power	Configuration pins power supply.	Connect this pin to either a 1.8 V, 2.5 V, or 3.0 V power supply. VCCPGM must ramp-up from 0V to VCCPGM within 100 ms when PORSEL is low or 4 ms when PORSEL is high to ensure successful configuration. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCIO and VCCPD, but only if each of these supplies require 2.5V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPD and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.	The VCCPD pins require a 2.5 V or 3.0 V power supply. VCCPD must ramp-up from 0V to VCCPD within 100 ms when PORSEL is low or 4 ms when PORSEL is high to ensure successful configuration. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCIO, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.	Connect these pins to 2.5 V power source. These pins may be tied to the same regulator as VCCIO, VCCPGM, and VCCPD, but only if each of these supplies require 2.5 V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 3.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	Connect this pin to a Non-volatile battery power source in the range of 1.2 V - 3.3 V when using design security volatile key. 3.0 V is the typical power selected for this supply. When not using the volatile key, tie this to a 3.0 V supply or GND. Do not share this source with other FPGA power supplies.
GND	Ground	Device ground pins.	All GND pins must be connected to the board ground plane.
VREF[1:8][A,C]N0, VREF[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 3.

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Stratix IV GT Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Transceiver Pins ***(See Notes 7 and 14)***			
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.	All VCCHIP_[L,R] pins require a 0.95 V supply. When not using HIP these pins may be connected to GND. These pins may be tied to the same 0.95 V plane as VCC. With a proper isolation filter these pins may be sourced from the same regulator as VCCD_PLL. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.	Connect VCCR_[L,R] to a 1.2 V linear regulator. These pins may be tied to the same 1.2 V plane as VCCT_[L,R] and/or VCCL_GXB[L,R] for data rates ≤ 6.5 Gbps. However, for better jitter performance this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 5, 6, and 15.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.	Connect VCCT_[L,R] to a 1.2 V linear regulator. These pins may be tied to the same 1.2 V plane as VCCR_[L,R] and/or VCCL_GXB[L,R] for data rates ≤ 6.5 Gbps. However, for better jitter performance this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 5, 6, and 15.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.	Connect VCCL_GXB[L,R][] to a 1.2 V linear regulator. These pins may be tied to the same 1.2 V plane as VCCT_[L,R] and/or VCCR_[L,R] for data rates ≤ 6.5Gbps. However, for better jitter performance this plane should be isolated from all other power supplies. For the best jitter performance, provide each quad its own power source. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 5, 6, 11, and 15.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers, specific to left (L) side and right (R) side.	Connect VCCH_GXB[L,R] to a 1.4 V linear regulator. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 5, 6, 10, 11, and 15.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.	Connect VCCA_[L,R] to a 3.3 V linear regulator. Decoupling depends on the design decoupling requirements of the specific board design. See Notes 3, 5, 6, and 15.
GXB_RX_[L,R][0:15]p	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. (Note 4) Connect all unused GXB_RXp pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 10 and 11.
GXB_RX_[L,R][0:15]n	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. (Note 4) Connect all unused GXB_RXn pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 10 and 11.
GXB_TX_[L,R][0:15]p	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating. See Notes 10 and 11.
GXB_TX_[L,R][0:15]n	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXn pins floating. See Notes 10 and 11.
REFCLK_[L,R][0:7]p, GXB_CMURX_[L,R][0:7]p	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.	These pins may be used for either reference clocks or CMU receiver channels. Switching between the two functions requires reprogramming the entire device. These pins should be AC-coupled when used as reference clocks (see Note 5). These pins may be AC-coupled or DC-coupled when used as CMU receiver channels (Note 4). Connect all unused GXB_CMURX_[L,R][]p/n pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 2 and 11.
REFCLK_[L,R][0:7]n, GXB_CMURX_[L,R][0:7]n	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.	These pins may be used for either reference clocks or CMU receiver channels. Switching between the two functions requires reprogramming the entire device. These pins should be AC-coupled when used as reference clocks (see Note 5). These pins may be AC-coupled or DC-coupled when used as CMU receiver channels (Note 4). Connect all unused GXB_CMURX_[L,R][]p/n pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 2 and 11.
GXB_CMUTX_[L,R][0:7]p, GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_CMUTX_[L,R][]p and GXB_CMUTX_[L,R][]n floating. See Notes 2 and Note 11.

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Stratix IV GT Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.	If any REFCLK pin or transceiver channel on one side (left or right) of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.00-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1) This pin connection guideline is created based on the Stratix IV GT EP4S40G2, EP4S100G2, EP4S100G3, EP4S100G4, EP4S40G5, and EP4S100G5.

2) Dual purpose CMU receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th transceiver channels.

3) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis Altera’s Power Distribution Network (PDN) design tool serves as an excellent decoupling analysis tool.
Power Distribution Network Design Tool

4) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel.

5) All transceiver power pins on the same side of the device must be connected either to the required supply or to GND. When ALL transceiver channels on the same side are unused, you have the option to connect all of the transceiver power pins on the same side of the device to GND or to the required supply.

6) Use the Stratix IV Early Power Estimator to determine the current requirements for VCC and other power supplies.

7) Example 1 and Figure 1 on the "Power Regs > 2.488 Gbps" tab below illustrate the minimum power supply regulator recommendations.

8) These clock pins are only available when transceivers on that side operate at or below 6.375 Gbps. Pins in this category have pin numbers that are appended with a single asterisk (*) in the pin table.

9) The DQS pins available depend on the device and the DQS mode (that is x4, x8/x9 or x18/x19) selected. Refer to the pin table for specific pin assignment. Many of the horizontal DQ/DQS pin are not available due to areas blocked for higher data rate performance. Designs requiring horizontal external memory access could be affected.

10) In Stratix IV GT devices, the 10 G transceivers are capable of operating anywhere in the range 600 Mbps to 11.3 Gbps.
- EP4S40G2 and EP4S40G5 have six 10 G transceivers (GXB_RX_[L,R][6:11] and GXB_TX_[L,R][6:11]) on each side, for a total of twelve 10 G transceivers per device. When using GXB_RX_[L,R][6:7] and GXB_TX_[L,R][6:7] at 10 G rates, VCCH_GXB[L,R][1] must be connected to 1.4 V.
- EP4S100G2 and EP4S100G5 in the 1517 package have twelve 10 G transceivers (GXB_RX_[L,R][0:11] and GXB_TX_[L,R][0:11]) on each side, for a total of twenty four 10 G transceivers per device.
- EP4S100G3 and EP4S100G4 in the 1932 package have twelve 10 G transceivers (GXB_RX_[L,R][4:15] and GXB_TX_[L,R][4:15]) on each side, for a total of twenty four 10 G transceivers per device.
- EP4S100G5 in the 1932 package has sixteen 10 G transceivers (GXB_RX_[L,R][0:15] and GXB_TX_[L,R][0:15]) on each side, for a total of thirty two 10 G transceivers per device.

11) The availability of these pins is device dependent. Refer to the pin tables to verify the availability of these pins for a given device.

12) Although some configuration pins may indicate that they serve as dual purpose (I/O and configuration) pins, this functionality is device dependent. Refer to the pin table of the specific device that you intend to use to determine which pins fit this category. Pins in this category have pin numbers that are appended with a two asterisks (**) in the pin table.

13) Although some differential pins may indicate that they serve as differential pins, this functionality is device dependent. Some pins in this category may have only one leg of the differential pair available. These pins may function as single-ended pins only. Refer to the pin table of the specific device that you intend to use to determine which pins fit this category. Pins in this category have pin numbers that are appended with a three asterisks (***) in the pin table.

14) Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via.

15) These supplies may share power planes across multiple Stratix IV GT devices.

16) RUP2A, RDN2A, RUP5A, RDN5A pins are not dual functionality pins. They can not be used as user I/O for the devices in the 1932 pin package.

17) PLL_R3_FB_CLKOUT0p, PLL_R3_CLKOUT0n pins are not available for the device in the 1932 pin package.

18) The JTAG pins TDI, TDO, TCK, TMS and TRST are powered by VCCPD1A.

19) Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components.
The switching frequency is usually between 800kHz and 1MHz and has fast transient response.
Line Regulation < 0.4%
Load Regulation < 1.2%

Example 1. Power Supply Sharing Guidelines for Data Rates Greater than 2.488 Gpbs

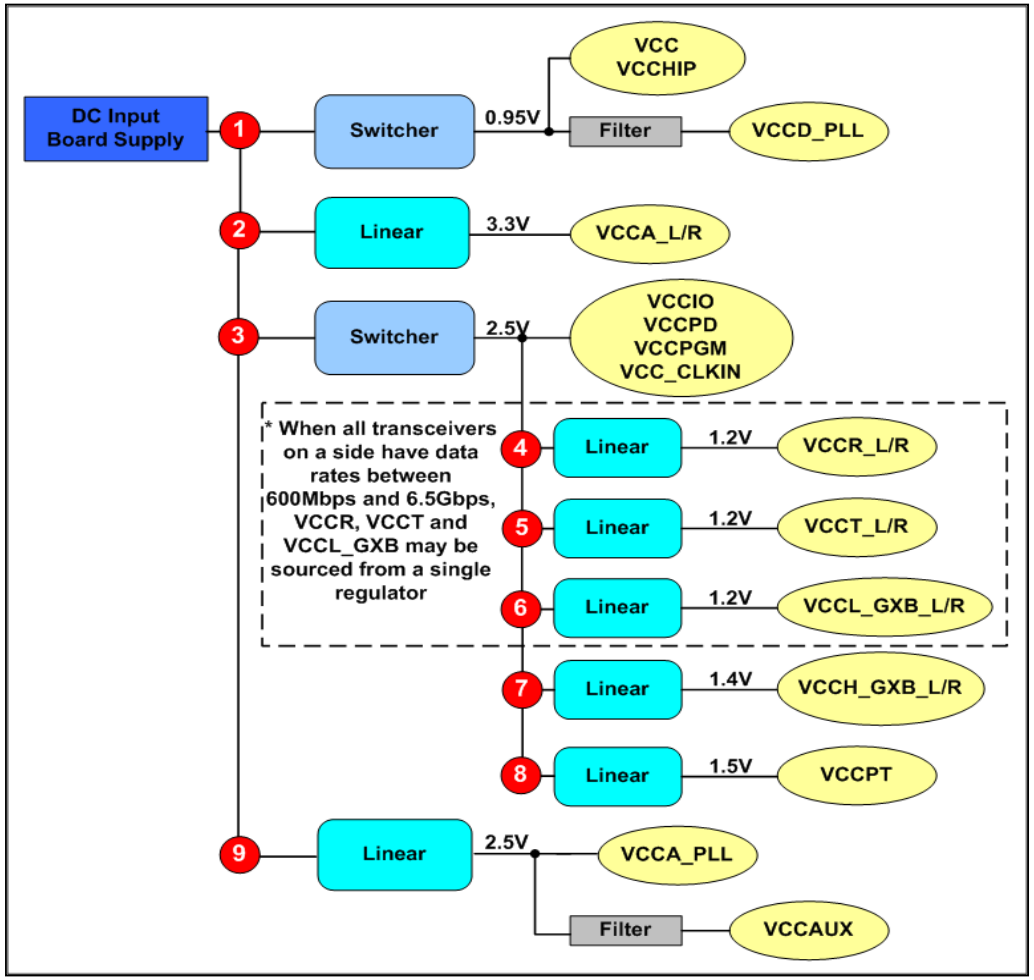
Example Requiring 9 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC**	1	0.95	± 30 mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND.
VCCHIP_[L,R]						
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCR_[L,R]*	2	1.2	± 50 mV	Linear	Isolate	The left [L] and [R] may share the same linear regulator. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV GT devices. Use the EPE (Early Power Estimation) tool within the Quartus II software to assist in determining the power required for your specific design.
VCCT_[L,R]*	3	1.2	± 50 mV	Linear	Isolate	The left [L] and [R] may share the same linear regulator. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV GT devices. Use the EPE (Early Power Estimation) tool within the Quartus II software to assist in determining the power required for your specific design.
VCCL_GXB[L,R][0:2]*	4	1.2	± 50 mV	Linear	Isolate	The left [L] and [R] may share the same linear regulator. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV GT devices. Use the EPE (Early Power Estimation) tool within the Quartus II software to assist in determining the power required for your specific design.
VCCH_GXB[L,R][0:2]	5	1.4	± 5%	Linear	Isolate	The left [L] and [R] may share the same linear regulator. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV GT devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCPT	6	1.5	± 50 mV	Linear	Isolate	
VCCA_[L,R]	7	3.3	± 4%	Linear	Isolate	Depending on the regulator capabilities, this supply may be shared with multiple Stratix IV GT devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCAUX **	8	2.5	± 5%	Linear	Isolate/share	VCCAUX and VCCA_PLL may be able to share a linear regulator with a proper isolation filter.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]						
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	9	Varies	± 5%	Switcher	Share if 2.5 V	If all of these supplies require 2.5 V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5 V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B						
VCCPGM						
VCC_CLKIN[3,4,7,8]C		2.5				

* Figure 1 shows an example for sharing 9 power regulators across both transceiver sides of the device and can be used for any data rate. If one side is designed for ≤ 6.5 Gbps then that side of the device may share the VCCR, VCCT, and VCCL_GXB power rails using a single regulator for that side. However, it is also acceptable to keep these rails separated if the board can accommodate this in the layout.
** To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram is provided in Figure 1.

Figure 1. Example Stratix IV GT Power Supplies Block Diagram for Data Rates > 2.488 Gbps



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Revision History

Revision	Description of Changes	Date
1.0	Initial Release.	7/17/2009
1.1	Removed I/O functionality from DEV_CLRn, DEV_OE, CLK_USER and some DATA[0:7], updated Figure 1 for 600 Mbps, updated note 10,diffio and memory interface pins guidelines. Removed ES1 references.	12/31/2009
1.2	Added note regarding VCC/VCCAUX power on sequencing. Changed TDI and TMS pull-up to 1 k - 10 kΩ. Changed PORSEL description.	1/21/2010
1.3	Removed "Preliminary" status, Added Note 18 and edited note 8, Added to CLKIN and PLL[*]CLK descriptions. Updated notes in Example 1 for VCCR/T/L/H. Updated GND guideline, nCSO and ASDO Pin Type.	6/22/2011
1.4	Updated note (5) for the Pin Connection Guidelines.	3/7/2013
1.5	Updated note (5) for the Pin Connection Guidelines.	8/16/2013
1.6	Updated note (5) for the Pin Connection Guidelines.	8/23/2013
1.7	Updated note (5) for the Pin Connection Guidelines.	10/7/2013
1.8	Added note regarding the low noise switching regulator.	12/28/2015