Pin Information for the Stratix® II GX EP2SGX30 Device
Version 1.3

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B2	VREFB2N0	IO	DIFFIO_RX28p		C28			DQ0L0	DQ1L0	DQ0L0	
B2	VREFB2N0	IO	DIFFIO_RX28n		C27			DQ0L1	DQ1L1	DQ0L1	
B2	VREFB2N0	IO	DIFFIO_TX28p		H23			DQ9L0	DQ14L0	DQ11L0	DQ18L0
B2	VREFB2N0	IO	DIFFIO_TX28n		H22			DQ9L1	DQ14L1	DQ11L1	DQ18L1
B2	VREFB2N0	IO	DIFFIO_RX27p		D28			DQS0L	DQS1L	DQS0L	DQ2L0
B2	VREFB2N0	IO	DIFFIO_RX27n		D27			DQ0L2	DQ1L2	DQ0L2	DQ2L1
B2	VREFB2N0	IO	DIFFIO_TX27p		F24			DQS9L	DQS14L	DQS11L	DQS18L
B2	VREFB2N0	IO	DIFFIO_TX27n		F23			DQ9L2	DQ14L2	DQ11L2	DQ18L2
B2	VREFB2N0	IO	DIFFIO_RX26p		F27			DQ0L3	DQ1L3	DQ0L3	DQS2L
B2	VREFB2N0	IO	DIFFIO_RX26n		F26			DM0L	DM1L	DQ1L0	DQ2L2
B2	VREFB2N0	IO	DIFFIO_TX26p		G24			DQ9L3	DQ14L3	DQ11L3	DQ18L3
B2	VREFB2N0	IO	DIFFIO_TX26n		G23			DM9L	DM14L	DQ12L0	DQ19L0
B2	VREFB2N0	IO	DIFFIO_RX25p		E28			DQ1L0	DQ2L0	DQ1L1	DQ2L3
B2	VREFB2N0	IO	DIFFIO_RX25n		F28			DQ1L1	DQ2L1	DQS1L	DQ3L0
B2	VREFB2N0	IO	DIFFIO_TX25p		E26			DQ10L0	DQ15L0	DQ12L1	DQ19L1
B2	VREFB2N0	IO	DIFFIO_TX25n		E25			DQ10L1	DQ15L1	DQS12L	DQS19L
B2	VREFB2N0	VREFB2N0	VREFB2N0		T21						
B2	VREFB2N0	IO	DIFFIO_RX24p		G28			DQS1L	DQS2L	DQ1L2	DQ3L1
B2	VREFB2N0	IO	DIFFIO_RX24n		G27			DQ1L2	DQ2L2	DQ1L3	DQS3L
B2	VREFB2N0	IO	DIFFIO_TX24p		K24			DQS10L	DQS15L	DQ12L2	DQ19L2
B2	VREFB2N0	IO	DIFFIO_TX24n		J23			DQ10L2	DQ15L2	DQ12L3	DQ19L3
B2	VREFB2N0	IO	DIFFIO_RX23p		J27			DQ1L3	DQ2L3	DQ2L0	DQ3L2
B2	VREFB2N0	IO	DIFFIO_RX23n		J26			DM1L	DM2L	DQ2L1	DQ3L3
B2	VREFB2N0	IO	DIFFIO_TX23p		K22			DQ10L3	DQ15L3	DQ13L0	
B2	VREFB2N0	IO	DIFFIO_TX23n		K21			DM10L	DM15L	DQ13L1	
B2	VREFB2N0	IO	DIFFIO_RX22p		H28			DQ2L0	DQ3L0	DQS2L	DQ4L0
B2	VREFB2N0	IO	DIFFIO_RX22n		J28			DQ2L1	DQ3L1	DQ2L2	DQ4L1
B2	VREFB2N0	IO	DIFFIO_TX22p		K23			DQ11L0		DQS13L	
B2	VREFB2N0	IO	DIFFIO_TX22n		L23			DQ11L1		DQ13L2	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B2	VREFB2N0	IO	DIFFIO_RX21p		L26			DQS2L	DQS3L	DQ2L3	DQS4L
B2	VREFB2N0	IO	DIFFIO_RX21n		L25			DQ2L2	DQ3L2	DQ3L0	DQ4L2
B2	VREFB2N0	IO	DIFFIO_TX21p		G26			DQS11L		DQ13L3	
B2	VREFB2N0	IO	DIFFIO_TX21n		G25			DQ11L2		DQ14L0	
B2	VREFB2N1	IO	DIFFIO_RX20p		K28			DQ2L3	DQ3L3	DQ3L1	DQ4L3
B2	VREFB2N1	IO	DIFFIO_RX20n		K27			DM2L	DM3L	DQS3L	DQ5L0
B2	VREFB2N1	IO	DIFFIO_TX20p		M22			DQ11L3	DQ16L0	DQ14L1	
B2	VREFB2N1	IO	DIFFIO_TX20n		M21			DM11L	DQ16L1	DQS14L	
B2	VREFB2N1	IO	DIFFIO_RX19p		M27			DQ3L0	DQ4L0	DQ3L2	DQ5L1
B2	VREFB2N1	IO	DIFFIO_RX19n		M26			DQ3L1	DQ4L1	DQ3L3	DQS5L
B2	VREFB2N1	IO	DIFFIO_TX19p		J25			DQ12L0	DQS16L	DQ14L2	
B2	VREFB2N1	IO	DIFFIO_TX19n		J24			DQ12L1	DQ16L2	DQ14L3	
B2	VREFB2N1	IO	DIFFIO_RX18p		L28			DQS3L	DQS4L	DQ4L0	DQ5L2
B2	VREFB2N1	IO	DIFFIO_RX18n		M28			DQ3L2	DQ4L2	DQ4L1	DQ5L3
B2	VREFB2N1	IO	DIFFIO_TX18p		H26			DQS12L	DQ16L3	DQ15L0	
B2	VREFB2N1	IO	DIFFIO_TX18n		H25			DQ12L2	DM16L	DQ15L1	
B2	VREFB2N1	IO	DIFFIO_RX17p		N28			DQ3L3	DQ4L3	DQS4L	DQ6L0
B2	VREFB2N1	IO	DIFFIO_RX17n		P28			DM3L	DM4L	DQ4L2	DQ6L1
B2	VREFB2N1	IO	DIFFIO_TX17p		K26			DQ12L3	DQ17L0	DQS15L	DQ20L0
B2	VREFB2N1	IO	DIFFIO_TX17n		K25			DM12L	DQ17L1	DQ15L2	DQ20L1
B2	VREFB2N1	VREFB2N1	VREFB2N1		M23						
B2	VREFB2N1	IO	DIFFIO_RX16p		N26			DQ4L0	DQ5L0	DQ4L3	DQS6L
B2	VREFB2N1	IO	DIFFIO_RX16n		N25			DQ4L1	DQ5L1	DQ5L0	DQ6L2
B2	VREFB2N1	IO	DIFFIO_TX16p		M25			DQ13L0	DQS17L	DQ15L3	DQS20L
B2	VREFB2N1	IO	DIFFIO_TX16n		M24			DQ13L1	DQ17L2	DQ16L0	DQ20L2
B2	VREFB2N1	IO	DIFFIO_RX15p		P27			DQS4L	DQS5L	DQ5L1	DQ6L3
B2	VREFB2N1	IO	DIFFIO_RX15n		P26			DQ4L2	DQ5L2	DQS5L	DQ7L0
B2	VREFB2N1	IO	DIFFIO_TX15p		P25			DQS13L	DQ17L3	DQ16L1	DQ20L3
B2	VREFB2N1	IO	DIFFIO_TX15n		P24			DQ13L2	DM17L	DQS16L	DQ21L0

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B2	VREFB2N1	IO	DIFFIO_RX14p		R28			DQ4L3	DQ5L3	DQ5L2	DQ7L1
B2	VREFB2N1	IO	DIFFIO_RX14n		T28			DM4L	DM5L	DQ5L3	DQS7L
B2	VREFB2N1	IO	DIFFIO_TX14p		M20			DQ13L3	DQ18L0	DQ16L2	DQ21L1
B2	VREFB2N1	IO	DIFFIO_TX14n		N20			DM13L	DQ18L1	DQ16L3	DQS21L
B2	VREFB2N1	IO	DIFFIO_RX13p		T27				DQS18L		DQ7L2
B2	VREFB2N1	IO	DIFFIO_RX13n		T26				DQ18L2		DQ7L3
B2	VREFB2N1	IO	DIFFIO_TX13p		R21				DQ18L3		DQ21L2
B2	VREFB2N1	IO	DIFFIO_TX13n		R20				DM18L		DQ21L3
B2	VREFB2N1	IO	CLK0n/DIFFIO_RX_C0n		R25						
B2	VREFB2N1	IO	CLK0p/DIFFIO_RX_C0p		R26						
B2	VREFB2N1	CLK1n	INPUT		T24						
B2	VREFB2N1	CLK1p	INPUT		T25						
		VCCD_PLL1			N22						
		VCCA_PLL1			N23						
		GNDA_PLL1			P23						
		GNDA_PLL1			P22						
		GNDA_PLL2			R23						
		GNDA_PLL2			R22						
		VCCA_PLL2			T23						
		VCCD_PLL2			T22						
B1	VREFB1N0	IO	CLK2p/DIFFIO_RX_C1p		U28						
B1	VREFB1N0	IO	CLK2n/DIFFIO_RX_C1n		U27						
B1	VREFB1N0	CLK3p	INPUT		U26						
B1	VREFB1N0	CLK3n	INPUT		U25						
B1	VREFB1N0	IO	DIFFIO_RX12p		V28			DQ5L0	DQ6L0	DQ6L0	DQ8L0
B1	VREFB1N0	IO	DIFFIO_RX12n		W28			DQ5L1	DQ6L1	DQ6L1	DQ8L1
B1	VREFB1N0	IO	DIFFIO_TX12p		T19			DQ14L0	DQ19L0	DQ17L0	
B1	VREFB1N0	IO	DIFFIO_TX12n		U19			DQ14L1	DQ19L1	DQ17L1	
B1	VREFB1N0	IO	DIFFIO_RX11p		Y28			DQS5L	DQS6L	DQS6L	DQS8L

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B1	VREFB1N0	IO	DIFFIO_RX11n		AA28			DQ5L2	DQ6L2	DQ6L2	DQ8L2
B1	VREFB1N0	IO	DIFFIO_TX11p		U20			DQS14L	DQS19L	DQS17L	
B1	VREFB1N0	IO	DIFFIO_TX11n		V20			DQ14L2	DQ19L2	DQ17L2	
B1	VREFB1N0	VREFB1N0	VREFB1N0		Y23						
B1	VREFB1N0	IO	DIFFIO_RX10p		W27			DQ5L3	DQ6L3	DQ6L3	DQ8L3
B1	VREFB1N0	IO	DIFFIO_RX10n		W26			DM5L	DM6L	DQ7L0	DQ9L0
B1	VREFB1N0	IO	DIFFIO_TX10p		Y25			DQ14L3	DQ19L3	DQ17L3	
B1	VREFB1N0	IO	DIFFIO_TX10n		Y24			DM14L	DM19L	DQ18L0	
B1	VREFB1N0	IO	DIFFIO_RX9p		Y27			DQ6L0	DQ7L0	DQ7L1	DQ9L1
B1	VREFB1N0	IO	DIFFIO_RX9n		Y26			DQ6L1	DQ7L1	DQS7L	DQS9L
B1	VREFB1N0	IO	DIFFIO_TX9p		U24			DQ15L0	DQ20L0	DQ18L1	
B1	VREFB1N0	IO	DIFFIO_TX9n		U23			DQ15L1	DQ20L1	DQS18L	
B1	VREFB1N0	IO	DIFFIO_RX8p		V26			DQS6L	DQS7L	DQ7L2	DQ9L2
B1	VREFB1N0	IO	DIFFIO_RX8n		V25			DQ6L2	DQ7L2	DQ7L3	DQ9L3
B1	VREFB1N0	IO	DIFFIO_TX8p		AA26			DQS15L	DQS20L	DQ18L2	
B1	VREFB1N0	IO	DIFFIO_TX8n		AA25			DQ15L2	DQ20L2	DQ18L3	
B1	VREFB1N0	IO	DIFFIO_RX7p		AB28			DQ6L3	DQ7L3	DQ8L0	DQ10L0
B1	VREFB1N0	IO	DIFFIO_RX7n		AB27			DM6L	DM7L	DQ8L1	DQ10L1
B1	VREFB1N0	IO	DIFFIO_TX7p		V23			DQ15L3	DQ20L3	DQ19L0	
B1	VREFB1N0	IO	DIFFIO_TX7n		V22			DM15L	DM20L	DQ19L1	
B1	VREFB1N1	IO	DIFFIO_RX6p		AC28			DQ7L0	DQ8L0	DQS8L	DQS10L
B1	VREFB1N1	IO	DIFFIO_RX6n		AD28			DQ7L1	DQ8L1	DQ8L2	DQ10L2
B1	VREFB1N1	IO	DIFFIO_TX6p		W21			DQ16L0	DQ21L0	DQS19L	DQ22L0
B1	VREFB1N1	IO	DIFFIO_TX6n		Y21			DQ16L1	DQ21L1	DQ19L2	DQ22L1
B1	VREFB1N1	IO	DIFFIO_RX5p		AD26			DQS7L	DQS8L	DQ8L3	DQ10L3
B1	VREFB1N1	IO	DIFFIO_RX5n		AD25			DQ7L2	DQ8L2	DQ9L0	DQ11L0
B1	VREFB1N1	IO	DIFFIO_TX5p		AC25			DQS16L	DQS21L	DQ19L3	DQS22L
B1	VREFB1N1	IO	DIFFIO_TX5n		AC24			DQ16L2	DQ21L2	DQ20L0	DQ22L2
B1	VREFB1N1	IO	DIFFIO_RX4p		W25			DQ7L3	DQ8L3	DQ9L1	DQ11L1

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B1	VREFB1N1	IO	DIFFIO_RX4n		W24			DM7L	DM8L	DQS9L	DQS11L
B1	VREFB1N1	IO	DIFFIO_TX4p		AB22			DQ16L3	DQ21L3	DQ20L1	DQ22L3
B1	VREFB1N1	IO	DIFFIO_TX4n		AB21			DM16L	DM21L	DQS20L	DQ23L0
B1	VREFB1N1	VREFB1N1	VREFB1N1		W23						
B1	VREFB1N1	IO	DIFFIO_RX3p		AC27			DQ8L0	DQ9L0	DQ9L2	DQ11L2
B1	VREFB1N1	IO	DIFFIO_RX3n		AC26			DQ8L1	DQ9L1	DQ9L3	DQ11L3
B1	VREFB1N1	IO	DIFFIO_TX3p		AE26			DQ17L0	DQ22L0	DQ20L2	DQ23L1
B1	VREFB1N1	IO	DIFFIO_TX3n		AE25			DQ17L1	DQ22L1	DQ20L3	DQS23L
B1	VREFB1N1	IO	DIFFIO_RX2p		AB26			DQS8L	DQS9L	DQ10L0	DQ12L0
B1	VREFB1N1	IO	DIFFIO_RX2n		AB25			DQ8L2	DQ9L2	DQ10L1	DQ12L1
B1	VREFB1N1	IO	DIFFIO_TX2p		AB24			DQS17L	DQS22L	DQ21L0	DQ23L2
B1	VREFB1N1	IO	DIFFIO_TX2n		AB23			DQ17L2	DQ22L2	DQ21L1	DQ23L3
B1	VREFB1N1	IO	DIFFIO_RX1p		AE28			DQ8L3	DQ9L3	DQS10L	DQS12L
B1	VREFB1N1	IO	DIFFIO_RX1n		AE27			DM8L	DM9L	DQ10L2	DQ12L2
B1	VREFB1N1	IO	DIFFIO_TX1p		AC23			DQ17L3	DQ22L3	DQS21L	
B1	VREFB1N1	IO	DIFFIO_TX1n		AC22			DM17L	DM22L	DQ21L2	
B1	VREFB1N1	IO	DIFFIO_RX0p		AF28					DQ10L3	DQ12L3
B1	VREFB1N1	IO	DIFFIO_RX0n		AF27						
B1	VREFB1N1	IO	DIFFIO_TX0p		AA23					DQ21L3	
B1	VREFB1N1	IO	DIFFIO_TX0n		AA22						
B8	VREFB8N0	TDI		TDI	V19						
B8	VREFB8N0	TMS		TMS	W19						
B8	VREFB8N0	TCK		TCK	V16						
B8	VREFB8N0	TRST		TRST	W17						
B8	VREFB8N0	nCONFIG		nCONFIG	V17						
B8	VREFB8N0	VCCSEL		VCCSEL	W18						
B8	VREFB8N0	IO		CS	AE24						
B8	VREFB8N0	IO		CLKUSR	AC21						
B8	VREFB8N0	IO		nWS	AE22						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B8	VREFB8N0	IO		nRS	AE21						
B8	VREFB8N0	IO			AE23			DQ0B1		DQ0B1	
B8	VREFB8N0	IO			AE20			DQS0B		DQS0B	
B8	VREFB8N0	IO			W16			DQ0B2		DQ0B2	
B8	VREFB8N0	IO			AD20			DQ0B3		DQ0B3	
B8	VREFB8N0	IO			AB20			DM0B		DQ1B0	
B8	VREFB8N0	IO	DQ17B		AF26	DQ3B		DQ1B1	DQ17B3	DQS1B	DQ17B3
B8	VREFB8N0	IO	DQSn17B		AF25	DQ3B	DQ1B	DQS1B	DQSB17B	DQ1B2	DQSB17B
B8	VREFB8N0	VREFB8N0	VREFB8N0		AD19						
B8	VREFB8N0	IO	DQ17B		AG26	DQ3B	DQ1B	DQ1B2	DQ17B2	DQ1B3	DQ17B2
B8	VREFB8N0	IO	DQ17B		AH25	DQ3B	DQ1B	DQ1B3	DQ17B1	DQ2B0	DQ17B1
B8	VREFB8N0	IO	DQ17B		AH26	DQ3B	DQ1B	DM1B	DQ17B0	DQ2B1	DQ17B0
B8	VREFB8N0	IO	DQS17B		AG25	DQVLD3B		DQ2B0	DQS17B	DQS2B	DQS17B
B8	VREFB8N0	IO			AA19			DQ2B1		DQ2B2	
B8	VREFB8N0	IO			AB19			DQS2B		DQ2B3	
B8	VREFB8N0	IO			AC20			DQ2B2		DQ3B0	
B8	VREFB8N0	IO	DQ15B		AH24	DQ3B	DQ1B	DQ2B3	DQ15B3	DQ3B1	DQ15B3
B8	VREFB8N0	IO	DQSn15B		AF23	DQSn3B	DQ1B	DM2B	DQSB15B	DQS3B	DQSB15B
B8	VREFB8N0	IO	DQ15B		AF24	DQ3B	DQ1B	DQ3B0	DQ15B2	DQ3B2	DQ15B2
B8	VREFB8N0	IO	DQ15B		AF22	DQ3B	DQ1B	DQ3B1	DQ15B1	DQ3B3	DQ15B1
B8	VREFB8N0	IO	DQ15B		AH23	DQ3B	DQ1B	DQS3B	DQ15B0	DQ4B0	DQ15B0
B8	VREFB8N0	IO	DQS15B		AG23	DQS3B	DQVLD1B	DQ3B2	DQS15B	DQ4B1	DQS15B
B8	VREFB8N0	IO			AC19			DQ3B3		DQS4B	
B8	VREFB8N0	IO			AB18			DM3B		DQ4B2	
B8	VREFB8N0	IO			AE19			DQ4B0		DQ4B3	
B8	VREFB8N1	IO			AC18			DQ4B1		DQ5B0	
B8	VREFB8N1	IO	DQ13B		AG22	DQ2B	DQ1B	DQS4B	DQ13B3	DQ5B1	DQ13B3
B8	VREFB8N1	IO	DQSn13B		AF20	DQ2B	DQSn1B	DQ4B2	DQSB13B	DQS5B	DQSB13B
B8	VREFB8N1	IO	DQ13B		AH22	DQ2B	DQ1B	DQ4B3	DQ13B2	DQ5B2	DQ13B2

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B8	VREFB8N1	IO	DQ13B		AH21	DQ2B	DQ1B	DM4B	DQ13B1	DQ5B3	DQ13B1
B8	VREFB8N1	IO	DQ13B		AF21	DQ2B	DQ1B	DQ5B0	DQ13B0	DQ6B0	DQ13B0
B8	VREFB8N1	IO	DQS13B		AG20	DQVLD2B	DQS1B	DQ5B1	DQS13B	DQ6B1	DQS13B
B8	VREFB8N1	IO			AA17			DQS5B		DQS6B	
B8	VREFB8N1	IO			Y17			DQ5B2		DQ6B2	
B8	VREFB8N1	IO			AE18			DQ5B3		DQ6B3	
B8	VREFB8N1	IO	DQ11B		AH20	DQ2B	DQ1B	DM5B	DQ11B3	DQ7B0	DQ11B3
B8	VREFB8N1	IO	DQSn11B		AG19	DQSn2B	DQ1B	DQ6B0	DQSB11B	DQ7B1	DQSB11B
B8	VREFB8N1	IO	DQ11B		AF19	DQ2B	DQ1B	DQ6B1	DQ11B2	DQS7B	DQ11B2
B8	VREFB8N1	IO	DQ11B		AF18	DQ2B	DQ1B	DQS6B	DQ11B1	DQ7B2	DQ11B1
B8	VREFB8N1	IO	DQ11B		AH18	DQ2B	DQ1B	DQ6B2	DQ11B0	DQ7B3	DQ11B0
B8	VREFB8N1	IO	DQS11B		AH19	DQS2B		DQ6B3	DQS11B	DQ8B0	DQS11B
B8	VREFB8N1	VREFB8N1	VREFB8N1		AD17						
B8	VREFB8N1	IO			AB17			DM6B		DQ8B1	
B8	VREFB8N1	IO			AC17			DQ7B0		DQS8B	
B8	VREFB8N1	IO			W15			DQ7B1		DQ8B2	
B8	VREFB8N1	IO			Y15			DQS7B		DQ8B3	
B8	VREFB8N1	IO			AB16			DQ7B3			
B8	VREFB8N1	IO		RUnLU	AC16						
B8	VREFB8N1	IO		DEV_OE	AD16						
B8	VREFB8N1	IO		DEV_CLRn	AE17						
B8	VREFB8N1	IO		nCS	AF17						
B8	VREFB8N1	IO	CLK5n		AB15						
B8	VREFB8N1	IO	CLK5p		AC15						
B8	VREFB8N1	IO	CLK4n		AG17						
B8	VREFB8N1	IO	CLK4p		AH17						
		GNDA_PLL6			W14						
		GNDA_PLL6			W13						
		VCCA_PLL6			Y14						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		VCCD_PLL6			V14						
B10		VCC_PLL6_OUT			AA14						
B7	VREFB7N0	IO	CLK7p		AF15						
B7	VREFB7N0	IO	CLK7n		AE15						
B7	VREFB7N0	IO	CLK6p		AH16						
B7	VREFB7N0	IO	CLK6n		AG16						
B10	VREFB7N0	IO	PLL6_OUT1p		AG14						
B10	VREFB7N0	IO	PLL6_OUT1n		AF14						
B10	VREFB7N0	IO	PLL6_OUT0p		AH15						
B10	VREFB7N0	IO	PLL6_OUT0n		AH14						
B10	VREFB7N0	IO	PLL6_FBp/OUT2p		AE14						
B10	VREFB7N0	IO	PLL6_FBn/OUT2n		AD14						
B7	VREFB7N0	IO			Y13			DQ8B0		DQ9B0	
B7	VREFB7N0	IO			AB13			DQ8B1		DQ9B1	
B7	VREFB7N0	IO			V13			DQS8B		DQS9B	
B7	VREFB7N0	IO	DQ9B		AG13	DQ1B		DQ8B2	DQ9B3	DQ9B2	DQ9B3
B7	VREFB7N0	IO	DQSn9B		AE13	DQ1B	DQ0B	DQ8B3	DQSB9B	DQ9B3	DQSB9B
B7	VREFB7N0	VREFB7N0	VREFB7N0		AB14						
B7	VREFB7N0	IO	DQ9B		AC14	DQ1B	DQ0B	DM8B	DQ9B2	DQ10B0	DQ9B2
B7	VREFB7N0	IO	DQ9B		AC13	DQ1B	DQ0B	DQ9B0	DQ9B1	DQ10B1	DQ9B1
B7	VREFB7N0	IO	DQ9B		AD13	DQ1B	DQ0B	DQ9B1	DQ9B0	DQS10B	DQ9B0
B7	VREFB7N0	IO	DQS9B		AF13	DQVLD1B		DQS9B	DQS9B	DQ10B2	DQS9B
B7	VREFB7N0	IO			AB12			DQ9B2		DQ10B3	
B7	VREFB7N0	IO			W12			DQ9B3		DQ11B0	
B7	VREFB7N0	IO			V11			DM9B		DQ11B1	
B7	VREFB7N0	IO			AC12			DQ10B0		DQS11B	
B7	VREFB7N0	IO	DQ7B		AH13	DQ1B	DQ0B	DQ10B1	DQ7B3	DQ11B2	DQ7B3
B7	VREFB7N0	IO	DQSn7B		AF12	DQSn1B	DQ0B	DQS10B	DQSB7B	DQ11B3	DQSB7B
B7	VREFB7N0	IO	DQ7B		AH12	DQ1B	DQ0B	DQ10B2	DQ7B2	DQ12B0	DQ7B2

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B7	VREFB7N0	IO	DQ7B		AG11	DQ1B	DQ0B	DQ10B3	DQ7B1	DQ12B1	DQ7B1
B7	VREFB7N0	IO	DQ7B		AH11	DQ1B	DQ0B	DM10B	DQ7B0	DQS12B	DQ7B0
B7	VREFB7N0	IO	DQS7B		AE12	DQS1B	DQVLD0B	DQ11B0	DQS7B	DQ12B2	DQS7B
B7	VREFB7N0	IO			AA11			DQ11B1		DQ12B3	
B7	VREFB7N0	IO			AB11			DQS11B		DQ13B0	
B7	VREFB7N0	IO			W11			DQ11B2		DQ13B1	
B7	VREFB7N1	IO			AC11			DQ11B3		DQS13B	
B7	VREFB7N1	IO	DQ5B		AD11	DQ0B	DQ0B	DM11B	DQ5B3	DQ13B2	DQ5B3
B7	VREFB7N1	IO	DQSn5B		AF11	DQ0B	DQSn0B	DQ12B0	DQSB5B	DQ13B3	DQSB5B
B7	VREFB7N1	IO	DQ5B		AF10	DQ0B	DQ0B	DQ12B1	DQ5B2	DQ14B0	DQ5B2
B7	VREFB7N1	IO	DQ5B		AG10	DQ0B	DQ0B	DQS12B	DQ5B1	DQ14B1	DQ5B1
B7	VREFB7N1	IO	DQ5B		AH10	DQ0B	DQ0B	DQ12B2	DQ5B0	DQS14B	DQ5B0
B7	VREFB7N1	IO	DQS5B		AE11	DQVLD0B	DQS0B	DQ12B3	DQS5B	DQ14B2	DQS5B
B7	VREFB7N1	IO			AB9			DM12B		DQ14B3	
B7	VREFB7N1	IO			AB10			DQ13B0		DQ15B0	
B7	VREFB7N1	IO			Y11			DQ13B1		DQ15B1	
B7	VREFB7N1	IO	DQ3B		AE10	DQ0B	DQ0B	DQS13B	DQ3B3	DQS15B	DQ3B3
B7	VREFB7N1	IO	DQSn3B		AF9	DQSn0B	DQ0B	DQ13B2	DQSB3B	DQ15B2	DQSB3B
B7	VREFB7N1	IO	DQ3B		AH8	DQ0B	DQ0B	DQ13B3	DQ3B2	DQ15B3	DQ3B2
B7	VREFB7N1	IO	DQ3B		AH9	DQ0B	DQ0B	DM13B	DQ3B1	DQ16B0	DQ3B1
B7	VREFB7N1	IO	DQ3B		AD10	DQ0B	DQ0B	DQ14B0	DQ3B0	DQ16B1	DQ3B0
B7	VREFB7N1	IO	DQS3B		AE9	DQS0B		DQ14B1	DQS3B	DQS16B	DQS3B
B7	VREFB7N1	VREFB7N1	VREFB7N1		AC10						
B7	VREFB7N1	IO			AC9			DQS14B		DQ16B2	
B7	VREFB7N1	IO			Y10			DQ14B3		DQ17B0	
B7	VREFB7N1	IO			W10			DM14B		DQ17B1	
B7	VREFB7N1	IO	DQ1B		AH7			DQ15B0	DQ1B3	DQS17B	DQ1B3
B7	VREFB7N1	IO	DQSn1B		AG8			DQ15B1	DQSB1B	DQ17B2	DQSB1B
B7	VREFB7N1	IO	DQ1B		AE7			DQS15B	DQ1B2	DQ17B3	DQ1B2

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B7	VREFB7N1	IO	DQ1B		AF7			DQ15B2	DQ1B1	DQ18B0	DQ1B1
B7	VREFB7N1	IO	DQ1B		AE8			DQ15B3	DQ1B0	DQ18B1	DQ1B0
B7	VREFB7N1	IO	DQS1B		AF8			DM15B	DQS1B	DQS18B	DQS1B
B7	VREFB7N1	IO			W9					DQ18B3	
B7	VREFB7N1	IO	RDN7		AC8						
B7	VREFB7N1	IO	RUP7		AB8						
B7	VREFB7N1	PORSEL		PORSEL	Y8						
B7	VREFB7N1	nIO_PULLUP		nIO_PULLUP	Y7						
B7	VREFB7N1	PLL_ENA		PLL_ENA	AA8						
		GND			AC7						
B7	VREFB7N1	nCEO		nCEO	AB7						
B14		GXB_RX7n (3)			AD2						
B14		GXB_RX7p (3)			AD1						
B14		GXB_TX7n (3)			AF5						
B14		GXB_TX7p (3)			AF4						
B14		GXB_RX6n (3)			AB2						
B14		GXB_RX6p (3)			AB1						
B14		GXB_TX6n (3)			AD5						
B14		GXB_TX6p (3)			AD4						
B14		RREFB14 (3)			Y4						
B14		REFCLK0_B14n (3)			Y2						
B14		REFCLK0_B14p (3)			Y1						
B14		REFCLK1_B14n (3)			AB5						
B14		REFCLK1_B14p (3)			AB4						
		VCCL_B14			U6						
		VCCA			V9						
		VCCA			T6						
		VCCA			V7						
		GND			V8						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B14		GXB_RX4n (3)			V2						
B14		GXB_RX4p (3)			V1						
B14		GXB_TX4n (3)			V5						
B14		GXB_TX4p (3)			V4						
B14		GXB_RX5n (3)			T2						
B14		GXB_RX5p (3)			T1						
B14		GXB_TX5n (3)			T5						
B14		GXB_TX5p (3)			T4						
B13		GXB_RX3n			N2						
B13		GXB_RX3p			N1						
B13		GXB_TX3n			N5						
B13		GXB_TX3p			N4						
B13		GXB_RX2n			L2						
B13		GXB_RX2p			L1						
B13		GXB_TX2n			L5						
B13		GXB_TX2p			L4						
B13		RREFB13			J4						
B13		REFCLK0_B13n			J2						
B13		REFCLK0_B13p			J1						
B13		REFCLK1_B13n			G5						
B13		REFCLK1_B13p			G4						
		VCCL_B13			N6						
		VCCA			P9						
		VCCA			M6						
		VCCA			P7						
		GND			P8						
B13		GXB_RX0n			G2						
B13		GXB_RX0p			G1						
B13		GXB_TX0n			E5						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B13		GXB_TX0p			E4						
B13		GXB_RX1n			E2						
B13		GXB_RX1p			E1						
B13		GXB_TX1n			C5						
B13		GXB_TX1p			C4						
		NC			K7						
		NC			K8						
		VCCA			K9						
		TEMPDIODEp			F7						
		TEMPDIODEn			G7						
B4	VREFB4N0	TDO		TDO	F8						
B4	VREFB4N0	MSEL3		MSEL3	G8						
B4	VREFB4N0	MSEL2		MSEL2	H8						
B4	VREFB4N0	MSEL1		MSEL1	E8						
B4	VREFB4N0	MSEL0		MSEL0	J8						
B4	VREFB4N0	IO	RUP4		C7						
B4	VREFB4N0	IO	RDN4		D7						
B4	VREFB4N0	IO	DQS1T		C8				DQS1T		DQS1T
B4	VREFB4N0	IO	DQ1T		D9				DQ1T0	DQ18T3	DQ1T0
B4	VREFB4N0	IO	DQ1T		A7				DQ1T1	DQ18T2	DQ1T1
B4	VREFB4N0	IO	DQ1T		D8			DM14T	DQ1T2	DQS18T	DQ1T2
B4	VREFB4N0	IO	DQSn1T		B8			DQ14T3	DQSB1T	DQ18T1	DQSB1T
B4	VREFB4N0	IO	DQ1T		A8			DQ14T2	DQ1T3	DQ18T0	DQ1T3
B4	VREFB4N0	IO			K10			DQS14T		DQ17T3	
B4	VREFB4N0	IO			G9			DQ14T1		DQ17T2	
B4	VREFB4N0	IO			H10			DQ14T0		DQS17T	
B4	VREFB4N0	IO			J10			DQ13T3		DQ17T0	
B4	VREFB4N0	VREFB4N0	VREFB4N0		F10						
B4	VREFB4N0	IO	DQS3T		D10	DQS0T		DQ13T2	DQS3T	DQ16T3	DQS3T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B4	VREFB4N0	IO	DQ3T		B10	DQ0T	DQ0T	DQS13T	DQ3T0	DQ16T2	DQ3T0
B4	VREFB4N0	IO	DQ3T		A9	DQ0T	DQ0T	DQ13T1	DQ3T1	DQS16T	DQ3T1
B4	VREFB4N0	IO	DQ3T		C9	DQ0T	DQ0T	DQ13T0	DQ3T2	DQ16T1	DQ3T2
B4	VREFB4N0	IO	DQSn3T		C10	DQSn0T	DQ0T	DM12T	DQSB3T	DQ16T0	DQSB3T
B4	VREFB4N0	IO	DQ3T		E11	DQ0T	DQ0T	DQ12T3	DQ3T3	DQ15T3	DQ3T3
B4	VREFB4N0	IO			E10			DQ12T2		DQ15T2	
B4	VREFB4N0	IO			K11			DQS12T		DQS15T	
B4	VREFB4N0	IO			G11			DQ12T1		DQ15T1	
B4	VREFB4N0	IO			G10			DQ12T0		DQ15T0	
B4	VREFB4N0	IO	DQS5T		C11	DQVLD0T	DQS0T	DM11T	DQS5T	DQ14T3	DQS5T
B4	VREFB4N0	IO	DQ5T		C12	DQ0T	DQ0T	DQ11T3	DQ5T0	DQ14T2	DQ5T0
B4	VREFB4N0	IO	DQ5T		D11	DQ0T	DQ0T	DQ11T2	DQ5T1	DQS14T	DQ5T1
B4	VREFB4N0	IO	DQ5T		A10	DQ0T	DQ0T	DQS11T	DQ5T2	DQ14T1	DQ5T2
B4	VREFB4N0	IO	DQSn5T		B11	DQ0T	DQSn0T	DQ11T1	DQSB5T	DQ14T0	DQSB5T
B4	VREFB4N0	IO	DQ5T		D12	DQ0T	DQ0T	DQ11T0	DQ5T3	DQ13T3	DQ5T3
B4	VREFB4N0	IO			J11			DM10T		DQ13T2	
B4	VREFB4N0	IO			H11			DQ10T3		DQS13T	
B4	VREFB4N1	IO			K12			DQ10T2		DQ13T1	
B4	VREFB4N1	IO			F11			DQS10T		DQ13T0	
B4	VREFB4N1	IO			L12			DQ10T1		DQ12T3	
B4	VREFB4N1	IO	DQS7T		D13	DQS1T	DQVLD0T	DQ10T0	DQS7T	DQ12T2	DQS7T
B4	VREFB4N1	IO	DQ7T		A11	DQ1T	DQ0T	DM9T	DQ7T0	DQS12T	DQ7T0
B4	VREFB4N1	IO	DQ7T		F13	DQ1T	DQ0T	DQ9T3	DQ7T1	DQ12T1	DQ7T1
B4	VREFB4N1	IO	DQ7T		A12	DQ1T	DQ0T	DQ9T2	DQ7T2	DQ12T0	DQ7T2
B4	VREFB4N1	IO	DQSn7T		C13	DQSn1T	DQ0T	DQS9T	DQSB7T	DQ11T3	DQSB7T
B4	VREFB4N1	IO	DQ7T		E13	DQ1T	DQ0T	DQ9T1	DQ7T3	DQ11T2	DQ7T3
B4	VREFB4N1	IO			G12			DQ9T0		DQS11T	
B4	VREFB4N1	IO			K13			DM8T		DQ11T1	
B4	VREFB4N1	IO			L14			DQ8T3		DQ11T0	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B4	VREFB4N1	IO			L13			DQ8T2		DQ10T3	
B4	VREFB4N1	IO	DQS9T		B14	DQVLD1T		DQS8T	DQS9T	DQ10T2	DQS9T
B4	VREFB4N1	IO	DQ9T		E14	DQ1T	DQ0T	DQ8T1	DQ9T0	DQS10T	DQ9T0
B4	VREFB4N1	IO	DQ9T		A13	DQ1T	DQ0T	DQ8T0	DQ9T1	DQ10T1	DQ9T1
B4	VREFB4N1	IO	DQ9T		B13	DQ1T	DQ0T	DM7T	DQ9T2	DQ10T0	DQ9T2
B4	VREFB4N1	VREFB4N1	VREFB4N1		F12						
B4	VREFB4N1	IO	DQSn9T		C14	DQ1T	DQ0T	DQ7T3	DQSB9T	DQ9T3	DQSB9T
B4	VREFB4N1	IO	DQ9T		D14	DQ1T		DQ7T2	DQ9T3	DQ9T2	DQ9T3
B4	VREFB4N1	IO			H13			DQS7T		DQS9T	
B4	VREFB4N1	IO			G13			DQ7T1		DQ9T1	
B4	VREFB4N1	IO			K14			DQ7T0		DQ9T0	
B9	VREFB4N1	IO	PLL5_FBn/OUT2n		G14						
B9	VREFB4N1	IO	PLL5_FBp/OUT2p		F14						
B9	VREFB4N1	IO	PLL5_OUT0n		A14						
B9	VREFB4N1	IO	PLL5_OUT0p		A15						
B9	VREFB4N1	IO	PLL5_OUT1n		D15						
B9	VREFB4N1	IO	PLL5_OUT1p		C15						
B4	VREFB4N1	IO	CLK12n		B16						
B4	VREFB4N1	IO	CLK12p		A16						
B4	VREFB4N1	IO	CLK13n		G15						
B4	VREFB4N1	IO	CLK13p		F15						
B9		VCC_PLL5_OUT			J14						
		VCCD_PLL5			K16						
		VCCA_PLL5			J15						
		GNDA_PLL5			J16						
		GNDA_PLL5			K15						
B3	VREFB3N0	IO	CLK14p		A17						
B3	VREFB3N0	IO	CLK14n		B17						
B3	VREFB3N0	IO	CLK15p		C16						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B3	VREFB3N0	IO	CLK15n		D16						
B3	VREFB3N0	IO		PGM2	E16						
B3	VREFB3N0	IO		PGM1	F16						
B3	VREFB3N0	IO		PGM0	G16						
B3	VREFB3N0	IO		ASDO	L16						
B3	VREFB3N0	IO		nCSO	D17						
B3	VREFB3N0	IO		CRC_ERROR	E17						
B3	VREFB3N0	IO		DATA0	F17						
B3	VREFB3N0	IO		DATA1	K17						
B3	VREFB3N0	IO			G17					DQ8T3	
B3	VREFB3N0	IO			D18					DQ8T2	
B3	VREFB3N0	IO			F18					DQS8T	
B3	VREFB3N0	IO			L17			DM6T		DQ8T1	
B3	VREFB3N0	VREFB3N0	VREFB3N0		E19						
B3	VREFB3N0	IO	DQS11T		A19	DQS2T		DQ6T3	DQS11T	DQ8T0	DQS11T
B3	VREFB3N0	IO	DQ11T		A18	DQ2T	DQ1T	DQ6T2	DQ11T0	DQ7T3	DQ11T0
B3	VREFB3N0	IO	DQ11T		C18	DQ2T	DQ1T	DQS6T	DQ11T1	DQ7T2	DQ11T1
B3	VREFB3N0	IO	DQ11T		C19	DQ2T	DQ1T	DQ6T1	DQ11T2	DQS7T	DQ11T2
B3	VREFB3N0	IO	DQSn11T		B19	DQSn2T	DQ1T	DQ6T0	DQSB11T	DQ7T1	DQSB11T
B3	VREFB3N0	IO	DQ11T		A20	DQ2T	DQ1T	DM5T	DQ11T3	DQ7T0	DQ11T3
B3	VREFB3N0	IO			F19			DQ5T3		DQ6T3	
B3	VREFB3N0	IO			G18			DQ5T2		DQ6T2	
B3	VREFB3N0	IO			J18			DQS5T		DQS6T	
B3	VREFB3N0	IO			K18			DQ5T1		DQ6T1	
B3	VREFB3N0	IO	DQS13T		B20	DQVLD2T	DQS1T	DQ5T0	DQS13T	DQ6T0	DQS13T
B3	VREFB3N0	IO	DQ13T		A21	DQ2T	DQ1T	DM4T	DQ13T0	DQ5T3	DQ13T0
B3	VREFB3N0	IO	DQ13T		C21	DQ2T	DQ1T	DQ4T3	DQ13T1	DQ5T2	DQ13T1
B3	VREFB3N0	IO	DQ13T		A22	DQ2T	DQ1T	DQ4T2	DQ13T2	DQS5T	DQ13T2
B3	VREFB3N0	IO	DQSn13T		C20	DQ2T	DQSn1T	DQS4T	DQSB13T	DQ5T1	DQSB13T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B3	VREFB3N0	IO	DQ13T		B22	DQ2T	DQ1T	DQ4T1	DQ13T3	DQ5T0	DQ13T3
B3	VREFB3N0	IO			K19			DQ4T0		DQ4T3	
B3	VREFB3N1	IO			H19			DM3T		DQ4T2	
B3	VREFB3N1	IO			D19			DQ3T3		DQS4T	
B3	VREFB3N1	IO	DQS15T		B23	DQS3T	DQVLD1T	DQ3T2	DQS15T	DQ4T1	DQS15T
B3	VREFB3N1	IO	DQ15T		A23	DQ3T	DQ1T	DQS3T	DQ15T0	DQ4T0	DQ15T0
B3	VREFB3N1	IO	DQ15T		C22	DQ3T	DQ1T	DQ3T1	DQ15T1	DQ3T3	DQ15T1
B3	VREFB3N1	IO	DQ15T		A24	DQ3T	DQ1T	DQ3T0	DQ15T2	DQ3T2	DQ15T2
B3	VREFB3N1	IO	DQSn15T		C23	DQSn3T	DQ1T	DM2T	DQSB15T	DQS3T	DQSB15T
B3	VREFB3N1	IO	DQ15T		C24	DQ3T	DQ1T	DQ2T3	DQ15T3	DQ3T1	DQ15T3
B3	VREFB3N1	IO			D20			DQ2T2		DQ3T0	
B3	VREFB3N1	IO			L19			DQS2T		DQ2T3	
B3	VREFB3N1	IO			G19			DQ2T1		DQ2T2	
B3	VREFB3N1	IO			G20			DQ2T0		DQS2T	
B3	VREFB3N1	IO	DQS17T		B25	DQVLD3T		DM1T	DQS17T	DQ2T1	DQS17T
B3	VREFB3N1	IO	DQ17T		A26	DQ3T	DQ1T	DQ1T3	DQ17T0	DQ2T0	DQ17T0
B3	VREFB3N1	IO	DQ17T		A25	DQ3T	DQ1T	DQ1T2	DQ17T1	DQ1T3	DQ17T1
B3	VREFB3N1	IO	DQ17T		C26	DQ3T	DQ1T	DQS1T	DQ17T2	DQ1T2	DQ17T2
B3	VREFB3N1	IO	DQSn17T		C25	DQ3T	DQ1T	DQ1T1	DQSB17T	DQS1T	DQSB17T
B3	VREFB3N1	IO	DQ17T		B26	DQ3T		DQ1T0	DQ17T3	DQ1T1	DQ17T3
B3	VREFB3N1	VREFB3N1	VREFB3N1		E20						
B3	VREFB3N1	IO			F20			DQ0T3		DQ0T3	
B3	VREFB3N1	IO			J20			DQ0T2		DQ0T2	
B3	VREFB3N1	IO			K20			DQS0T		DQS0T	
B3	VREFB3N1	IO			L20			DQ0T0		DQ0T0	
B3	VREFB3N1	IO		DATA2	F21						
B3	VREFB3N1	IO		DATA3	D21						
B3	VREFB3N1	IO		DATA4	G21						
B3	VREFB3N1	IO		DATA5	D23						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
B3	VREFB3N1	IO		DATA6	F22						
B3	VREFB3N1	IO		DATA7	D22						
B3	VREFB3N1	IO		RDYnBSY	J21						
B3	VREFB3N1	IO		INIT_DONE	G22						
B3	VREFB3N1	nSTATUS		nSTATUS	E23						
B3	VREFB3N1	nCE		nCE	D24						
B3	VREFB3N1	DCLK		DCLK	D25						
B3	VREFB3N1	CONF_DONE		CONF_DONE	D26						
		VCCIO2			J22						
		VCCIO2			L22						
		VCCIO2			N21						
		VCCIO1			U22						
		VCCIO1			V21						
		VCCIO1			Y22						
		VCCIO8			AA16						
		VCCIO8			Y18						
		VCCIO8			Y19						
		VCCIO7			AA10						
		VCCIO7			AA13						
		VCCIO7			Y9						
		VCCT_B14			R8						
		VCCT_B14			T8						
		VCCH_B14			R9						
		VCCH_B14			T9						
		VCCR			R7						
		VCCR			T7						
		VCCA			R6						
		VCCT_B13			L8						
		VCCT_B13			M8						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		VCCH_B13			L9						
		VCCH_B13			M9						
		VCCR			L7						
		VCCR			M7						
		VCCA			L6						
		VCCP			R10						
		VCCP			T10						
		VCCP			L10						
		VCCP			M10						
		VCCIO4			H14						
		VCCIO4			J9						
		VCCIO4			J12						
		VCCIO3			H17						
		VCCIO3			H20						
		VCCIO3			J19						
		VCCINT			M11						
		VCCINT			M13						
		VCCINT			M15						
		VCCINT			M17						
		VCCINT			N12						
		VCCINT			N14						
		VCCINT			N16						
		VCCINT			N18						
		VCCINT			P11						
		VCCINT			P13						
		VCCINT			P15						
		VCCINT			P17						
		VCCINT			R12						
		VCCINT			R14						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		VCCINT			R16						
		VCCINT			R18						
		VCCINT			T11						
		VCCINT			T13						
		VCCINT			T15						
		VCCINT			T17						
		VCCINT			U12						
		VCCINT			U14						
		VCCINT			U16						
		VCCINT			U18						
		GND			AA21						
		GND			AA24						
		GND			AA27						
		GND			AD24						
		GND			AD27						
		GND			AG27						
		GND			AG28						
		GND			B28						
		GND			E27						
		GND			H21						
		GND			H24						
		GND			H27						
		GND			L21						
		GND			L24						
		GND			L27						
		GND			M19						
		GND			N24						
		GND			N27						
		GND			P21						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			R24						
		GND			R27						
		GND			U21						
		GND			V24						
		GND			V27						
		GND			W20						
		GND			W22						
		GND			Y20						
		GND			W8						
		GND			W7						
		GND			V18						
		GND			V15						
		GND			V12						
		GND			V10						
		GND			AH27						
		GND			AG9						
		GND			AG7						
		GND			AG24						
		GND			AG21						
		GND			AG18						
		GND			AG15						
		GND			AG12						
		GND			AD9						
		GND			AD7						
		GND			AD21						
		GND			AD18						
		GND			AD15						
		GND			AD12						
		GND			AA9						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			AA7						
		GND			AA20						
		GND			AA18						
		GND			AA15						
		GND			AA12						
		GND			A2						
		GND			A3						
		GND			A4						
		GND			A5						
		GND			A6						
		GND			AA1						
		GND			AA2						
		GND			AA3						
		GND			AA4						
		GND			AA5						
		GND			AA6						
		GND			AB3						
		GND			AB6						
		GND			AC1						
		GND			AC2						
		GND			AC3						
		GND			AC4						
		GND			AC5						
		GND			AC6						
		GND			AD3						
		GND			AD6						
		GND			AE1						
		GND			AE2						
		GND			AE3						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			AE4						
		GND			AE5						
		GND			AE6						
		GND			AF1						
		GND			AF2						
		GND			AF3						
		GND			AF6						
		GND			AG1						
		GND			AG2						
		GND			AG3						
		GND			AG4						
		GND			AG5						
		GND			AG6						
		GND			AH2						
		GND			AH3						
		GND			AH4						
		GND			AH5						
		GND			AH6						
		GND			B1						
		GND			B2						
		GND			B3						
		GND			B4						
		GND			B5						
		GND			B6						
		GND			C1						
		GND			C2						
		GND			C3						
		GND			C6						
		GND			D1						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			D2						
		GND			D3						
		GND			D4						
		GND			D5						
		GND			D6						
		GND			E3						
		GND			E6						
		GND			F1						
		GND			F2						
		GND			F3						
		GND			F4						
		GND			F5						
		GND			F6						
		GND			G3						
		GND			G6						
		GND			H1						
		GND			H2						
		GND			H3						
		GND			H4						
		GND			H5						
		GND			H6						
		GND			J3						
		GND			J5						
		GND			J6						
		GND			K1						
		GND			K2						
		GND			K3						
		GND			K4						
		GND			K5						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			K6						
		GND			L3						
		GND			M1						
		GND			M2						
		GND			M3						
		GND			M4						
		GND			M5						
		GND			N3						
		GND			N7						
		GND			N8						
		GND			N9						
		GND			N10						
		GND			P1						
		GND			P2						
		GND			P3						
		GND			P4						
		GND			P5						
		GND			P6						
		GND			R1						
		GND			R2						
		GND			R3						
		GND			R4						
		GND			R5						
		GND			T3						
		GND			U1						
		GND			U2						
		GND			U3						
		GND			U4						
		GND			U5						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			U7						
		GND			U8						
		GND			U9						
		GND			U10						
		GND			V3						
		GND			V6						
		GND			W1						
		GND			W2						
		GND			W3						
		GND			W4						
		GND			W5						
		GND			W6						
		GND			Y3						
		GND			Y5						
		GND			Y6						
		GND			A27						
		GND			B12						
		GND			B15						
		GND			B18						
		GND			B21						
		GND			B24						
		GND			B27						
		GND			B7						
		GND			B9						
		GND			E12						
		GND			E15						
		GND			E18						
		GND			E21						
		GND			E24						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			E7						
		GND			E9						
		GND			H12						
		GND			H15						
		GND			H16						
		GND			H18						
		GND			H7						
		GND			H9						
		GND			J7						
		GND			L11						
		GND			L15						
		GND			L18						
		GND			M12						
		GND			M14						
		GND			M16						
		GND			M18						
		GND			N11						
		GND			N13						
		GND			N15						
		GND			N17						
		GND			N19						
		GND			P10						
		GND			P12						
		GND			P14						
		GND			P16						
		GND			P18						
		GND			P19						
		GND			R11						
		GND			R13						

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780
		GND			R15						
		GND			R17						
		GND			R19						
		GND			T12						
		GND			T14						
		GND			T16						
		GND			T18						
		GND			U11						
		GND			U13						
		GND			U15						
		GND			U17						
		VCCPD2			P20						
		VCCPD1			T20						
		VCCPD8			Y16						
		VCCPD7			Y12						
		VCCPD4			J13						
		VCCPD3			J17						
		NC			AD8						
		NC			AD22						
		NC			AD23						
		NC			AE16						
		NC			AF16						
		NC			C17						
		NC			E22						
		NC			F9						
		NC			F25						

Notes:

(1) This mode is used for x4 DDR2 SDRAM (with DM support) devices and x9 RLDRAM II devices.

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F780	x8/x9 Mode	x16/x18 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780	DQ group for non-DQS mode (non-migratable) F780	DQ group for non-DQS mode (migratable) F780

(2) This mode is used for DDR/DDR2 SDRAM, RLDRAM II, and QDRII SRAM interfaces, except for x9 RLDRAM II devices. This mode can support x4 DDR2 SDRAM devices if the DM pins are not used.

(3) The EP2SGX30C device does not provide the following signals on bank 14: REFCLK[0:1]_B14p/n, GXB_RX[4:7]p/n, GXB_TX[4:7]p/n.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	1.2-V internal logic array voltage supply pins. VCCINT also supplies power to the column dedicated clock input pins for the LVDS, LVPECL, HSTL, SSTL, differential HSTL, and differential SSTL I/O standards.
VCCIO[1..4,7,8]	Power	I/O supply voltage pins for banks 1-4, 7, and 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for row differential standards as well as all single-ended I/O standards with the exception of HSTL and SSTL on column dedicated clock input pins which are powered by VCCINT.
VCCPD[1..4,7,8]	Power	Dedicated power pins. This 3.3-V supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The VCCPD pins must be connected to 3.3 V and must ramp up from 0 V to 3.3 V within 100 ms to ensure successful configuration. If you use the AES key programming feature of the device, VCCPD8 powers the circuitry, enabling the key to be programmed in non-volatile memory. During key programming, apply 3.7 V to VCCPD8. For further information, refer to AN341: Using the Design Security Feature in Stratix II and Stratix II GX Devices.
GND	Ground	Device ground pins.
VREFB[1..4,7,8]N[4..0] (Note 8)	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for that bank. All the VREF pins within a bank are shorted together. If VREF pins are not used, you should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p, and PLL5_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL5 in bank 9 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p, and PLL6_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL6 in bank 10 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL11_OUT (Note 6)	Power	External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p, and PLL11_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL11 in bank 11 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL12_OUT (Note 6)	Power	External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p, and PLL12_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL12 in bank 12 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCCA_PLL[1,2,5..8,11,12] (Note 4)	Power	1.2-V analog power for PLL[1,2,5..8,11,12].
VCCD_PLL[1,2,5..8,11,12] (Note 4)	Power	1.2-V digital power for PLL[1,2,5..8,11,12].
GNDA_PLL[1,2,5..8,11,12] (Note 4)	Ground	Analog ground for PLL[1,2,5..8,11,12].
NC	No Connect	Do not drive any signals into this pin.
RUP4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
RDN4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
RUP7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rup must be connected to the designated RUP pin within bank 7. If not required, this pin is a regular I/O pin.
RDN7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rdn must be connected to the designated RDN pin within bank 7. If not required, this pin is a regular I/O pin.
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns it on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device or microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the Stratix II GX device. If the temperature-sensing diode is not used, then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the Stratix II GX device. If the temperature-sensing diode is not used, then connect this pin to GND.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Stratix II GX device. In AS mode, DCLK is an output from the Stratix II GX device that provides timing for the configuration interface.
MSEL[3..0]	Input	Configuration input pins that set the Stratix II GX device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic-high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PORSEL	Input	Dedicated input that selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms.
Optional/Dual-Purpose Configuration Pins		
nCSO	I/O, Output	Output control signal from the Stratix II GX FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	I/O, Output	Control signal from the Stratix II GX FPGA to the serial configuration device in AS mode used to read out configuration data.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[6..1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[7..0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
DATA7	I/O, Bidirectional	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal has been strobed low.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
nCS, CS	I/O, Input	These are chip-select inputs that enable the Stratix II GX device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active-high enable, use the CS pin and drive the nCS pin low. If a design requires an active-low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
RUnLU	I/O, Input	Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration modes, this pin is available as general-purpose user I/O pin.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Clock and PLL Pins		
CLK[1,3]p	Clock, Input	Dedicated clock input pins 1 and 3 that can also be used for data inputs.
CLK[1,3]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs.
CLK[2,0]p/DIFFIO_RX_C[1,0]p (Note 5)	I/O, Clock	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[2,0]n/DIFFIO_RX_C[1,0]n (Note 5)	I/O, Clock	These pins can be used as I/O pins, the negative clock input pins for differential clock input, or the negative data pins of differential receiver channels.
CLK[4-7,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-7,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs.
FPLL[8..7]CLKp (Note 6)	Clock, Input	Dedicated positive clock inputs for fast PLLs (PLLs 7 and 8), which can also be used for data inputs.
FPLL[8..7]CLKn (Note 6)	Clock, Input	Dedicated negative clock inputs associated with the FPLL[7,8]CLKp pins, which can also be used for data inputs.
PLL5_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL5. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL5).
PLL5_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL5. If the clock outputs are single-ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL6_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL6. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL6).
PLL6_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL6. If the clock outputs are single-ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL11_OUT[1,0]p (Note 6)	Output	Optional positive external clock outputs [1,0] from enhanced PLL11. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL11).
PLL11_OUT[1,0]n (Note 6)	Output	Optional negative external clock outputs [1,0] from enhanced PLL11. If the clock outputs are single-ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL12_OUT[1,0]p (Note 6)	Output	Optional positive external clock outputs [1,0] from enhanced PLL12. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL12).
PLL12_OUT[1,0]n (Note 6)	Output	Optional negative external clock outputs [1,0] from enhanced PLL12. If the clock outputs are single-ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL[6..5]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or external clock outputs for PLL[6,5].
PLL[6..5]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[6,5]_FBp, or negative terminal clock output pins for differential clock output.
PLL[12..11]_FBp/OUT2p (Note 6)	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or positive external clock outputs for PLL[12..11].
PLL[12..11]_FBn/OUT2n (Note 6)	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[12..11]_FBp, or negative external clock output pins for differential clock output.
Dual-Purpose Differential & External Memory Interface Pins		
DIFFIO_RX[76..1]p (Note 5)	I/O, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_RX[76..1]n (Note 5)	I/O, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[77..0]p (Note 5)	I/O, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[77..0]n (Note 5)	I/O, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[17..0][T,B] (Note 7)	DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[17..0][T,B]	DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase-shift circuitry.
DQ[17..0][T,B][3..0] (Note 7)	DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DQVLD[8..0][T,B]	DQVLD	Optional data valid signal for use in external memory interfacing.
Transceiver (I/O Banks) Pins		
VCCP	Power	GX bank [17..13] PCS power. This power is connected to 1.2 V.
VCCR	Power	GX bank [17..13] receiver analog power. This power is connected to 1.2 V.
VCCT_B[17..13] (Note 3)	Power	GX bank [17..13] transmitter analog power. This power is connected to 1.2 V.
VCCA	Power	GX bank [17..13] analog power. This power is connected to 3.3 V.
VCCH_B[17..13] (Note 3)	Power	GX bank [17..13] transmitter driver analog power. This power is connected to 1.2 V or 1.5 V.
VCCL_B[17..13] (Note 3)	Power	GX bank [17..13] VCO analog power. This power is connected to 1.2 V.
GXB_RX[19..0]p (Note 2)	I, Input	High-speed positive differential receiver channels.
GXB_RX[19..0]n (Note 2)	I, Input	High-speed negative differential receiver channels.
GXB_TX[19..0]p (Note 2)	O, Output	High-speed positive differential transmitter channel.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
GXB_TX[19..0]n (Note 2)	O, Output	High-speed negative differential transmitter channels.
REFCLK[0,1]_B[17..13]p (Note 3)	I, Input	High-speed differential I/O reference clock positive. This pin is powered by 1.2-V VCCT_B[17..13].
REFCLK[0,1]_B[17..13]n (Note 3)	I, Input	High-speed differential I/O reference clock negative. This pin is powered by 1.2-V VCCT_B[17..13].
RREFB[17..13] (Note 3)	I, Input	Reference resistor for GX side banks.

Notes:

1) These descriptions are created based on the Stratix II GX130 device (EP2SGX130GF1508).

2) Transceiver signals GXB_RX[19..0] and GXB_TX[19..0] are device-specific.
EP2SGX30C and EP2SGX60C each contains 4 transceivers: GXB_RX[3..0] and GXB_TX[3..0].
EP2SGX30D and EP2SGX60D each contains 8 transceivers: GXB_RX[7..0] and GXB_TX[7..0].
EP2SGX60E and EP2SGX90E each contains 12 transceivers: GXB_RX[11..0] and GXB_TX[11..0].
EP2SGX90F contains 16 transceivers: GXB_RX[15..0] and GXB_TX[15..0].
EP2SGX130G contains 20 transceivers: GXB_RX[19..0] and GXB_TX[19..0].

3) Pins VCCT_B[17..13], VCCH_B[17..13], REFCLK[0,1]_B[17..13], RREFB[17..13], and VCCL[17..13] refer to the bank number of the transceiver.
EP2SGX30C and EP2SGX60C each consists of 4 transceivers in Bank 13.
EP2SGX30D and EP2SGX60D each consists of 8 transceivers in Banks 13 to 14.
EP2SGX60E and EP2SGX90E each consists of 12 transceivers in Banks 13 to 15.
EP2SGX90F consists of 16 transceivers in Banks 13 to 16.
EP2SGX130G consists of 20 transceivers in Banks 13 to 17.

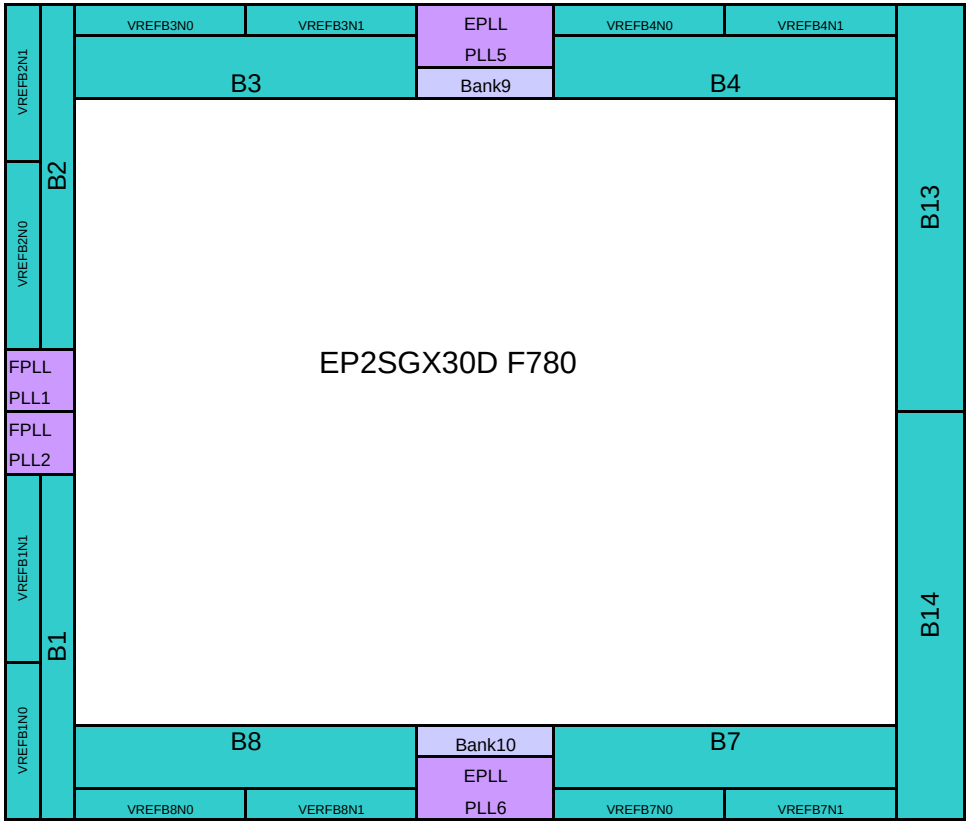
4) EP2SGX30 and EP2SGX 60C/D only have PLL(1, 2, 5 & 6). EP2SGX60E, EP2SGX90, and EP2SGX130 have PLL(1,2, 5, 6, 7, 8, 11 & 12).

5) The differential TX/RX count for each device and package is different.
EP2SGX30, EP2SGX60C, and EP2SGX60D each consists of 29 transmit and 29 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX60E consists of 42 transmit and 40 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX90E consists of 45 transmit and 45 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX90F consists of 59 transmit and 57 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX130G consists of 71 transmit and 71 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]). The transmit bus numbers 15-17 and 64-68 are unused. Also, the receive bus numbers 15-17, 64, and 65 are not unused.

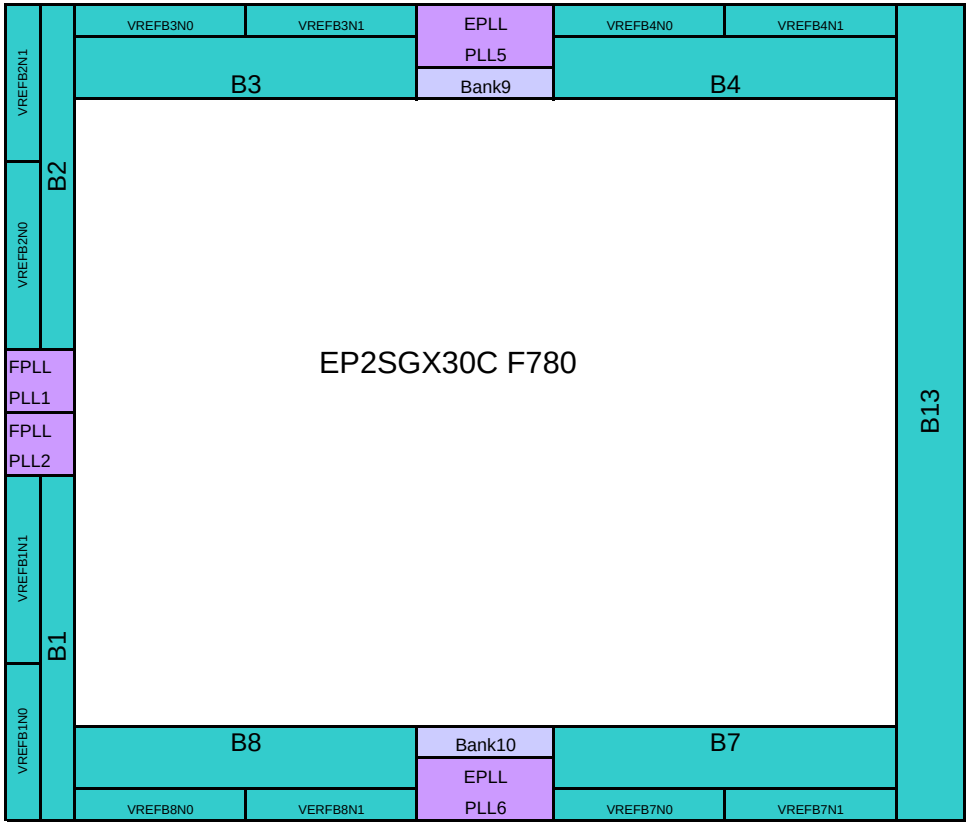
6) EP2SGX30 does not have the following signals: FPLL[8..7]CLK, PLL11_OUT[1,0], PLL12_OUT[1,0], PLL[12..11]_FBp/OUT2, VCC_PLL11_OUT, and VCC_PLL12_OUT.
EP2SGX60C/D does not have the following signals: FPLL[8..7]CLK, PLL11_OUT[1]p/n, PLL11_OUT[0]p, PLL12_OUT[1]p/n, PLL12_OUT[0]n, PLL[11]_FBp/OUT2p/n, PLL[12]_FBp/OUT2p, VCC_PLL11_OUT, and VCC_PLL12_OUT.

7) EP2SGX30C, EP2SGX30D, EP2SGX60C, and EP2SGX60D support either (18, x4) (8, x8/x9) or (4, x16/x18) DQ and DQS bus modes.
EP2SGX60E, EP2SGX90D, EP2SGX90F, and EP2SGX130G support either (36, x4) (18, x8/x9) or (8, x16/x18) DQ and DQS bus modes.

8) The number of VREF pins varies according to the device.
EP2SGX30 has 2 VREF pins per bank, VREFB[1..4,7,8]N[1..0].
EP2SGX60 and EP2SGX90 have 3 VREF pins per bank, VREFB[1..4,7,8]N[2..0].
EP2SGX130 has 5 VREF pins per bank, VREFB[1..4,7,8]N[4..0].



Notes:
1. This is a top view of the silicon die. For flip-chip packages, the die is mounted upside-down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.



Notes:

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Version History	Date	Changes Made
1.0	5/4/2006	Initial release
1.1	8/10/2006	Updated VCCL pins to VCCL_B[17..13] in Pin List and Pin Definitions
		Updated pin definitions for VCCPD[1..4,7,8]
		Removed Bank 7 reference for GND pin AC7 (F780) in Pin List
		Updated Bank & PLL Diagram with the correct number of VREFs per bank
		Added Note (8) for VREF in Pin Definitions
		Added VCCL in Note (3) in Pin Definitions
1.2	1/15/2007	Updated pin definition for REFCLK to mention that it is powered by 1.2-V VCCT
		Updated pin definition for VREF pins
		Updated Note (4) in Pin Definitions
		Corrected Note (3) in Pin List to mention EP2SGX30C.
1.3	12/14/2007	Updated pin descriptions for VCCIO, VCCINT, VCCPD, TEMPDIODEp, and TEMPDIODEn.