Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		VCCD_PLL7			L28							
		VCCA_PLL7			J29							
		GNDA_PLL7			K29							
		GNDA_PLL7			K28							
B2	VREFB2N0	FPLL7CLKp	INPUT		C39							
B2	VREFB2N0	FPLL7CLKn	INPUT		C38							
B2	VREFB2N0	IO	DIFFIO_TX77p		G33				DQ0L0		DQ0L0	
B2	VREFB2N0	IO	DIFFIO_TX77n		G32				DQ0L1		DQ0L1	
B2	VREFB2N0	IO	DIFFIO_RX76p		C37				DQS0L		DQS0L	
B2	VREFB2N0	IO	DIFFIO_RX76n		C36				DQ0L2		DQ0L2	
B2	VREFB2N0	IO	DIFFIO_TX76p		J32				DQ0L3		DQ0L3	
B2	VREFB2N0	IO	DIFFIO_TX76n		J31				DM0L			
B2	VREFB2N0	IO	DIFFIO_RX75p		D37				DQ1L0		DQ1L0	
B2	VREFB2N0	IO	DIFFIO_RX75n		D36				DQ1L1		DQ1L1	
B2	VREFB2N0	IO	DIFFIO_TX75p		K30				DQS1L		DQS1L	
B2	VREFB2N0	IO	DIFFIO_TX75n		L31				DQ1L2		DQ1L2	
B2	VREFB2N0	VREFB2N0	VREFB2N0		W35							
B2	VREFB2N0	IO	DIFFIO_RX74p		D39				DQ1L3		DQ1L3	
B2	VREFB2N0	IO	DIFFIO_RX74n		D38				DM1L			
B2	VREFB2N0	IO	DIFFIO_TX74p		K32				DQ2L0		DQ2L0	
B2	VREFB2N0	IO	DIFFIO_TX74n		K31				DQ2L1		DQ2L1	
B2	VREFB2N0	IO	DIFFIO_RX73p		F34				DQS2L		DQS2L	
B2	VREFB2N0	IO	DIFFIO_RX73n		F33				DQ2L2		DQ2L2	
B2	VREFB2N0	IO	DIFFIO_TX73p		K34				DQ2L3		DQ2L3	
B2	VREFB2N0	IO	DIFFIO_TX73n		K33				DM2L			
B2	VREFB2N0	IO	DIFFIO_RX72p		E37				DQ3L0		DQ3L0	
B2	VREFB2N0	IO	DIFFIO_RX72n		E36				DQ3L1		DQ3L1	
B2	VREFB2N0	IO	DIFFIO_TX72p		L34				DQS3L		DQS3L	
B2	VREFB2N0	IO	DIFFIO_TX72n		L33				DQ3L2		DQ3L2	
B2	VREFB2N0	IO	DIFFIO_RX71p		E39				DQ3L3		DQ3L3	
B2	VREFB2N0	IO	DIFFIO_RX71n		F39				DM3L			
B2	VREFB2N0	IO	DIFFIO_TX71p		L30				DQ4L0		DQ4L0	
B2	VREFB2N0	IO	DIFFIO_TX71n		M30				DQ4L1		DQ4L1	
B2	VREFB2N1	IO	DIFFIO_RX70p		F38				DQS4L		DQS4L	
B2	VREFB2N1	IO	DIFFIO_RX70n		F37				DQ4L2		DQ4L2	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B2	VREFB2N1	IO	DIFFIO_TX70p		M29				DQ4L3		DQ4L3	
B2	VREFB2N1	IO	DIFFIO_TX70n		N28				DM4L			
B2	VREFB2N1	IO	DIFFIO_RX69p		F36				DQ5L0		DQ5L0	
B2	VREFB2N1	IO	DIFFIO_RX69n		F35				DQ5L1		DQ5L1	
B2	VREFB2N1	IO	DIFFIO_TX69p		M32				DQS5L		DQS5L	
B2	VREFB2N1	IO	DIFFIO_TX69n		M31				DQ5L2		DQ5L2	
B2	VREFB2N1	IO	DIFFIO_RX68p		J34				DQ5L3		DQ5L3	
B2	VREFB2N1	IO	DIFFIO_RX68n		J33				DM5L			
B2	VREFB2N1	IO	DIFFIO_TX68p		N30				DQ6L0		DQ6L0	
B2	VREFB2N1	IO	DIFFIO_TX68n		N29				DQ6L1		DQ6L1	
B2	VREFB2N1	VREFB2N1	VREFB2N1		T36							
B2	VREFB2N1	IO	DIFFIO_RX67p		H34				DQS6L		DQS6L	
B2	VREFB2N1	IO	DIFFIO_RX67n		H33				DQ6L2		DQ6L2	
B2	VREFB2N1	IO	DIFFIO_RX66p		G35				DQ6L3		DQ6L3	
B2	VREFB2N1	IO	DIFFIO_RX66n		G34				DM6L			
B2	VREFB2N2	IO	DIFFIO_RX63p		G38				DQ7L0		DQ7L0	
B2	VREFB2N2	IO	DIFFIO_RX63n		G37				DQ7L1		DQ7L1	
B2	VREFB2N2	IO	DIFFIO_TX63p		N32				DQS7L		DQS7L	
B2	VREFB2N2	IO	DIFFIO_TX63n		N31				DQ7L2		DQ7L2	
B2	VREFB2N2	IO	DIFFIO_RX62p		H37				DQ7L3		DQ7L3	
B2	VREFB2N2	IO	DIFFIO_RX62n		H36				DM7L			
B2	VREFB2N2	IO	DIFFIO_TX62p		N34				DQ8L0		DQ8L0	
B2	VREFB2N2	IO	DIFFIO_TX62n		N33				DQ8L1		DQ8L1	
B2	VREFB2N2	IO	DIFFIO_RX61p		G39				DQS8L	DQS0L	DQS8L	DQS0L
B2	VREFB2N2	IO	DIFFIO_RX61n		H39				DQ8L2	DQ0L2	DQ8L2	DQ0L2
B2	VREFB2N2	IO	DIFFIO_TX61p		N27				DQ8L3	DQ13L3	DQ8L3	DQ13L3
B2	VREFB2N2	IO	DIFFIO_TX61n		P28				DM8L	DM13L		
B2	VREFB2N2	IO	DIFFIO_RX60p		M34				DQ9L0	DQ0L0	DQ9L0	DQ0L0
B2	VREFB2N2	IO	DIFFIO_RX60n		M33				DQ9L1	DQ0L1	DQ9L1	DQ0L1
B2	VREFB2N2	IO	DIFFIO_TX60p		P34				DQS9L		DQS9L	
B2	VREFB2N2	IO	DIFFIO_TX60n		P33				DQ9L2		DQ9L2	
B2	VREFB2N2	VREFB2N2	VREFB2N2		M35							
B2	VREFB2N2	IO	DIFFIO_RX59p		K36				DQ9L3	DQ0L3	DQ9L3	DQ0L3
B2	VREFB2N2	IO	DIFFIO_RX59n		K35				DM9L	DM0L		
B2	VREFB2N2	IO	DIFFIO_TX59p		P30				DQ10L0		DQ10L0	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B2	VREFB2N2	IO	DIFFIO_TX59n		R31				DQ10L1		DQ10L1	
B2	VREFB2N2	IO	DIFFIO_RX58p		J37				DQS10L	DQS13L	DQS10L	DQS13L
B2	VREFB2N2	IO	DIFFIO_RX58n		J36				DQ10L2	DQ13L2	DQ10L2	DQ13L2
B2	VREFB2N2	IO	DIFFIO_TX58p		R33				DQ10L3	DQS14L	DQ10L3	DQS14L
B2	VREFB2N2	IO	DIFFIO_TX58n		R32				DM10L	DQ14L2		DQ14L2
B2	VREFB2N2	IO	DIFFIO_RX57p		L37				DQ11L0	DQ1L0	DQ11L0	DQ1L0
B2	VREFB2N2	IO	DIFFIO_RX57n		L36				DQ11L1	DQ1L1	DQ11L1	DQ1L1
B2	VREFB2N2	IO	DIFFIO_TX57p		P27				DQS11L	DQ13L0	DQS11L	DQ13L0
B2	VREFB2N2	IO	DIFFIO_TX57n		R27				DQ11L2	DQ13L1	DQ11L2	DQ13L1
B2	VREFB2N2	IO	DIFFIO_RX56p		J39				DQ11L3		DQ11L3	
B2	VREFB2N2	IO	DIFFIO_RX56n		J38				DM11L			
B2	VREFB2N2	IO	DIFFIO_TX56p		R30				DQ12L0	DQ14L3	DQ12L0	DQ14L3
B2	VREFB2N2	IO	DIFFIO_TX56n		T29				DQ12L1	DM14L	DQ12L1	
B2	VREFB2N3	IO	DIFFIO_RX55p		K38				DQS12L	DQS1L	DQS12L	DQS1L
B2	VREFB2N3	IO	DIFFIO_RX55n		K37				DQ12L2	DQ1L2	DQ12L2	DQ1L2
B2	VREFB2N3	IO	DIFFIO_TX55p		T33				DQ12L3	DQ14L0	DQ12L3	DQ14L0
B2	VREFB2N3	IO	DIFFIO_TX55n		T32				DM12L	DQ14L1		DQ14L1
B2	VREFB2N3	IO	DIFFIO_RX54p		K39				DQ13L0	DQ1L3	DQ13L0	DQ1L3
B2	VREFB2N3	IO	DIFFIO_RX54n		L39				DQ13L1	DM1L	DQ13L1	
B2	VREFB2N3	IO	DIFFIO_TX54p		U34				DQS13L	DQS15L	DQS13L	DQS15L
B2	VREFB2N3	IO	DIFFIO_TX54n		U33				DQ13L2	DQ15L2	DQ13L2	DQ15L2
B2	VREFB2N3	IO	DIFFIO_RX53p		M37				DQ13L3	DQ2L0	DQ13L3	DQ2L0
B2	VREFB2N3	IO	DIFFIO_RX53n		M36				DM13L	DQ2L1		DQ2L1
B2	VREFB2N3	IO	DIFFIO_TX53p		T31				DQ14L0	DQ15L3	DQ14L0	DQ15L3
B2	VREFB2N3	IO	DIFFIO_TX53n		T30				DQ14L1	DM15L	DQ14L1	
B2	VREFB2N3	IO	DIFFIO_RX52p		N36				DQS14L	DQS2L	DQS14L	DQS2L
B2	VREFB2N3	IO	DIFFIO_RX52n		N35				DQ14L2	DQ2L2	DQ14L2	DQ2L2
B2	VREFB2N3	IO	DIFFIO_TX52p		R26				DQ14L3	DQ15L0	DQ14L3	DQ15L0
B2	VREFB2N3	IO	DIFFIO_TX52n		T26				DM14L	DQ15L1		DQ15L1
B2	VREFB2N3	VREFB2N3	VREFB2N3		J35							
B2	VREFB2N3	IO	DIFFIO_RX51p		M39				DQ15L0	DQ2L3	DQ15L0	DQ2L3
B2	VREFB2N3	IO	DIFFIO_RX51n		M38				DQ15L1	DM2L	DQ15L1	
B2	VREFB2N3	IO	DIFFIO_TX51p		T25				DQS15L		DQS15L	
B2	VREFB2N3	IO	DIFFIO_TX51n		T24				DQ15L2		DQ15L2	
B2	VREFB2N3	IO	DIFFIO_RX50p		N38				DQ15L3	DQ3L0	DQ15L3	DQ3L0

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B2	VREFB2N3	IO	DIFFIO_RX50n		N37				DM15L	DQ3L1		DQ3L1
B2	VREFB2N3	IO	DIFFIO_TX50p		T27				DQ16L0		DQ16L0	
B2	VREFB2N3	IO	DIFFIO_TX50n		U27				DQ16L1		DQ16L1	
B2	VREFB2N3	IO	DIFFIO_RX49p		N39				DQS16L	DQS3L	DQS16L	DQS3L
B2	VREFB2N3	IO	DIFFIO_RX49n		P39				DQ16L2	DQ3L2	DQ16L2	DQ3L2
B2	VREFB2N3	IO	DIFFIO_TX49p		U25				DQ16L3		DQ16L3	
B2	VREFB2N3	IO	DIFFIO_TX49n		V26				DM16L			
B2	VREFB2N3	IO	DIFFIO_RX48p		R35				DQ17L0	DQ3L3	DQ17L0	DQ3L3
B2	VREFB2N3	IO	DIFFIO_RX48n		R34				DQ17L1	DM3L	DQ17L1	
B2	VREFB2N3	IO	DIFFIO_TX48p		V25				DQS17L	DQ16L0	DQS17L	DQ16L0
B2	VREFB2N3	IO	DIFFIO_TX48n		W25				DQ17L2	DQ16L1	DQ17L2	DQ16L1
B2	VREFB2N4	IO	DIFFIO_RX47p		T35				DQ17L3	DQ4L0	DQ17L3	DQ4L0
B2	VREFB2N4	IO	DIFFIO_RX47n		T34				DM17L	DQ4L1		DQ4L1
B2	VREFB2N4	IO	DIFFIO_TX47p		V31				DQ18L0	DQS16L	DQ18L0	DQS16L
B2	VREFB2N4	IO	DIFFIO_TX47n		U30				DQ18L1	DQ16L2	DQ18L1	DQ16L2
B2	VREFB2N4	IO	DIFFIO_RX46p		P37				DQS18L	DQS4L	DQS18L	DQS4L
B2	VREFB2N4	IO	DIFFIO_RX46n		P36				DQ18L2	DQ4L2	DQ18L2	DQ4L2
B2	VREFB2N4	IO	DIFFIO_TX46p		W27				DQ18L3	DQ16L3	DQ18L3	DQ16L3
B2	VREFB2N4	IO	DIFFIO_TX46n		W26				DM18L	DM16L		
B2	VREFB2N4	IO	DIFFIO_RX45p		R37				DQ19L0	DQ4L3	DQ19L0	DQ4L3
B2	VREFB2N4	IO	DIFFIO_RX45n		R36				DQ19L1	DM4L	DQ19L1	
B2	VREFB2N4	IO	DIFFIO_TX45p		V28				DQS19L	DQ17L0	DQS19L	DQ17L0
B2	VREFB2N4	IO	DIFFIO_TX45n		V27				DQ19L2	DQ17L1	DQ19L2	DQ17L1
B2	VREFB2N4	IO	DIFFIO_RX44p		R39				DQ19L3	DQ5L0	DQ19L3	DQ5L0
B2	VREFB2N4	IO	DIFFIO_RX44n		R38				DM19L	DQ5L1		DQ5L1
B2	VREFB2N4	IO	DIFFIO_TX44p		V35				DQ20L0	DQS17L	DQ20L0	DQS17L
B2	VREFB2N4	IO	DIFFIO_TX44n		V34				DQ20L1	DQ17L2	DQ20L1	DQ17L2
B2	VREFB2N4	VREFB2N4	VREFB2N4		G36							
B2	VREFB2N4	IO	DIFFIO_RX43p		U37				DQS20L	DQS5L	DQS20L	DQS5L
B2	VREFB2N4	IO	DIFFIO_RX43n		U36				DQ20L2	DQ5L2	DQ20L2	DQ5L2
B2	VREFB2N4	IO	DIFFIO_TX43p		V33				DQ20L3	DQ17L3	DQ20L3	DQ17L3
B2	VREFB2N4	IO	DIFFIO_TX43n		V32				DM20L	DM17L		
B2	VREFB2N4	IO	DIFFIO_RX42p		T38				DQ21L0	DQ5L3	DQ21L0	DQ5L3
B2	VREFB2N4	IO	DIFFIO_RX42n		T37				DQ21L1	DM5L	DQ21L1	
B2	VREFB2N4	IO	DIFFIO_TX42p		W34				DQS21L	DQ18L0	DQS21L	DQ18L0

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B2	VREFB2N4	IO	DIFFIO_TX42n		W33				DQ21L2	DQ18L1	DQ21L2	DQ18L1
B2	VREFB2N4	IO	DIFFIO_RX41p		U39				DQ21L3	DQS18L	DQ21L3	DQS18L
B2	VREFB2N4	IO	DIFFIO_RX41n		T39				DM21L	DQ18L2		DQ18L2
B2	VREFB2N4	IO	DIFFIO_TX41p		W32					DQ18L3		DQ18L3
B2	VREFB2N4	IO	DIFFIO_TX41n		Y31					DM18L		
B2	VREFB2N4	IO	CLK0n/DIFFIO_RX_C0n		V38							
B2	VREFB2N4	IO	CLK0p/DIFFIO_RX_C0p		V39							
B2	VREFB2N4	CLK1n	INPUT		V36							
B2	VREFB2N4	CLK1p	INPUT		V37							
		VCCD_PLL1			W28							
		VCCA_PLL1			V30							
		GNDA_PLL1			W30							
		GNDA_PLL1			W29							
		GNDA_PLL2			Y28							
		GNDA_PLL2			AA29							
		VCCA_PLL2			Y30							
		VCCD_PLL2			AA28							
B1	VREFB1N0	IO	CLK2p/DIFFIO_RX_C1p		W39							
B1	VREFB1N0	IO	CLK2n/DIFFIO_RX_C1n		W38							
B1	VREFB1N0	CLK3p	INPUT		W37							
B1	VREFB1N0	CLK3n	INPUT		W36							
B1	VREFB1N0	IO	DIFFIO_RX40p		Y37				DQ22L0	DQ6L0	DQ22L0	DQ6L0
B1	VREFB1N0	IO	DIFFIO_RX40n		Y36				DQ22L1	DQ6L1	DQ22L1	DQ6L1
B1	VREFB1N0	IO	DIFFIO_TX40p		Y25				DQS22L	DQ19L0	DQS22L	DQ19L0
B1	VREFB1N0	IO	DIFFIO_TX40n		AA25				DQ22L2	DQ19L1	DQ22L2	DQ19L1
B1	VREFB1N0	IO	DIFFIO_RX39p		AA39				DQ22L3	DQS6L	DQ22L3	DQS6L
B1	VREFB1N0	IO	DIFFIO_RX39n		Y39				DM22L	DQ6L2		DQ6L2
B1	VREFB1N0	IO	DIFFIO_TX39p		Y27				DQ23L0	DQS19L	DQ23L0	DQS19L
B1	VREFB1N0	IO	DIFFIO_TX39n		AA26				DQ23L1	DQ19L2	DQ23L1	DQ19L2
B1	VREFB1N0	IO	DIFFIO_RX38p		AA38				DQS23L	DQ6L3	DQS23L	DQ6L3
B1	VREFB1N0	IO	DIFFIO_RX38n		AA37				DQ23L2	DM6L	DQ23L2	
B1	VREFB1N0	IO	DIFFIO_TX38p		AA27				DQ23L3	DQ19L3	DQ23L3	DQ19L3
B1	VREFB1N0	IO	DIFFIO_TX38n		AB27				DM23L	DM19L		
B1	VREFB1N0	VREFB1N0	VREFB1N0		AP35							
B1	VREFB1N0	IO	DIFFIO_RX37p		AA35				DQ24L0	DQ7L0	DQ24L0	DQ7L0

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B1	VREFB1N0	IO	DIFFIO_RX37n		AA34				DQ24L1	DQ7L1	DQ24L1	DQ7L1
B1	VREFB1N0	IO	DIFFIO_TX37p		Y34				DQS24L	DQ20L0	DQS24L	DQ20L0
B1	VREFB1N0	IO	DIFFIO_TX37n		Y33				DQ24L2	DQ20L1	DQ24L2	DQ20L1
B1	VREFB1N0	IO	DIFFIO_RX36p		AB39				DQ24L3	DQS7L	DQ24L3	DQS7L
B1	VREFB1N0	IO	DIFFIO_RX36n		AB38				DM24L	DQ7L2		DQ7L2
B1	VREFB1N0	IO	DIFFIO_TX36p		AA32				DQ25L0	DQS20L	DQ25L0	DQS20L
B1	VREFB1N0	IO	DIFFIO_TX36n		AA31				DQ25L1	DQ20L2	DQ25L1	DQ20L2
B1	VREFB1N0	IO	DIFFIO_RX35p		AB37				DQS25L	DQ7L3	DQS25L	DQ7L3
B1	VREFB1N0	IO	DIFFIO_RX35n		AB36				DQ25L2	DM7L	DQ25L2	
B1	VREFB1N0	IO	DIFFIO_TX35p		AB25				DQ25L3	DQ20L3	DQ25L3	DQ20L3
B1	VREFB1N0	IO	DIFFIO_TX35n		AC25				DM25L	DM20L		
B1	VREFB1N0	IO	DIFFIO_RX34p		AB35				DQ26L0	DQ8L0	DQ26L0	DQ8L0
B1	VREFB1N0	IO	DIFFIO_RX34n		AB34				DQ26L1	DQ8L1	DQ26L1	DQ8L1
B1	VREFB1N0	IO	DIFFIO_TX34p		AB26				DQS26L	DQ21L0	DQS26L	DQ21L0
B1	VREFB1N0	IO	DIFFIO_TX34n		AC27				DQ26L2	DQ21L1	DQ26L2	DQ21L1
B1	VREFB1N1	IO	DIFFIO_RX33p		AC37				DQ26L3	DQS8L	DQ26L3	DQS8L
B1	VREFB1N1	IO	DIFFIO_RX33n		AC36				DM26L	DQ8L2		DQ8L2
B1	VREFB1N1	IO	DIFFIO_TX33p		AB30				DQ27L0	DQS21L	DQ27L0	DQS21L
B1	VREFB1N1	IO	DIFFIO_TX33n		AB29				DQ27L1	DQ21L2	DQ27L1	DQ21L2
B1	VREFB1N1	IO	DIFFIO_RX32p		AC39				DQS27L	DQ8L3	DQS27L	DQ8L3
B1	VREFB1N1	IO	DIFFIO_RX32n		AD39				DQ27L2	DM8L	DQ27L2	
B1	VREFB1N1	IO	DIFFIO_TX32p		AB32				DQ27L3	DQ21L3	DQ27L3	DQ21L3
B1	VREFB1N1	IO	DIFFIO_TX32n		AB31				DM27L	DM21L		
B1	VREFB1N1	IO	DIFFIO_RX31p		AD35				DQ28L0	DQ9L0	DQ28L0	DQ9L0
B1	VREFB1N1	IO	DIFFIO_RX31n		AD34				DQ28L1	DQ9L1	DQ28L1	DQ9L1
B1	VREFB1N1	IO	DIFFIO_TX31p		AA33				DQS28L	DQ22L0	DQS28L	DQ22L0
B1	VREFB1N1	IO	DIFFIO_TX31n		AB33				DQ28L2	DQ22L1	DQ28L2	DQ22L1
B1	VREFB1N1	IO	DIFFIO_RX30p		AD38				DQ28L3	DQS9L	DQ28L3	DQS9L
B1	VREFB1N1	IO	DIFFIO_RX30n		AD37				DM28L	DQ9L2		DQ9L2
B1	VREFB1N1	IO	DIFFIO_TX30p		AD26				DQ29L0		DQ29L0	
B1	VREFB1N1	IO	DIFFIO_TX30n		AD25				DQ29L1		DQ29L1	
B1	VREFB1N1	VREFB1N1	VREFB1N1		AL35							
B1	VREFB1N1	IO	DIFFIO_RX29p		AE39				DQS29L	DQ9L3	DQS29L	DQ9L3
B1	VREFB1N1	IO	DIFFIO_RX29n		AE38				DQ29L2	DM9L	DQ29L2	
B1	VREFB1N1	IO	DIFFIO_TX29p		AE27				DQ29L3	DQ22L3	DQ29L3	DQ22L3

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B1	VREFB1N1	IO	DIFFIO_TX29n		AE26				DM29L	DM22L		
B1	VREFB1N1	IO	DIFFIO_RX28p		AE37				DQ30L0	DQ10L0	DQ30L0	DQ10L0
B1	VREFB1N1	IO	DIFFIO_RX28n		AE36				DQ30L1	DQ10L1	DQ30L1	DQ10L1
B1	VREFB1N1	IO	DIFFIO_TX28p		AC34				DQS30L	DQ23L0	DQS30L	DQ23L0
B1	VREFB1N1	IO	DIFFIO_TX28n		AC33				DQ30L2	DQ23L1	DQ30L2	DQ23L1
B1	VREFB1N1	IO	DIFFIO_RX27p		AF39				DQ30L3	DQS10L	DQ30L3	DQS10L
B1	VREFB1N1	IO	DIFFIO_RX27n		AG39				DM30L	DQ10L2		DQ10L2
B1	VREFB1N1	IO	DIFFIO_TX27p		AC30				DQ31L0	DQS22L	DQ31L0	DQS22L
B1	VREFB1N1	IO	DIFFIO_TX27n		AD30				DQ31L1	DQ22L2	DQ31L1	DQ22L2
B1	VREFB1N1	IO	DIFFIO_RX26p		AE35				DQS31L		DQS31L	
B1	VREFB1N1	IO	DIFFIO_RX26n		AE34				DQ31L2		DQ31L2	
B1	VREFB1N1	IO	DIFFIO_TX26p		AD32				DQ31L3	DQ23L3	DQ31L3	DQ23L3
B1	VREFB1N1	IO	DIFFIO_TX26n		AD31				DM31L	DM23L		
B1	VREFB1N2	IO	DIFFIO_RX25p		AF37				DQ32L0		DQ32L0	
B1	VREFB1N2	IO	DIFFIO_RX25n		AF36				DQ32L1		DQ32L1	
B1	VREFB1N2	IO	DIFFIO_TX25p		AD33				DQS32L	DQ24L0	DQS32L	DQ24L0
B1	VREFB1N2	IO	DIFFIO_TX25n		AE33				DQ32L2	DQ24L1	DQ32L2	DQ24L1
B1	VREFB1N2	IO	DIFFIO_RX24p		AG38				DQ32L3	DQS11L	DQ32L3	DQS11L
B1	VREFB1N2	IO	DIFFIO_RX24n		AG37				DM32L	DQ11L2		DQ11L2
B1	VREFB1N2	IO	DIFFIO_TX24p		AD27				DQ33L0	DQS23L	DQ33L0	DQS23L
B1	VREFB1N2	IO	DIFFIO_TX24n		AE28				DQ33L1	DQ23L2	DQ33L1	DQ23L2
B1	VREFB1N2	IO	DIFFIO_RX23p		AG36				DQS33L	DQ10L3	DQS33L	DQ10L3
B1	VREFB1N2	IO	DIFFIO_RX23n		AG35				DQ33L2	DM10L	DQ33L2	
B1	VREFB1N2	IO	DIFFIO_TX23p		AE32				DQ33L3	DQ24L3	DQ33L3	DQ24L3
B1	VREFB1N2	IO	DIFFIO_TX23n		AE31				DM33L	DM24L		
B1	VREFB1N2	IO	DIFFIO_RX22p		AH39				DQ34L0	DQ25L0	DQ34L0	DQ25L0
B1	VREFB1N2	IO	DIFFIO_RX22n		AH38				DQ34L1	DQ25L1	DQ34L1	DQ25L1
B1	VREFB1N2	IO	DIFFIO_TX22p		AF34				DQS34L	DQS24L	DQS34L	DQS24L
B1	VREFB1N2	IO	DIFFIO_TX22n		AF33				DQ34L2	DQ24L2	DQ34L2	DQ24L2
B1	VREFB1N2	VREFB1N2	VREFB1N2		AH35							
B1	VREFB1N2	IO	DIFFIO_RX21p		AH37				DQ34L3	DQ11L0	DQ34L3	DQ11L0
B1	VREFB1N2	IO	DIFFIO_RX21n		AH36				DM34L	DQ11L1		DQ11L1
B1	VREFB1N2	IO	DIFFIO_TX21p		AE30				DQ35L0	DQS25L	DQ35L0	DQS25L
B1	VREFB1N2	IO	DIFFIO_TX21n		AE29				DQ35L1	DQ25L2	DQ35L1	DQ25L2
B1	VREFB1N2	IO	DIFFIO_RX20p		AJ39				DQS35L	DQ11L3	DQS35L	DQ11L3

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B1	VREFB1N2	IO	DIFFIO_RX20n		AK39				DQ35L2	DM11L	DQ35L2	
B1	VREFB1N2	IO	DIFFIO_TX20p		AF28				DQ35L3		DQ35L3	
B1	VREFB1N2	IO	DIFFIO_TX20n		AF27				DM35L			
B1	VREFB1N2	IO	DIFFIO_RX19p		AJ37				DQ36L0	DQ25L3	DQ36L0	DQ25L3
B1	VREFB1N2	IO	DIFFIO_RX19n		AJ36				DQ36L1	DM25L	DQ36L1	
B1	VREFB1N2	IO	DIFFIO_TX19p		AG34				DQS36L		DQS36L	
B1	VREFB1N2	IO	DIFFIO_TX19n		AG33				DQ36L2		DQ36L2	
B1	VREFB1N2	IO	DIFFIO_RX18p		AK38				DQ36L3		DQ36L3	
B1	VREFB1N2	IO	DIFFIO_RX18n		AK37				DM36L			
B1	VREFB1N2	IO	DIFFIO_TX18p		AF30				DQ37L0		DQ37L0	
B1	VREFB1N2	IO	DIFFIO_TX18n		AG30				DQ37L1		DQ37L1	
B1	VREFB1N3	IO	DIFFIO_RX14p		AL37				DQS37L		DQS37L	
B1	VREFB1N3	IO	DIFFIO_RX14n		AL36				DQ37L2		DQ37L2	
B1	VREFB1N3	IO	DIFFIO_TX14p		AG28				DQ37L3		DQ37L3	
B1	VREFB1N3	IO	DIFFIO_TX14n		AG27				DM37L			
B1	VREFB1N3	VREFB1N3	VREFB1N3		AD36							
B1	VREFB1N3	IO	DIFFIO_RX13p		AK36				DQ38L0		DQ38L0	
B1	VREFB1N3	IO	DIFFIO_RX13n		AK35				DQ38L1		DQ38L1	
B1	VREFB1N3	IO	DIFFIO_TX13p		AG32				DQS38L		DQS38L	
B1	VREFB1N3	IO	DIFFIO_TX13n		AG31				DQ38L2		DQ38L2	
B1	VREFB1N3	IO	DIFFIO_RX12p		AL39				DQ38L3		DQ38L3	
B1	VREFB1N3	IO	DIFFIO_RX12n		AL38				DM38L			
B1	VREFB1N3	IO	DIFFIO_TX12p		AH34				DQ39L0		DQ39L0	
B1	VREFB1N3	IO	DIFFIO_TX12n		AH33				DQ39L1		DQ39L1	
B1	VREFB1N3	IO	DIFFIO_RX11p		AM37				DQS39L		DQS39L	
B1	VREFB1N3	IO	DIFFIO_RX11n		AM36				DQ39L2		DQ39L2	
B1	VREFB1N3	IO	DIFFIO_TX11p		AH32				DQ39L3		DQ39L3	
B1	VREFB1N3	IO	DIFFIO_TX11n		AH31				DM39L			
B1	VREFB1N3	IO	DIFFIO_RX10p		AN39				DQ40L0		DQ40L0	
B1	VREFB1N3	IO	DIFFIO_RX10n		AM39				DQ40L1		DQ40L1	
B1	VREFB1N3	IO	DIFFIO_TX10p		AJ34				DQS40L		DQS40L	
B1	VREFB1N3	IO	DIFFIO_TX10n		AJ33				DQ40L2		DQ40L2	
B1	VREFB1N3	IO	DIFFIO_RX9p		AN38				DQ40L3		DQ40L3	
B1	VREFB1N3	IO	DIFFIO_RX9n		AN37				DM40L			
B1	VREFB1N3	IO	DIFFIO_TX9p		AH30				DQ41L0		DQ41L0	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B1	VREFB1N3	IO	DIFFIO_TX9n		AH29				DQ41L1		DQ41L1	
B1	VREFB1N4	IO	DIFFIO_RX8p		AP39				DQS41L		DQS41L	
B1	VREFB1N4	IO	DIFFIO_RX8n		AP38				DQ41L2		DQ41L2	
B1	VREFB1N4	IO	DIFFIO_TX8p		AK34				DQ41L3		DQ41L3	
B1	VREFB1N4	IO	DIFFIO_TX8n		AK33				DM41L			
B1	VREFB1N4	IO	DIFFIO_RX7p		AN36				DQ42L0		DQ42L0	
B1	VREFB1N4	IO	DIFFIO_RX7n		AN35				DQ42L1		DQ42L1	
B1	VREFB1N4	IO	DIFFIO_TX7p		AL34				DQS42L		DQS42L	
B1	VREFB1N4	IO	DIFFIO_TX7n		AL33				DQ42L2		DQ42L2	
B1	VREFB1N4	IO	DIFFIO_RX6p		AP37				DQ42L3		DQ42L3	
B1	VREFB1N4	IO	DIFFIO_RX6n		AP36				DM42L			
B1	VREFB1N4	IO	DIFFIO_TX6p		AK32				DQ43L0		DQ43L0	
B1	VREFB1N4	IO	DIFFIO_TX6n		AK31				DQ43L1		DQ43L1	
B1	VREFB1N4	IO	DIFFIO_RX5p		AR39				DQS43L		DQS43L	
B1	VREFB1N4	IO	DIFFIO_RX5n		AT39				DQ43L2		DQ43L2	
B1	VREFB1N4	IO	DIFFIO_TX5p		AM34				DQ43L3		DQ43L3	
B1	VREFB1N4	IO	DIFFIO_TX5n		AM33				DM43L			
B1	VREFB1N4	VREFB1N4	VREFB1N4		AA36							
B1	VREFB1N4	IO	DIFFIO_RX4p		AR37				DQ44L0		DQ44L0	
B1	VREFB1N4	IO	DIFFIO_RX4n		AR36				DQ44L1		DQ44L1	
B1	VREFB1N4	IO	DIFFIO_TX4p		AL32				DQS44L		DQS44L	
B1	VREFB1N4	IO	DIFFIO_TX4n		AL31				DQ44L2		DQ44L2	
B1	VREFB1N4	IO	DIFFIO_RX3p		AT38				DQ44L3		DQ44L3	
B1	VREFB1N4	IO	DIFFIO_RX3n		AT37				DM44L			
B1	VREFB1N4	IO	DIFFIO_TX3p		AN34				DQ45L0		DQ45L0	
B1	VREFB1N4	IO	DIFFIO_TX3n		AN33				DQ45L1		DQ45L1	
B1	VREFB1N4	IO	DIFFIO_RX2p		AU37				DQS45L		DQS45L	
B1	VREFB1N4	IO	DIFFIO_RX2n		AU36				DQ45L2		DQ45L2	
B1	VREFB1N4	IO	DIFFIO_TX2p		AJ30				DQ45L3		DQ45L3	
B1	VREFB1N4	IO	DIFFIO_TX2n		AK30				DM45L			
B1	VREFB1N4	IO	DIFFIO_RX1p		AT36							
B1	VREFB1N4	IO	DIFFIO_RX1n		AT35							
B1	VREFB1N4	IO	DIFFIO_TX1p		AM31							
B1	VREFB1N4	IO	DIFFIO_TX1n		AN32							
B1	VREFB1N4	FPLL8CLKn	INPUT		AU38							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B1	VREFB1N4	FPLL8CLKp	INPUT		AU39							
B1	VREFB1N4	IO	DIFFIO_TX0p		AM30							
B1	VREFB1N4	IO	DIFFIO_TX0n		AL30							
		GNDA_PLL8			AK28							
		GNDA_PLL8			AK29							
		VCCA_PLL8			AL29							
		VCCD_PLL8			AJ28							
B8	VREFB8N0	TDI		TDI	AP34							
B8	VREFB8N0	TMS		TMS	AP33							
B8	VREFB8N0	TCK		TCK	AU35							
B8	VREFB8N0	TRST		TRST	AP32							
B8	VREFB8N0	nCONFIG		nCONFIG	AR34							
B8	VREFB8N0	VCCSEL		VCCSEL	AT34							
B8	VREFB8N0	IO			AN31				DQ0B0		DQ0B0	
B8	VREFB8N0	IO			AN30				DQ0B1		DQ0B1	
B8	VREFB8N0	IO		CS	AR33							
B8	VREFB8N0	IO		CLKUSR	AT33							
B8	VREFB8N0	IO		nWS	AU34							
B8	VREFB8N0	IO		nRS	AT32							
B8	VREFB8N0	VREFB8N0	VREFB8N0		AR31							
B8	VREFB8N0	IO			AP31				DQS0B		DQS0B	
B8	VREFB8N0	IO			AP30				DQ0B2		DQ0B2	
B8	VREFB8N0	IO			AT31				DQ0B3		DQ0B3	
B8	VREFB8N0	IO			AH28				DM0B			
B8	VREFB8N0	IO			AN29				DQ1B0		DQ1B0	
B8	VREFB8N0	IO	DQ17B		AW37	DQ8B			DQ1B1		DQ1B1	
B8	VREFB8N0	IO	DQSn17B		AV36	DQ8B	DQ3B	DQ1B	DQS1B		DQS1B	
B8	VREFB8N0	IO	DQ17B		AV37	DQ8B	DQ3B		DQ1B2		DQ1B2	
B8	VREFB8N0	IO	DQ17B		AV34	DQ8B	DQ3B	DQ1B	DQ1B3		DQ1B3	
B8	VREFB8N0	IO	DQ17B		AW35	DQ8B	DQ3B	DQ1B	DM1B			
B8	VREFB8N0	IO	DQS17B		AW36	DQVLD8B			DQ2B0		DQ2B0	
B8	VREFB8N1	IO			AT30				DQ2B1		DQ2B1	
B8	VREFB8N1	IO			AL28				DQS2B		DQS2B	
B8	VREFB8N1	IO			AP29				DQ2B2		DQ2B2	
B8	VREFB8N1	IO			AM28				DQ2B3		DQ2B3	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B8	VREFB8N1	IO	DQ16B		AW34	DQ8B	DQ3B	DQ1B	DM2B			
B8	VREFB8N1	IO	DQSn16B		AV33	DQSn8B	DQ3B	DQ1B	DQ3B0		DQ3B0	
B8	VREFB8N1	IO	DQ16B		AU33	DQ8B	DQ3B	DQ1B	DQ3B1		DQ3B1	
B8	VREFB8N1	IO	DQ16B		AU32	DQ8B	DQ3B	DQ1B	DQS3B		DQS3B	
B8	VREFB8N1	IO	DQ16B		AW32	DQ8B	DQ3B	DQ1B	DQ3B2		DQ3B2	
B8	VREFB8N1	IO	DQS16B		AW33	DQS8B	DQVLD3B		DQ3B3		DQ3B3	
B8	VREFB8N1	VREFB8N1	VREFB8N1		AR30							
B8	VREFB8N1	IO			AL27				DM3B			
B8	VREFB8N1	IO			AN28				DQ4B0		DQ4B0	
B8	VREFB8N1	IO			AK27				DQ4B1		DQ4B1	
B8	VREFB8N1	IO	DQ15B		AU31	DQ7B	DQ3B	DQ1B	DQS4B		DQS4B	
B8	VREFB8N1	IO	DQSn15B		AV31	DQ7B	DQSn3B	DQ1B	DQ4B2		DQ4B2	
B8	VREFB8N1	IO	DQ15B		AW31	DQ7B	DQ3B	DQ1B	DQ4B3		DQ4B3	
B8	VREFB8N1	IO	DQ15B		AW30	DQ7B	DQ3B	DQ1B	DM4B			
B8	VREFB8N1	IO	DQ15B		AU30	DQ7B	DQ3B	DQ1B	DQ5B0		DQ5B0	
B8	VREFB8N1	IO	DQS15B		AV30	DQVLD7B	DQS3B		DQ5B1		DQ5B1	
B8	VREFB8N2	IO			AP28				DQS5B		DQS5B	
B8	VREFB8N2	IO			AM27				DQ5B2		DQ5B2	
B8	VREFB8N2	IO			AN27				DQ5B3		DQ5B3	
B8	VREFB8N2	IO			AJ27				DM5B			
B8	VREFB8N2	IO	DQ14B		AT29	DQ7B	DQ3B	DQ1B	DQ6B0		DQ6B0	
B8	VREFB8N2	IO	DQSn14B		AU29	DQSn7B	DQ3B	DQ1B	DQ6B1		DQ6B1	
B8	VREFB8N2	IO	DQ14B		AR28	DQ7B	DQ3B	DQ1B	DQS6B		DQS6B	
B8	VREFB8N2	IO	DQ14B		AW29	DQ7B	DQ3B	DQ1B	DQ6B2		DQ6B2	
B8	VREFB8N2	IO	DQ14B		AT28	DQ7B	DQ3B	DQ1B	DQ6B3		DQ6B3	
B8	VREFB8N2	IO	DQS14B		AU28	DQS7B			DM6B			
B8	VREFB8N2	VREFB8N2	VREFB8N2		AR27							
B8	VREFB8N2	IO			AH27				DQ7B0		DQ7B0	
B8	VREFB8N2	IO			AH26				DQ7B1		DQ7B1	
B8	VREFB8N2	IO			AP27				DQS7B		DQS7B	
B8	VREFB8N2	IO			AN26				DQ7B2		DQ7B2	
B8	VREFB8N2	IO			AG26				DQ7B3		DQ7B3	
B8	VREFB8N2	IO	DQ13B		AT27	DQ6B			DM7B			
B8	VREFB8N2	IO	DQSn13B		AV28	DQ6B	DQ2B	DQSn1B	DQ8B0		DQ8B0	
B8	VREFB8N2	IO	DQ13B		AW28	DQ6B	DQ2B	DQ1B	DQ8B1		DQ8B1	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B8	VREFB8N2	IO	DQ13B		AW27	DQ6B	DQ2B	DQ1B	DQS8B		DQS8B	
B8	VREFB8N2	IO	DQ13B		AU27	DQ6B	DQ2B	DQ1B	DQ8B2		DQ8B2	
B8	VREFB8N2	IO	DQS13B		AV27	DQVLD6B		DQS1B	DQ8B3		DQ8B3	
B8	VREFB8N3	IO			AK25				DM8B			
B8	VREFB8N3	IO			AL25				DQ9B0		DQ9B0	
B8	VREFB8N3	IO			AM25				DQ9B1		DQ9B1	
B8	VREFB8N3	IO			AJ25				DQS9B		DQS9B	
B8	VREFB8N3	IO			AH25				DQ9B2		DQ9B2	
B8	VREFB8N3	IO	DQ12B		AW26	DQ6B	DQ2B	DQ1B	DQ9B3		DQ9B3	
B8	VREFB8N3	IO	DQSn12B		AT26	DQSn6B	DQ2B	DQ1B	DM9B			
B8	VREFB8N3	IO	DQ12B		AU26	DQ6B	DQ2B	DQ1B	DQ10B0		DQ10B0	
B8	VREFB8N3	IO	DQ12B		AR25	DQ6B	DQ2B	DQ1B	DQ10B1		DQ10B1	
B8	VREFB8N3	IO	DQ12B		AP25	DQ6B	DQ2B	DQ1B	DQS10B		DQS10B	
B8	VREFB8N3	IO	DQS12B		AT25	DQS6B	DQVLD2B	DQVLD1B	DQ10B2		DQ10B2	
B8	VREFB8N3	VREFB8N3	VREFB8N3		AR24							
B8	VREFB8N3	IO			AK24				DQ10B3		DQ10B3	
B8	VREFB8N3	IO			AF25				DM10B			
B8	VREFB8N3	IO			AG25				DQ11B0		DQ11B0	
B8	VREFB8N3	IO			AL24				DQ11B1		DQ11B1	
B8	VREFB8N3	IO			AH24				DQS11B		DQS11B	
B8	VREFB8N3	IO			AE25				DQ11B2		DQ11B2	
B8	VREFB8N3	IO	DQ11B		AV25	DQ5B	DQ2B	DQ1B	DQ11B3		DQ11B3	
B8	VREFB8N3	IO	DQSn11B		AU25	DQ5B	DQSn2B	DQ1B	DM11B			
B8	VREFB8N3	IO	DQ11B		AW25	DQ5B	DQ2B	DQ1B	DQ12B0		DQ12B0	
B8	VREFB8N3	IO	DQ11B		AP24	DQ5B	DQ2B	DQ1B	DQ12B1		DQ12B1	
B8	VREFB8N3	IO	DQ11B		AT24	DQ5B	DQ2B	DQ1B	DQS12B		DQS12B	
B8	VREFB8N3	IO	DQS11B		AU24	DQVLD5B	DQS2B		DQ12B2		DQ12B2	
B8	VREFB8N3	IO			AF24				DQ12B3		DQ12B3	
B8	VREFB8N3	IO			AG24				DM12B			
B8	VREFB8N3	IO			AP26				DQ13B0		DQ13B0	
B8	VREFB8N3	IO			AN25				DQ13B1		DQ13B1	
B8	VREFB8N4	IO			AG23				DQS13B		DQS13B	
B8	VREFB8N4	IO			AE24				DQ13B2		DQ13B2	
B8	VREFB8N4	IO	DQ10B		AV24	DQ5B	DQ2B	DQ1B	DQ13B3		DQ13B3	
B8	VREFB8N4	IO	DQSn10B		AT23	DQSn5B	DQ2B	DQ1B	DM13B			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B8	VREFB8N4	IO	DQ10B		AW24	DQ5B	DQ2B	DQ1B	DQ14B0		DQ14B0	
B8	VREFB8N4	IO	DQ10B		AW23	DQ5B	DQ2B	DQ1B	DQ14B1		DQ14B1	
B8	VREFB8N4	IO	DQ10B		AP23	DQ5B	DQ2B	DQ1B	DQS14B		DQS14B	
B8	VREFB8N4	IO	DQS10B		AU23	DQS5B			DQ14B2		DQ14B2	
B8	VREFB8N4	VREFB8N4	VREFB8N4		AR21							
B8	VREFB8N4	IO			AE23				DQ14B3		DQ14B3	
B8	VREFB8N4	IO			AE22				DM14B			
B8	VREFB8N4	IO			AM24							
B8	VREFB8N4	IO			AN24							
B8	VREFB8N4	IO		RUnLU	AL21							
B8	VREFB8N4	IO		DEV_OE	AM21							
B8	VREFB8N4	IO		DEV_CLRn	AM22							
B8	VREFB8N4	IO		nCS	AN23							
B12	VREFB8N4	IO	PLL12_FBn/OUT2n		AN22							
B12	VREFB8N4	IO	PLL12_FBp/OUT2p		AP22							
B8	VREFB8N4	IO			AF22							
B8	VREFB8N4	IO			AG22							
B12	VREFB8N4	IO	PLL12_OUT1n		AR22							
B12	VREFB8N4	IO	PLL12_OUT1p		AT21							
B12	VREFB8N4	IO	PLL12_OUT0n		AT22							
B12	VREFB8N4	IO	PLL12_OUT0p		AU22							
B8	VREFB8N4	IO	CLK5n		AN21							
B8	VREFB8N4	IO	CLK5p		AP21							
B8	VREFB8N4	IO	CLK4n		AV22							
B8	VREFB8N4	IO	CLK4p		AW22							
B12		VCC_PLL12_OUT			AJ24							
		VCCD_PLL12			AJ21							
		VCCA_PLL12			AL22							
		GNDA_PLL12			AK22							
		GNDA_PLL12			AJ22							
		GNDA_PLL6			AK20							
		VCCA_PLL6			AL20							
		VCCD_PLL6			AJ19							
		GNDA_PLL6			AK19							
B10		VCC_PLL6_OUT			AJ18							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B7	VREFB7N0	IO	CLK7p		AV21							
B7	VREFB7N0	IO	CLK7n		AU21							
B7	VREFB7N0	IO	CLK6p		AW20							
B7	VREFB7N0	IO	CLK6n		AW21							
B10	VREFB7N0	IO	PLL6_OUT1p		AU20							
B10	VREFB7N0	IO	PLL6_OUT1n		AT20							
B10	VREFB7N0	IO	PLL6_OUT0p		AW19							
B10	VREFB7N0	IO	PLL6_OUT0n		AV19							
B10	VREFB7N0	IO	PLL6_FBp/OUT2p		AP20							
B10	VREFB7N0	IO	PLL6_FBn/OUT2n		AN20							
B7	VREFB7N0	IO			AM19				DQ15B0		DQ15B0	
B7	VREFB7N0	IO			AG21				DQ15B1		DQ15B1	
B7	VREFB7N0	VREFB7N0	VREFB7N0		AR19							
B7	VREFB7N0	IO			AH20				DQS15B		DQS15B	
B7	VREFB7N0	IO	DQ9B		AN19	DQ4B			DQ15B2		DQ15B2	
B7	VREFB7N0	IO	DQSn9B		AP19	DQ4B	DQ1B	DQ0B	DQ15B3		DQ15B3	
B7	VREFB7N0	IO	DQ9B		AU19	DQ4B	DQ1B		DM15B			
B7	VREFB7N0	IO	DQ9B		AT19	DQ4B	DQ1B	DQ0B	DQ16B0		DQ16B0	
B7	VREFB7N0	IO	DQ9B		AN18	DQ4B	DQ1B	DQ0B	DQ16B1		DQ16B1	
B7	VREFB7N0	IO	DQS9B		AP18	DQVLD4B			DQS16B		DQS16B	
B7	VREFB7N0	IO			AF21				DQ16B2		DQ16B2	
B7	VREFB7N0	IO			AL18				DQ16B3		DQ16B3	
B7	VREFB7N1	IO			AK18				DM16B			
B7	VREFB7N1	IO	DQ8B		AR18	DQ4B	DQ1B	DQ0B	DQ17B0		DQ17B0	
B7	VREFB7N1	IO	DQSn8B		AU18	DQSn4B	DQ1B	DQ0B	DQ17B1		DQ17B1	
B7	VREFB7N1	IO	DQ8B		AW17	DQ4B	DQ1B	DQ0B	DQS17B		DQS17B	
B7	VREFB7N1	IO	DQ8B		AT18	DQ4B	DQ1B	DQ0B	DQ17B2		DQ17B2	
B7	VREFB7N1	IO	DQ8B		AW18	DQ4B	DQ1B	DQ0B	DQ17B3		DQ17B3	
B7	VREFB7N1	IO	DQS8B		AV18	DQS4B	DQVLD1B		DM17B			
B7	VREFB7N1	IO			AG20				DQ18B0		DQ18B0	
B7	VREFB7N1	IO			AM18				DQ18B1		DQ18B1	
B7	VREFB7N1	VREFB7N1	VREFB7N1		AR16							
B7	VREFB7N1	IO	DQ7B		AP17	DQ3B	DQ1B	DQ0B	DQS18B		DQS18B	
B7	VREFB7N1	IO	DQSn7B		AU17	DQ3B	DQSn1B	DQ0B	DQ18B2		DQ18B2	
B7	VREFB7N1	IO	DQ7B		AV16	DQ3B	DQ1B	DQ0B	DQ18B3		DQ18B3	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B7	VREFB7N1	IO	DQ7B		AW16	DQ3B	DQ1B	DQ0B	DM18B			
B7	VREFB7N1	IO	DQ7B		AN17	DQ3B	DQ1B	DQ0B	DQ19B0		DQ19B0	
B7	VREFB7N1	IO	DQS7B		AT17	DQVLD3B	DQS1B		DQ19B1		DQ19B1	
B7	VREFB7N1	IO			AE20				DQS19B		DQS19B	
B7	VREFB7N1	IO			AE21				DQ19B2		DQ19B2	
B7	VREFB7N1	IO			AG19				DQ19B3		DQ19B3	
B7	VREFB7N2	IO			AF19				DM19B			
B7	VREFB7N2	IO	DQ6B		AT16	DQ3B	DQ1B	DQ0B	DQ20B0		DQ20B0	
B7	VREFB7N2	IO	DQSn6B		AP16	DQSn3B	DQ1B	DQ0B	DQ20B1		DQ20B1	
B7	VREFB7N2	IO	DQ6B		AU16	DQ3B	DQ1B	DQ0B	DQS20B		DQS20B	
B7	VREFB7N2	IO	DQ6B		AN15	DQ3B	DQ1B	DQ0B	DQ20B2		DQ20B2	
B7	VREFB7N2	IO	DQ6B		AN16	DQ3B	DQ1B	DQ0B	DQ20B3		DQ20B3	
B7	VREFB7N2	IO	DQS6B		AP15	DQS3B			DM20B			
B7	VREFB7N2	IO			AE19				DQ21B0		DQ21B0	
B7	VREFB7N2	IO			AK16				DQ21B1		DQ21B1	
B7	VREFB7N2	IO			AG18				DQS21B		DQS21B	
B7	VREFB7N2	IO			AL16				DQ21B2		DQ21B2	
B7	VREFB7N2	VREFB7N2	VREFB7N2		AR13							
B7	VREFB7N2	IO			AE18				DQ21B3		DQ21B3	
B7	VREFB7N2	IO			AF18				DM21B			
B7	VREFB7N2	IO	DQ5B		AW15	DQ2B			DQ22B0		DQ22B0	
B7	VREFB7N2	IO	DQSn5B		AV15	DQ2B	DQ0B	DQSn0B	DQ22B1		DQ22B1	
B7	VREFB7N2	IO	DQ5B		AW14	DQ2B	DQ0B	DQ0B	DQS22B		DQS22B	
B7	VREFB7N2	IO	DQ5B		AR15	DQ2B	DQ0B	DQ0B	DQ22B2		DQ22B2	
B7	VREFB7N2	IO	DQ5B		AT15	DQ2B	DQ0B	DQ0B	DQ22B3		DQ22B3	
B7	VREFB7N2	IO	DQS5B		AU15	DQVLD2B		DQS0B	DM22B			
B7	VREFB7N2	IO			AH16				DQ23B0		DQ23B0	
B7	VREFB7N2	IO			AJ16				DQ23B1		DQ23B1	
B7	VREFB7N2	IO			AG17				DQS23B		DQS23B	
B7	VREFB7N2	IO			AM16				DQ23B2		DQ23B2	
B7	VREFB7N3	IO			AE17				DQ23B3		DQ23B3	
B7	VREFB7N3	IO			AK15				DM23B			
B7	VREFB7N3	IO	DQ4B		AP14	DQ2B	DQ0B	DQ0B	DQ24B0		DQ24B0	
B7	VREFB7N3	IO	DQSn4B		AU14	DQSn2B	DQ0B	DQ0B	DQ24B1		DQ24B1	
B7	VREFB7N3	IO	DQ4B		AV13	DQ2B	DQ0B	DQ0B	DQS24B		DQS24B	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B7	VREFB7N3	IO	DQ4B		AN14	DQ2B	DQ0B	DQ0B	DQ24B2		DQ24B2	
B7	VREFB7N3	IO	DQ4B		AW13	DQ2B	DQ0B	DQ0B	DQ24B3		DQ24B3	
B7	VREFB7N3	IO	DQS4B		AT14	DQS2B	DQVLD0B	DQVLD0B	DM24B			
B7	VREFB7N3	IO			AJ15				DQ25B0		DQ25B0	
B7	VREFB7N3	IO			AG16				DQ25B1		DQ25B1	
B7	VREFB7N3	IO			AL15				DQS25B		DQS25B	
B7	VREFB7N3	IO			AM15				DQ25B2		DQ25B2	
B7	VREFB7N3	VREFB7N3	VREFB7N3		AP11							
B7	VREFB7N3	IO			AE16				DQ25B3		DQ25B3	
B7	VREFB7N3	IO			AF16				DM25B			
B7	VREFB7N3	IO	DQ3B		AU13	DQ1B	DQ0B	DQ0B	DQ26B0		DQ26B0	
B7	VREFB7N3	IO	DQSn3B		AP13	DQ1B	DQSn0B	DQ0B	DQ26B1		DQ26B1	
B7	VREFB7N3	IO	DQ3B		AN12	DQ1B	DQ0B	DQ0B	DQS26B		DQS26B	
B7	VREFB7N3	IO	DQ3B		AT13	DQ1B	DQ0B	DQ0B	DQ26B2		DQ26B2	
B7	VREFB7N3	IO	DQ3B		AN13	DQ1B	DQ0B	DQ0B	DQ26B3		DQ26B3	
B7	VREFB7N3	IO	DQS3B		AP12	DQVLD1B	DQS0B		DM26B			
B7	VREFB7N3	IO			AF15				DQ27B0		DQ27B0	
B7	VREFB7N3	IO			AG15				DQ27B1		DQ27B1	
B7	VREFB7N3	IO			AH15				DQS27B		DQS27B	
B7	VREFB7N3	IO			AM13				DQ27B2		DQ27B2	
B7	VREFB7N4	IO			AE15				DQ27B3		DQ27B3	
B7	VREFB7N4	IO			AE14				DM27B			
B7	VREFB7N4	IO	DQ2B		AW12	DQ1B	DQ0B	DQ0B	DQ28B0		DQ28B0	
B7	VREFB7N4	IO	DQSn2B		AV12	DQSn1B	DQ0B	DQ0B	DQ28B1		DQ28B1	
B7	VREFB7N4	IO	DQ2B		AR12	DQ1B	DQ0B	DQ0B	DQS28B		DQS28B	
B7	VREFB7N4	IO	DQ2B		AW11	DQ1B	DQ0B	DQ0B	DQ28B2		DQ28B2	
B7	VREFB7N4	IO	DQ2B		AT12	DQ1B	DQ0B	DQ0B	DQ28B3		DQ28B3	
B7	VREFB7N4	IO	DQS2B		AU12	DQS1B			DM28B			
B7	VREFB7N4	IO			AK13				DQ29B0		DQ29B0	
B7	VREFB7N4	IO			AL13				DQ29B1		DQ29B1	
B7	VREFB7N4	IO	DQ1B		AW10	DQ0B			DQS29B		DQS29B	
B7	VREFB7N4	IO	DQSn1B		AU11	DQ0B			DQ29B2		DQ29B2	
B7	VREFB7N4	VREFB7N4	VREFB7N4		AR10							
B7	VREFB7N4	IO	DQ1B		AN11	DQ0B			DQ29B3		DQ29B3	
B7	VREFB7N4	IO	DQ1B		AU10	DQ0B			DM29B			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B7	VREFB7N4	IO	DQ1B		AV10	DQ0B			DQ30B0		DQ30B0	
B7	VREFB7N4	IO	DQS1B		AT11	DQVLD0B			DQ30B1		DQ30B1	
B7	VREFB7N4	IO	RDN7		AH14							
B7	VREFB7N4	IO	RUP7		AG14							
B7	VREFB7N4	IO	DQ0B		AW9	DQ0B			DQS30B		DQS30B	
B7	VREFB7N4	IO	DQSn0B		AT10	DQSn0B			DQ30B2		DQ30B2	
B7	VREFB7N4	IO	DQ0B		AP10	DQ0B			DQ30B3		DQ30B3	
B7	VREFB7N4	IO	DQ0B		AN10	DQ0B			DM30B			
B7	VREFB7N4	IO	DQ0B		AU9	DQ0B						
B7	VREFB7N4	IO	DQS0B		AT9	DQS0B						
B7	VREFB7N4	PORSEL		PORSEL	AL10							
B7	VREFB7N4	nIO_PULLUP		nIO_PULLUP	AL11							
B7	VREFB7N4	PLL_ENA		PLL_ENA	AL12							
		GND			AM12							
B7	VREFB7N4	nCEO		nCEO	AM10							
B16		GXB_RX15n			AL2							
B16		GXB_RX15p			AL1							
B16		GXB_TX15n			AL5							
B16		GXB_TX15p			AL4							
B16		GXB_RX14n			AJ2							
B16		GXB_RX14p			AJ1							
B16		GXB_TX14n			AJ5							
B16		GXB_TX14p			AJ4							
B16		RREFB16			AD7							
B16		REFCLK0_B16n			AH8							
B16		REFCLK0_B16p			AH7							
B16		REFCLK1_B16n			AF8							
B16		REFCLK1_B16p			AF7							
		VCCL_B16			AE9							
		VCCA			AF12							
		VCCA			AD9							
		VCCA			AF10							
		GND			AF11							
B16		GXB_RX12n			AG2							
B16		GXB_RX12p			AG1							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B16		GXB_TX12n			AG5							
B16		GXB_TX12p			AG4							
B16		GXB_RX13n			AE2							
B16		GXB_RX13p			AE1							
B16		GXB_TX13n			AE5							
B16		GXB_TX13p			AE4							
B15		GXB_RX11n			AC2							
B15		GXB_RX11p			AC1							
B15		GXB_TX11n			AC5							
B15		GXB_TX11p			AC4							
B15		GXB_RX10n			AA2							
B15		GXB_RX10p			AA1							
B15		GXB_TX10n			AA5							
B15		GXB_TX10p			AA4							
B15		RREFB15			Y7							
B15		REFCLK0_B15n			AB8							
B15		REFCLK0_B15p			AB7							
B15		REFCLK1_B15n			V8							
B15		REFCLK1_B15p			V7							
		VCCL_B15			AA9							
		VCCA			AB12							
		VCCA			Y9							
		VCCA			AB10							
		GND			AB11							
B15		GXB_RX8n			W2							
B15		GXB_RX8p			W1							
B15		GXB_TX8n			W5							
B15		GXB_TX8p			W4							
B15		GXB_RX9n			U2							
B15		GXB_RX9p			U1							
B15		GXB_TX9n			U5							
B15		GXB_TX9p			U4							
B17		GXB_RX19n			AW4							
B17		GXB_RX19p			AW3							
B17		GXB_TX19n			AW7							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B17		GXB_TX19p			AW6							
B17		GXB_RX18n			AU2							
B17		GXB_RX18p			AU1							
B17		GXB_TX18n			AU5							
B17		GXB_TX18p			AU4							
B17		RREFB17			AK7							
B17		REFCLK0_B17n			AP8							
B17		REFCLK0_B17p			AP7							
B17		REFCLK1_B17n			AM8							
B17		REFCLK1_B17p			AM7							
		VCCL_B17			AJ9							
		VCCA			AK12							
		VCCA			AH9							
		VCCA			AK10							
		GND			AK11							
B17		GXB_RX16n			AR2							
B17		GXB_RX16p			AR1							
B17		GXB_TX16n			AR5							
B17		GXB_TX16p			AR4							
B17		GXB_RX17n			AN2							
B17		GXB_RX17p			AN1							
B17		GXB_TX17n			AN5							
B17		GXB_TX17p			AN4							
		NC			V10							
		NC			V11							
		VCCA			V12							
B14		GXB_RX7n			R2							
B14		GXB_RX7p			R1							
B14		GXB_TX7n			R5							
B14		GXB_TX7p			R4							
B14		GXB_RX6n			N2							
B14		GXB_RX6p			N1							
B14		GXB_TX6n			N5							
B14		GXB_TX6p			N4							
B14		RREFB14			T7							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B14		REFCLK0_B14n			P8							
B14		REFCLK0_B14p			P7							
B14		REFCLK1_B14n			M8							
B14		REFCLK1_B14p			M7							
		VCCL_B14			T9							
		VCCA			U12							
		VCCA			R9							
		VCCA			U10							
		GND			U11							
B14		GXB_RX4n			L2							
B14		GXB_RX4p			L1							
B14		GXB_TX4n			L5							
B14		GXB_TX4p			L4							
B14		GXB_RX5n			J2							
B14		GXB_RX5p			J1							
B14		GXB_TX5n			J5							
B14		GXB_TX5p			J4							
B13		GXB_RX3n			G2							
B13		GXB_RX3p			G1							
B13		GXB_TX3n			G5							
B13		GXB_TX3p			G4							
B13		GXB_RX2n			E2							
B13		GXB_RX2p			E1							
B13		GXB_TX2n			E5							
B13		GXB_TX2p			E4							
B13		RREFB13			K7							
B13		REFCLK0_B13n			H8							
B13		REFCLK0_B13p			H7							
B13		REFCLK1_B13n			F8							
B13		REFCLK1_B13p			F7							
		VCCL_B13			M9							
		VCCA			N12							
		VCCA			L9							
		VCCA			N10							
		GND			N11							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B13		GXB_RX0n			C2							
B13		GXB_RX0p			C1							
B13		GXB_TX0n			C5							
B13		GXB_TX0p			C4							
B13		GXB_RX1n			A4							
B13		GXB_RX1p			A3							
B13		GXB_TX1n			A7							
B13		GXB_TX1p			A6							
		TEMPDIODEp			H10							
		TEMPDIODEn			J10							
B4	VREFB4N0	TDO		TDO	H13							
B4	VREFB4N0	MSEL3		MSEL3	H12							
B4	VREFB4N0	MSEL2		MSEL2	J13							
B4	VREFB4N0	MSEL1		MSEL1	J12							
B4	VREFB4N0	MSEL0		MSEL0	J11							
B4	VREFB4N0	IO	DQS0T		D9	DQS0T						
B4	VREFB4N0	IO	DQ0T		C9	DQ0T						
B4	VREFB4N0	IO	DQ0T		G10	DQ0T			DM29T			
B4	VREFB4N0	IO	DQ0T		F10	DQ0T			DQ29T3		DQ29T3	
B4	VREFB4N0	IO	DQSn0T		D10	DQSn0T			DQ29T2		DQ29T2	
B4	VREFB4N0	IO	DQ0T		A9	DQ0T			DQS29T		DQS29T	
B4	VREFB4N0	IO	RUP4		N13							
B4	VREFB4N0	IO	RDN4		N14							
B4	VREFB4N0	IO	DQS1T		D11	DQVLD0T			DQ29T1		DQ29T1	
B4	VREFB4N0	IO	DQ1T		C10	DQ0T			DQ29T0		DQ29T0	
B4	VREFB4N0	IO	DQ1T		A10	DQ0T			DM28T			
B4	VREFB4N0	IO	DQ1T		G11	DQ0T			DQ28T3		DQ28T3	
B4	VREFB4N0	VREFB4N0	VREFB4N0		E10							
B4	VREFB4N0	IO	DQSn1T		C11	DQ0T			DQ28T2		DQ28T2	
B4	VREFB4N0	IO	DQ1T		B10	DQ0T			DQS28T		DQS28T	
B4	VREFB4N0	IO			M14				DQ28T1		DQ28T1	
B4	VREFB4N0	IO			R14				DQ28T0		DQ28T0	
B4	VREFB4N0	IO	DQS2T		C12	DQS1T			DM27T			
B4	VREFB4N0	IO	DQ2T		D12	DQ1T	DQ0T	DQ0T	DQ27T3		DQ27T3	
B4	VREFB4N0	IO	DQ2T		A11	DQ1T	DQ0T	DQ0T	DQ27T2		DQ27T2	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B4	VREFB4N0	IO	DQ2T		E12	DQ1T	DQ0T	DQ0T	DQS27T		DQS27T	
B4	VREFB4N0	IO	DQSn2T		B12	DQSn1T	DQ0T	DQ0T	DQ27T1		DQ27T1	
B4	VREFB4N0	IO	DQ2T		A12	DQ1T	DQ0T	DQ0T	DQ27T0		DQ27T0	
B4	VREFB4N0	IO			R15				DM26T			
B4	VREFB4N1	IO			H15				DQ26T3		DQ26T3	
B4	VREFB4N1	IO			N15				DQ26T2		DQ26T2	
B4	VREFB4N1	IO			P15				DQS26T		DQS26T	
B4	VREFB4N1	IO	DQS3T		D13	DQVLD1T	DQS0T		DQ26T1		DQ26T1	
B4	VREFB4N1	IO	DQ3T		B13	DQ1T	DQ0T	DQ0T	DQ26T0		DQ26T0	
B4	VREFB4N1	IO	DQ3T		G12	DQ1T	DQ0T	DQ0T	DM25T			
B4	VREFB4N1	IO	DQ3T		F12	DQ1T	DQ0T	DQ0T	DQ25T3		DQ25T3	
B4	VREFB4N1	IO	DQSn3T		C13	DQ1T	DQSn0T	DQ0T	DQ25T2		DQ25T2	
B4	VREFB4N1	IO	DQ3T		A13	DQ1T	DQ0T	DQ0T	DQS25T		DQS25T	
B4	VREFB4N1	IO			M15				DQ25T1		DQ25T1	
B4	VREFB4N1	VREFB4N1	VREFB4N1		F11							
B4	VREFB4N1	IO			J15				DQ25T0		DQ25T0	
B4	VREFB4N1	IO			K15				DM24T			
B4	VREFB4N1	IO	DQS4T		F13	DQS2T	DQVLD0T	DQVLD0T	DQ24T3		DQ24T3	
B4	VREFB4N1	IO	DQ4T		D14	DQ2T	DQ0T	DQ0T	DQ24T2		DQ24T2	
B4	VREFB4N1	IO	DQ4T		G13	DQ2T	DQ0T	DQ0T	DQS24T		DQS24T	
B4	VREFB4N1	IO	DQ4T		G14	DQ2T	DQ0T	DQ0T	DQ24T1		DQ24T1	
B4	VREFB4N1	IO	DQSn4T		F14	DQSn2T	DQ0T	DQ0T	DQ24T0		DQ24T0	
B4	VREFB4N1	IO	DQ4T		C14	DQ2T	DQ0T	DQ0T	DM23T			
B4	VREFB4N1	IO			L15				DQ23T3		DQ23T3	
B4	VREFB4N2	IO			H16				DQ23T2		DQ23T2	
B4	VREFB4N2	IO			R16				DQS23T		DQS23T	
B4	VREFB4N2	IO	DQS5T		C15	DQVLD2T		DQS0T	DQ23T1		DQ23T1	
B4	VREFB4N2	IO	DQ5T		D15	DQ2T	DQ0T	DQ0T	DQ23T0		DQ23T0	
B4	VREFB4N2	IO	DQ5T		E15	DQ2T	DQ0T	DQ0T	DM22T			
B4	VREFB4N2	IO	DQ5T		A14	DQ2T	DQ0T	DQ0T	DQ22T3		DQ22T3	
B4	VREFB4N2	IO	DQSn5T		B15	DQ2T	DQ0T	DQSn0T	DQ22T2		DQ22T2	
B4	VREFB4N2	IO	DQ5T		A15	DQ2T			DQS22T		DQS22T	
B4	VREFB4N2	IO			M16				DQ22T1		DQ22T1	
B4	VREFB4N2	VREFB4N2	VREFB4N2		E13							
B4	VREFB4N2	IO			J16				DQ22T0		DQ22T0	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B4	VREFB4N2	IO			K16				DM21T			
B4	VREFB4N2	IO			L16				DQ21T3		DQ21T3	
B4	VREFB4N2	IO	DQS6T		D16	DQS3T			DQ21T2		DQ21T2	
B4	VREFB4N2	IO	DQ6T		B16	DQ3T	DQ1T	DQ0T	DQS21T		DQS21T	
B4	VREFB4N2	IO	DQ6T		G15	DQ3T	DQ1T	DQ0T	DQ21T1		DQ21T1	
B4	VREFB4N2	IO	DQ6T		F15	DQ3T	DQ1T	DQ0T	DQ21T0		DQ21T0	
B4	VREFB4N2	IO	DQSn6T		C16	DQSn3T	DQ1T	DQ0T	DM20T			
B4	VREFB4N2	IO	DQ6T		A16	DQ3T	DQ1T	DQ0T	DQ20T3		DQ20T3	
B4	VREFB4N2	IO			N16				DQ20T2		DQ20T2	
B4	VREFB4N2	IO			P16				DQS20T		DQS20T	
B4	VREFB4N3	IO			R18				DQ20T1		DQ20T1	
B4	VREFB4N3	IO			P18				DQ20T0		DQ20T0	
B4	VREFB4N3	IO			N17				DM19T			
B4	VREFB4N3	IO			R17				DQ19T3		DQ19T3	
B4	VREFB4N3	IO	DQS7T		F16	DQVLD3T	DQS1T		DQ19T2		DQ19T2	
B4	VREFB4N3	IO	DQ7T		G17	DQ3T	DQ1T	DQ0T	DQS19T		DQS19T	
B4	VREFB4N3	IO	DQ7T		D17	DQ3T	DQ1T	DQ0T	DQ19T1		DQ19T1	
B4	VREFB4N3	IO	DQ7T		G16	DQ3T	DQ1T	DQ0T	DQ19T0		DQ19T0	
B4	VREFB4N3	IO	DQSn7T		F17	DQ3T	DQSn1T	DQ0T	DM18T			
B4	VREFB4N3	IO	DQ7T		C17	DQ3T	DQ1T	DQ0T	DQ18T3		DQ18T3	
B4	VREFB4N3	IO			N18				DQ18T2		DQ18T2	
B4	VREFB4N3	IO			P19				DQS18T		DQS18T	
B4	VREFB4N3	VREFB4N3	VREFB4N3		E16							
B4	VREFB4N3	IO			H18				DQ18T1		DQ18T1	
B4	VREFB4N3	IO			R20				DQ18T0		DQ18T0	
B4	VREFB4N3	IO			R19				DM17T			
B4	VREFB4N3	IO			N19				DQ17T3		DQ17T3	
B4	VREFB4N3	IO	DQS8T		B18	DQS4T	DQVLD1T		DQ17T2		DQ17T2	
B4	VREFB4N3	IO	DQ8T		A18	DQ4T	DQ1T	DQ0T	DQS17T		DQS17T	
B4	VREFB4N3	IO	DQ8T		A17	DQ4T	DQ1T	DQ0T	DQ17T1		DQ17T1	
B4	VREFB4N3	IO	DQ8T		D18	DQ4T	DQ1T	DQ0T	DQ17T0		DQ17T0	
B4	VREFB4N3	IO	DQSn8T		C18	DQSn4T	DQ1T	DQ0T	DM16T			
B4	VREFB4N3	IO	DQ8T		E18	DQ4T	DQ1T	DQ0T	DQ16T3		DQ16T3	
B4	VREFB4N3	IO			J18				DQ16T2		DQ16T2	
B4	VREFB4N3	IO			K18				DQS16T		DQS16T	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B4	VREFB4N4	IO			H19				DQ16T1		DQ16T1	
B4	VREFB4N4	IO			P21				DQ16T0		DQ16T0	
B4	VREFB4N4	IO			R21				DM15T			
B4	VREFB4N4	IO			N20				DQ15T3		DQ15T3	
B4	VREFB4N4	IO	DQS9T		F18	DQVLD4T			DQ15T2		DQ15T2	
B4	VREFB4N4	IO	DQ9T		D19	DQ4T	DQ1T	DQ0T	DQS15T		DQS15T	
B4	VREFB4N4	IO	DQ9T		G18	DQ4T	DQ1T	DQ0T	DQ15T1		DQ15T1	
B4	VREFB4N4	IO	DQ9T		C19	DQ4T	DQ1T		DQ15T0		DQ15T0	
B4	VREFB4N4	VREFB4N4	VREFB4N4		E19							
B4	VREFB4N4	IO	DQSn9T		F19	DQ4T	DQ1T	DQ0T	DM14T			
B4	VREFB4N4	IO	DQ9T		G19	DQ4T			DQ14T3		DQ14T3	
B4	VREFB4N4	IO			N21				DQ14T2		DQ14T2	
B4	VREFB4N4	IO			M20				DQS14T		DQS14T	
B4	VREFB4N4	IO			J21				DQ14T1		DQ14T1	
B4	VREFB4N4	IO			H21				DQ14T0		DQ14T0	
B9	VREFB4N4	IO	PLL5_FBn/OUT2n		G20							
B9	VREFB4N4	IO	PLL5_FBp/OUT2p		F20							
B9	VREFB4N4	IO	PLL5_OUT0n		B19							
B9	VREFB4N4	IO	PLL5_OUT0p		A19							
B9	VREFB4N4	IO	PLL5_OUT1n		D20							
B9	VREFB4N4	IO	PLL5_OUT1p		C20							
B4	VREFB4N4	IO	CLK12n		A21							
B4	VREFB4N4	IO	CLK12p		A20							
B4	VREFB4N4	IO	CLK13n		C21							
B4	VREFB4N4	IO	CLK13p		B21							
B9		VCC_PLL5_OUT			L18							
		VCCD_PLL5			L19							
		VCCA_PLL5			J20							
		GNDA_PLL5			K19							
		GNDA_PLL5			K20							
		GNDA_PLL11			K22							
		GNDA_PLL11			L22							
		VCCA_PLL11			J22							
		VCCD_PLL11			L21							
B11		VCC_PLL11_OUT			L24							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B3	VREFB3N0	IO	CLK14p		C22							
B3	VREFB3N0	IO	CLK14n		D21							
B3	VREFB3N0	IO	CLK15p		F21							
B3	VREFB3N0	IO	CLK15n		G21							
B11	VREFB3N0	IO	PLL11_OUT0p		A22							
B11	VREFB3N0	IO	PLL11_OUT0n		B22							
B11	VREFB3N0	IO	PLL11_OUT1p		D22							
B11	VREFB3N0	IO	PLL11_OUT1n		E22							
B11	VREFB3N0	IO	PLL11_FBp/OUT2p		F22							
B11	VREFB3N0	IO	PLL11_FBn/OUT2n		G22							
B3	VREFB3N0	IO		PGM2	G23							
B3	VREFB3N0	IO		PGM1	H22							
B3	VREFB3N0	IO		PGM0	N22							
B3	VREFB3N0	IO		ASDO	P22							
B3	VREFB3N0	IO		nCSO	G24							
B3	VREFB3N0	IO		CRC_ERROR	H24							
B3	VREFB3N0	IO		DATA0	J24							
B3	VREFB3N0	IO		DATA1	R22							
B3	VREFB3N0	VREFB3N0	VREFB3N0		E21							
B3	VREFB3N0	IO	DQS10T		C23	DQS5T						
B3	VREFB3N0	IO	DQ10T		F23	DQ5T	DQ2T	DQ1T				
B3	VREFB3N0	IO	DQ10T		A23	DQ5T	DQ2T	DQ1T				
B3	VREFB3N0	IO	DQ10T		A24	DQ5T	DQ2T	DQ1T				
B3	VREFB3N0	IO	DQSn10T		D23	DQSn5T	DQ2T	DQ1T	DM13T			
B3	VREFB3N0	IO	DQ10T		B24	DQ5T	DQ2T	DQ1T	DQ13T4		DQ13T4	
B3	VREFB3N1	IO			N23				DQ13T2		DQ13T2	
B3	VREFB3N1	IO			R23				DQS13T		DQS13T	
B3	VREFB3N1	IO	DQS11T		C24	DQVLD5T	DQS2T		DQ13T1		DQ13T1	
B3	VREFB3N1	IO	DQ11T		D24	DQ5T	DQ2T	DQ1T	DQ13T0		DQ13T0	
B3	VREFB3N1	IO	DQ11T		F24	DQ5T	DQ2T	DQ1T	DM12T			
B3	VREFB3N1	IO	DQ11T		A25	DQ5T	DQ2T	DQ1T	DQ12T3		DQ12T3	
B3	VREFB3N1	IO	DQSn11T		C25	DQ5T	DQSn2T	DQ1T	DQ12T2		DQ12T2	
B3	VREFB3N1	IO	DQ11T		B25	DQ5T	DQ2T	DQ1T	DQS12T		DQS12T	
B3	VREFB3N1	IO			G25				DQ12T1		DQ12T1	
B3	VREFB3N1	IO			M24				DQ12T0		DQ12T0	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B3	VREFB3N1	IO			K24				DM11T			
B3	VREFB3N1	VREFB3N1	VREFB3N1		E24							
B3	VREFB3N1	IO	DQS12T		D25	DQS6T	DQVLD2T	DQVLD1T	DQ11T3		DQ11T3	
B3	VREFB3N1	IO	DQ12T		F25	DQ6T	DQ2T	DQ1T	DQ11T2		DQ11T2	
B3	VREFB3N1	IO	DQ12T		E25	DQ6T	DQ2T	DQ1T	DQS11T		DQS11T	
B3	VREFB3N1	IO	DQ12T		C26	DQ6T	DQ2T	DQ1T	DQ11T1		DQ11T1	
B3	VREFB3N1	IO	DQSn12T		D26	DQSn6T	DQ2T	DQ1T	DQ11T0		DQ11T0	
B3	VREFB3N1	IO	DQ12T		A26	DQ6T	DQ2T	DQ1T	DM10T			
B3	VREFB3N1	IO			N24				DQ10T3		DQ10T3	
B3	VREFB3N1	IO			H25				DQ10T2		DQ10T2	
B3	VREFB3N1	IO			J25				DQS10T		DQS10T	
B3	VREFB3N1	IO			P24				DQ10T1		DQ10T1	
B3	VREFB3N1	IO			R24				DQ10T0		DQ10T0	
B3	VREFB3N2	IO	DQS13T		B27	DQVLD6T		DQS1T	DM9T			
B3	VREFB3N2	IO	DQ13T		D27	DQ6T	DQ2T	DQ1T	DQ9T3		DQ9T3	
B3	VREFB3N2	IO	DQ13T		A27	DQ6T	DQ2T	DQ1T	DQ9T2		DQ9T2	
B3	VREFB3N2	IO	DQ13T		A28	DQ6T	DQ2T	DQ1T	DQS9T		DQS9T	
B3	VREFB3N2	IO	DQSn13T		B28	DQ6T	DQ2T	DQSn1T	DQ9T1		DQ9T1	
B3	VREFB3N2	IO	DQ13T		C27	DQ6T			DQ9T0		DQ9T0	
B3	VREFB3N2	IO			K25				DM8T			
B3	VREFB3N2	IO			L25				DQ8T3		DQ8T3	
B3	VREFB3N2	IO			F26				DQ8T2		DQ8T2	
B3	VREFB3N2	IO			G26				DQS8T		DQS8T	
B3	VREFB3N2	IO			M25				DQ8T1		DQ8T1	
B3	VREFB3N2	IO			N25				DQ8T0		DQ8T0	
B3	VREFB3N2	VREFB3N2	VREFB3N2		E27							
B3	VREFB3N2	IO	DQS14T		C28	DQS7T			DM7T			
B3	VREFB3N2	IO	DQ14T		D28	DQ7T	DQ3T	DQ1T	DQ7T3		DQ7T3	
B3	VREFB3N2	IO	DQ14T		A29	DQ7T	DQ3T	DQ1T	DQ7T2		DQ7T2	
B3	VREFB3N2	IO	DQ14T		E28	DQ7T	DQ3T	DQ1T	DQS7T		DQS7T	
B3	VREFB3N2	IO	DQSn14T		C29	DQSn7T	DQ3T	DQ1T	DQ7T1		DQ7T1	
B3	VREFB3N2	IO	DQ14T		D29	DQ7T	DQ3T	DQ1T	DQ7T0		DQ7T0	
B3	VREFB3N2	IO			P25				DM6T			
B3	VREFB3N2	IO			R25				DQ6T3		DQ6T3	
B3	VREFB3N2	IO			F27				DQ6T2		DQ6T2	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B3	VREFB3N2	IO			H27				DQS6T		DQS6T	
B3	VREFB3N2	IO			G27				DQ6T1		DQ6T1	
B3	VREFB3N2	IO			M26				DQ6T0		DQ6T0	
B3	VREFB3N3	IO	DQS15T		B30	DQVLD7T	DQS3T		DM5T			
B3	VREFB3N3	IO	DQ15T		C30	DQ7T	DQ3T	DQ1T	DQ5T3		DQ5T3	
B3	VREFB3N3	IO	DQ15T		A31	DQ7T	DQ3T	DQ1T	DQ5T2		DQ5T2	
B3	VREFB3N3	IO	DQ15T		A30	DQ7T	DQ3T	DQ1T	DQS5T		DQS5T	
B3	VREFB3N3	IO	DQSn15T		B31	DQ7T	DQSn3T	DQ1T	DQ5T1		DQ5T1	
B3	VREFB3N3	IO	DQ15T		C31	DQ7T	DQ3T	DQ1T	DQ5T0		DQ5T0	
B3	VREFB3N3	IO			N26				DM4T			
B3	VREFB3N3	IO			J27				DQ4T3		DQ4T3	
B3	VREFB3N3	IO			F28				DQ4T2		DQ4T2	
B3	VREFB3N3	IO			G28				DQS4T		DQS4T	
B3	VREFB3N3	IO			M27				DQ4T1		DQ4T1	
B3	VREFB3N3	IO			K27				DQ4T0		DQ4T0	
B3	VREFB3N3	VREFB3N3	VREFB3N3		E30							
B3	VREFB3N3	IO	DQS16T		A33	DQS8T	DQVLD3T		DM3T			
B3	VREFB3N3	IO	DQ16T		A32	DQ8T	DQ3T	DQ1T	DQ3T3		DQ3T3	
B3	VREFB3N3	IO	DQ16T		C32	DQ8T	DQ3T	DQ1T	DQ3T2		DQ3T2	
B3	VREFB3N3	IO	DQ16T		C33	DQ8T	DQ3T	DQ1T	DQS3T		DQS3T	
B3	VREFB3N3	IO	DQSn16T		B33	DQSn8T	DQ3T	DQ1T	DQ3T1		DQ3T1	
B3	VREFB3N3	IO	DQ16T		A34	DQ8T	DQ3T	DQ1T	DQ3T0		DQ3T0	
B3	VREFB3N3	IO			H28				DM2T			
B3	VREFB3N3	IO			L27				DQ2T3		DQ2T3	
B3	VREFB3N3	IO			F29				DQ2T2		DQ2T2	
B3	VREFB3N3	IO			J28				DQS2T		DQS2T	
B3	VREFB3N3	IO			D30				DQ2T1		DQ2T1	
B3	VREFB3N3	IO			M28				DQ2T0		DQ2T0	
B3	VREFB3N4	IO	DQS17T		A36	DQVLD8T			DM1T			
B3	VREFB3N4	IO	DQ17T		A35	DQ8T	DQ3T	DQ1T	DQ1T3		DQ1T3	
B3	VREFB3N4	IO	DQ17T		B34	DQ8T	DQ3T	DQ1T	DQ1T2		DQ1T2	
B3	VREFB3N4	IO	DQ17T		B37	DQ8T	DQ3T		DQS1T		DQS1T	
B3	VREFB3N4	IO	DQSn17T		B36	DQ8T	DQ3T	DQ1T	DQ1T1		DQ1T1	
B3	VREFB3N4	IO	DQ17T		A37	DQ8T			DQ1T0		DQ1T0	
B3	VREFB3N4	IO			G29				DM0T			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
B3	VREFB3N4	IO			E34				DQ0T3		DQ0T3	
B3	VREFB3N4	VREFB3N4	VREFB3N4		E31							
B3	VREFB3N4	IO			D31				DQ0T2		DQ0T2	
B3	VREFB3N4	IO			F30				DQS0T		DQS0T	
B3	VREFB3N4	IO			H31				DQ0T1		DQ0T1	
B3	VREFB3N4	IO			J30				DQ0T0		DQ0T0	
B3	VREFB3N4	IO		DATA2	D32							
B3	VREFB3N4	IO		DATA3	D33							
B3	VREFB3N4	IO		DATA4	F31							
B3	VREFB3N4	IO		DATA5	H30							
B3	VREFB3N4	IO		DATA6	G30							
B3	VREFB3N4	IO		DATA7	F32							
B3	VREFB3N4	IO		RDYnBSY	G31							
B3	VREFB3N4	IO		INIT_DONE	E33							
B3	VREFB3N4	nSTATUS		nSTATUS	C34							
B3	VREFB3N4	nCE		nCE	D34							
B3	VREFB3N4	DCLK		DCLK	C35							
B3	VREFB3N4	CONF_DONE		CONF_DONE	D35							
		VCCIO2			P31							
		VCCIO2			R29							
		VCCIO2			U31							
		VCCIO2			V29							
		VCCIO2			W31							
		VCCIO1			AA30							
		VCCIO1			AC31							
		VCCIO1			AD29							
		VCCIO1			AF31							
		VCCIO1			AG29							
		VCCIO1			AJ31							
		VCCIO8			AK21							
		VCCIO8			AK23							
		VCCIO8			AK26							
		VCCIO8			AL23							
		VCCIO8			AL26							
		VCCIO7			AK14							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		VCCIO7			AK17							
		VCCIO7			AL14							
		VCCIO7			AL17							
		VCCIO7			AL19							
		VCCT_B16			AC11							
		VCCT_B16			AD11							
		VCCH_B16			AC12							
		VCCH_B16			AD12							
		VCCR			AC10							
		VCCR			AD10							
		VCCA			AC9							
		VCCT_B15			W11							
		VCCT_B15			Y11							
		VCCH_B15			W12							
		VCCH_B15			Y12							
		VCCR			W10							
		VCCR			Y10							
		VCCA			W9							
		VCCT_B17			AG11							
		VCCT_B17			AH11							
		VCCH_B17			AG12							
		VCCH_B17			AH12							
		VCCR			AG10							
		VCCR			AH10							
		VCCA			AG9							
		VCCT_B14			P11							
		VCCT_B14			R11							
		VCCH_B14			P12							
		VCCH_B14			R12							
		VCCR			P10							
		VCCR			R10							
		VCCA			P9							
		VCCT_B13			K11							
		VCCT_B13			L11							
		VCCH_B13			K12							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		VCCH_B13			L12							
		VCCR			K10							
		VCCR			L10							
		VCCA			K9							
		VCCP			AC13							
		VCCP			AD13							
		VCCP			W13							
		VCCP			Y13							
		VCCP			AG13							
		VCCP			AH13							
		VCCP			P13							
		VCCP			R13							
		VCCP			K13							
		VCCP			L13							
		VCCIO4			J14							
		VCCIO4			J17							
		VCCIO4			J19							
		VCCIO4			K14							
		VCCIO4			K17							
		VCCIO3			J23							
		VCCIO3			J26							
		VCCIO3			K21							
		VCCIO3			K23							
		VCCIO3			K26							
		VCCINT			AA15							
		VCCINT			AA17							
		VCCINT			AA23							
		VCCINT			AB14							
		VCCINT			AB16							
		VCCINT			AB18							
		VCCINT			AB20							
		VCCINT			AB22							
		VCCINT			AB24							
		VCCINT			AC15							
		VCCINT			AC17							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		VCCINT			AC19							
		VCCINT			AC21							
		VCCINT			AC23							
		VCCINT			AD14							
		VCCINT			AD15							
		VCCINT			AD16							
		VCCINT			AD17							
		VCCINT			AD18							
		VCCINT			AD19							
		VCCINT			AD20							
		VCCINT			AD21							
		VCCINT			AD22							
		VCCINT			AD23							
		VCCINT			AD24							
		VCCINT			T14							
		VCCINT			T15							
		VCCINT			T16							
		VCCINT			T17							
		VCCINT			T18							
		VCCINT			T19							
		VCCINT			T20							
		VCCINT			T21							
		VCCINT			T22							
		VCCINT			T23							
		VCCINT			U15							
		VCCINT			U17							
		VCCINT			U19							
		VCCINT			U21							
		VCCINT			U23							
		VCCINT			V14							
		VCCINT			V16							
		VCCINT			V18							
		VCCINT			V20							
		VCCINT			V22							
		VCCINT			V24							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		VCCINT			W15							
		VCCINT			W17							
		VCCINT			W23							
		VCCINT			Y14							
		VCCINT			Y16							
		VCCINT			Y18							
		VCCINT			Y22							
		VCCINT			Y24							
		GND			AC29							
		GND			AC32							
		GND			AC35							
		GND			AC38							
		GND			AF32							
		GND			AF35							
		GND			AF38							
		GND			AJ32							
		GND			AJ35							
		GND			AJ38							
		GND			AM35							
		GND			AM38							
		GND			AR38							
		GND			AV39							
		GND			B38							
		GND			B39							
		GND			E38							
		GND			H35							
		GND			H38							
		GND			L32							
		GND			L35							
		GND			L38							
		GND			P32							
		GND			P35							
		GND			P38							
		GND			U29							
		GND			U32							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			U35							
		GND			U38							
		GND			Y32							
		GND			Y35							
		GND			Y38							
		GND			AJ26							
		GND			AJ29							
		GND			AM11							
		GND			AM14							
		GND			AM17							
		GND			AM20							
		GND			AM23							
		GND			AM26							
		GND			AM29							
		GND			AM32							
		GND			AR11							
		GND			AR14							
		GND			AR17							
		GND			AR20							
		GND			AR23							
		GND			AR26							
		GND			AR29							
		GND			AR32							
		GND			AR35							
		GND			AV11							
		GND			AV14							
		GND			AV17							
		GND			AV20							
		GND			AV23							
		GND			AV26							
		GND			AV29							
		GND			AV32							
		GND			AV35							
		GND			AV38							
		GND			AV9							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			AW38							
		GND			A2							
		GND			A5							
		GND			A8							
		GND			AA3							
		GND			AA6							
		GND			AA7							
		GND			AA8							
		GND			AA10							
		GND			AA11							
		GND			AA12							
		GND			AA13							
		GND			AB1							
		GND			AB2							
		GND			AB3							
		GND			AB4							
		GND			AB5							
		GND			AB6							
		GND			AB9							
		GND			AC3							
		GND			AC6							
		GND			AC7							
		GND			AC8							
		GND			AD1							
		GND			AD2							
		GND			AD3							
		GND			AD4							
		GND			AD5							
		GND			AD6							
		GND			AD8							
		GND			AE3							
		GND			AE6							
		GND			AE7							
		GND			AE8							
		GND			AE10							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			AE11							
		GND			AE12							
		GND			AE13							
		GND			AF1							
		GND			AF2							
		GND			AF3							
		GND			AF4							
		GND			AF5							
		GND			AF6							
		GND			AF9							
		GND			AG3							
		GND			AG6							
		GND			AG7							
		GND			AG8							
		GND			AH1							
		GND			AH2							
		GND			AH3							
		GND			AH4							
		GND			AH5							
		GND			AH6							
		GND			AJ3							
		GND			AJ6							
		GND			AJ7							
		GND			AJ8							
		GND			AJ10							
		GND			AJ11							
		GND			AJ12							
		GND			AJ13							
		GND			AK1							
		GND			AK2							
		GND			AK3							
		GND			AK4							
		GND			AK5							
		GND			AK6							
		GND			AK8							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			AK9							
		GND			AL3							
		GND			AL6							
		GND			AL7							
		GND			AL8							
		GND			AL9							
		GND			AM1							
		GND			AM2							
		GND			AM3							
		GND			AM4							
		GND			AM5							
		GND			AM6							
		GND			AM9							
		GND			AN3							
		GND			AN6							
		GND			AN7							
		GND			AN8							
		GND			AN9							
		GND			AP1							
		GND			AP2							
		GND			AP3							
		GND			AP4							
		GND			AP5							
		GND			AP6							
		GND			AP9							
		GND			AR3							
		GND			AR6							
		GND			AR7							
		GND			AR8							
		GND			AR9							
		GND			AT1							
		GND			AT2							
		GND			AT3							
		GND			AT4							
		GND			AT5							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			AT6							
		GND			AT7							
		GND			AT8							
		GND			AU3							
		GND			AU6							
		GND			AU7							
		GND			AU8							
		GND			AV1							
		GND			AV2							
		GND			AV3							
		GND			AV4							
		GND			AV5							
		GND			AV6							
		GND			AV7							
		GND			AV8							
		GND			AW2							
		GND			AW5							
		GND			AW8							
		GND			B1							
		GND			B2							
		GND			B3							
		GND			B4							
		GND			B5							
		GND			B6							
		GND			B7							
		GND			B8							
		GND			C3							
		GND			C6							
		GND			C7							
		GND			C8							
		GND			D1							
		GND			D2							
		GND			D3							
		GND			D4							
		GND			D5							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			D6							
		GND			D7							
		GND			D8							
		GND			E3							
		GND			E6							
		GND			E7							
		GND			E8							
		GND			E9							
		GND			F1							
		GND			F2							
		GND			F3							
		GND			F4							
		GND			F5							
		GND			F6							
		GND			F9							
		GND			G3							
		GND			G6							
		GND			G7							
		GND			G8							
		GND			G9							
		GND			H1							
		GND			H2							
		GND			H3							
		GND			H4							
		GND			H5							
		GND			H6							
		GND			H9							
		GND			J3							
		GND			J6							
		GND			J7							
		GND			J8							
		GND			J9							
		GND			K1							
		GND			K2							
		GND			K3							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			K4							
		GND			K5							
		GND			K6							
		GND			K8							
		GND			L3							
		GND			L6							
		GND			L7							
		GND			L8							
		GND			M1							
		GND			M2							
		GND			M3							
		GND			M4							
		GND			M5							
		GND			M6							
		GND			M10							
		GND			M11							
		GND			M12							
		GND			M13							
		GND			N3							
		GND			N6							
		GND			N7							
		GND			N8							
		GND			N9							
		GND			P1							
		GND			P2							
		GND			P3							
		GND			P4							
		GND			P5							
		GND			P6							
		GND			R3							
		GND			R6							
		GND			R7							
		GND			R8							
		GND			T1							
		GND			T2							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			T3							
		GND			T4							
		GND			T5							
		GND			T6							
		GND			T8							
		GND			T10							
		GND			T11							
		GND			T12							
		GND			T13							
		GND			U3							
		GND			U6							
		GND			U7							
		GND			U8							
		GND			U9							
		GND			V1							
		GND			V2							
		GND			V3							
		GND			V4							
		GND			V5							
		GND			V6							
		GND			V9							
		GND			W3							
		GND			W6							
		GND			W7							
		GND			W8							
		GND			Y1							
		GND			Y2							
		GND			Y3							
		GND			Y4							
		GND			Y5							
		GND			Y6							
		GND			Y8							
		GND			A38							
		GND			B11							
		GND			B14							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			B17							
		GND			B20							
		GND			B23							
		GND			B26							
		GND			B29							
		GND			B32							
		GND			B35							
		GND			B9							
		GND			E11							
		GND			E14							
		GND			E17							
		GND			E20							
		GND			E23							
		GND			E26							
		GND			E29							
		GND			E32							
		GND			E35							
		GND			H11							
		GND			H14							
		GND			H17							
		GND			H20							
		GND			H23							
		GND			H26							
		GND			H29							
		GND			H32							
		GND			L23							
		GND			L26							
		GND			L29							
		GND			AA14							
		GND			AA16							
		GND			AA18							
		GND			AA22							
		GND			AA24							
		GND			AB13							
		GND			AB15							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			AB17							
		GND			AB19							
		GND			AB21							
		GND			AB23							
		GND			AC14							
		GND			AC16							
		GND			AC18							
		GND			AC20							
		GND			AC22							
		GND			AC24							
		GND			AC26							
		GND			AF13							
		GND			AF14							
		GND			AF17							
		GND			AF20							
		GND			AF23							
		GND			AF26							
		GND			AF29							
		GND			AJ14							
		GND			AJ17							
		GND			AJ20							
		GND			AJ23							
		GND			L14							
		GND			L17							
		GND			L20							
		GND			P14							
		GND			P17							
		GND			P20							
		GND			P23							
		GND			P26							
		GND			P29							
		GND			U13							
		GND			U14							
		GND			U16							
		GND			U18							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		GND			U20							
		GND			U22							
		GND			U24							
		GND			U26							
		GND			V13							
		GND			V15							
		GND			V17							
		GND			V19							
		GND			V21							
		GND			V23							
		GND			W14							
		GND			W16							
		GND			W18							
		GND			W22							
		GND			W24							
		GND			Y15							
		GND			Y17							
		GND			Y23							
		GND			Y26							
		GND			Y29							
		VCCPD2			R28							
		VCCPD2			T28							
		VCCPD2			U28							
		VCCPD1			AB28							
		VCCPD1			AC28							
		VCCPD1			AD28							
		VCCPD8			AH21							
		VCCPD8			AH22							
		VCCPD8			AH23							
		VCCPD7			AH17							
		VCCPD7			AH18							
		VCCPD7			AH19							
		VCCPD4			M17							
		VCCPD4			M18							
		VCCPD4			M19							

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	F1508	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode	x5 Mode (Note 1)		x4 Mode (Note 2)	
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508	DQ group for non-DQS mode (non-migratable) F1508	DQ group for non-DQS mode (migratable) F1508
		VCCPD3			M21							
		VCCPD3			M22							
		VCCPD3			M23							

Notes:

(1) This mode is used for x4 DDR2 SDRAM (with DM support) devices and x9 RLDRAM II devices.

(2) This mode is used for DDR/DDR2 SDRAM, RLDRAM II, and QDRII SRAM interfaces, except for x9 RLDRAM II devices. This mode can support x4 DDR2 SDRAM devices if the DM pins are not used.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	1.2-V internal logic array voltage supply pins. VCCINT also supplies power to the column dedicated clock input pins for the LVDS, LVPECL, HSTL, SSTL, differential HSTL, and differential SSTL I/O standards.
VCCIO[1..4,7,8]	Power	I/O supply voltage pins for banks 1-4, 7, and 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for row differential standards as well as all single-ended I/O standards with the exception of HSTL and SSTL on column dedicated clock input pins which are powered by VCCINT.
VCCPD[1..4,7,8]	Power	Dedicated power pins. This 3.3-V supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The VCCPD pins must be connected to 3.3 V and must ramp up from 0 V to 3.3 V within 100 ms to ensure successful configuration. If you use the AES key programming feature of the device, VCCPD8 powers the circuitry, enabling the key to be programmed in non-volatile memory. During key programming, apply 3.7 V to VCCPD8. For further information, refer to AN341: Using the Design Security Feature in Stratix II and Stratix II GX Devices.
GND	Ground	Device ground pins.
VREFB[1..4,7,8]N[4..0] (Note 8)	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for that bank. All the VREF pins within a bank are shorted together. If VREF pins are not used, you should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p, and PLL5_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL5 in bank 9 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p, and PLL6_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL6 in bank 10 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL11_OUT (Note 6)	Power	External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p, and PLL11_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL11 in bank 11 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL12_OUT (Note 6)	Power	External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p, and PLL12_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL12 in bank 12 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCCA_PLL[1,2,5..8,11,12] (Note 4)	Power	1.2-V analog power for PLL[1,2,5..8,11,12].
VCCD_PLL[1,2,5..8,11,12] (Note 4)	Power	1.2-V digital power for PLL[1,2,5..8,11,12].
GNDA_PLL[1,2,5..8,11,12] (Note 4)	Ground	Analog ground for PLL[1,2,5..8,11,12].
NC	No Connect	Do not drive any signals into this pin.
RUP4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
RDN4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
RUP7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rup must be connected to the designated RUP pin within bank 7. If not required, this pin is a regular I/O pin.
RDN7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rdn must be connected to the designated RDN pin within bank 7. If not required, this pin is a regular I/O pin.
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns it on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device or microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the Stratix II GX device. If the temperature-sensing diode is not used, then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the Stratix II GX device. If the temperature-sensing diode is not used, then connect this pin to GND.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Stratix II GX device. In AS mode, DCLK is an output from the Stratix II GX device that provides timing for the configuration interface.
MSEL[3..0]	Input	Configuration input pins that set the Stratix II GX device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic-high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
PORSEL	Input	Dedicated input that selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms.
Optional/Dual-Purpose Configuration Pins		
nCSO	I/O, Output	Output control signal from the Stratix II GX FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	I/O, Output	Control signal from the Stratix II GX FPGA to the serial configuration device in AS mode used to read out configuration data.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[6..1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[7..0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
DATA7	I/O, Bidirectional	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal has been strobed low.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
nCS, CS	I/O, Input	These are chip-select inputs that enable the Stratix II GX device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active-high enable, use the CS pin and drive the nCS pin low. If a design requires an active-low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
RUnLU	I/O, Input	Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration modes, this pin is available as general-purpose user I/O pin.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Clock and PLL Pins		
CLK[1,3]p	Clock, Input	Dedicated clock input pins 1 and 3 that can also be used for data inputs.
CLK[1,3]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs.
CLK[2,0]p/DIFFIO_RX_C[1,0]p (Note 5)	I/O, Clock	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[2,0]n/DIFFIO_RX_C[1,0]n (Note 5)	I/O, Clock	These pins can be used as I/O pins, the negative clock input pins for differential clock input, or the negative data pins of differential receiver channels.
CLK[4-7,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-7,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs.
FPLL[8..7]CLKp (Note 6)	Clock, Input	Dedicated positive clock inputs for fast PLLs (PLLs 7 and 8), which can also be used for data inputs.
FPLL[8..7]CLKn (Note 6)	Clock, Input	Dedicated negative clock inputs associated with the FPLL[7,8]CLKp pins, which can also be used for data inputs.
PLL5_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL5. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL5).
PLL5_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL5. If the clock outputs are single-ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL6_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL6. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL6).
PLL6_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL6. If the clock outputs are single-ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL11_OUT[1,0]p (Note 6)	Output	Optional positive external clock outputs [1,0] from enhanced PLL11. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL11).
PLL11_OUT[1,0]n (Note 6)	Output	Optional negative external clock outputs [1,0] from enhanced PLL11. If the clock outputs are single-ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL12_OUT[1,0]p (Note 6)	Output	Optional positive external clock outputs [1,0] from enhanced PLL12. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL12).
PLL12_OUT[1,0]n (Note 6)	Output	Optional negative external clock outputs [1,0] from enhanced PLL12. If the clock outputs are single-ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
PLL[6..5]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or external clock outputs for PLL[6,5].
PLL[6..5]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[6,5]_FBp, or negative terminal clock output pins for differential clock output.
PLL[12..11]_FBp/OUT2p (Note 6)	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or positive external clock outputs for PLL[12..11].
PLL[12..11]_FBn/OUT2n (Note 6)	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[12..11]_FBp, or negative external clock output pins for differential clock output.
Dual-Purpose Differential & External Memory Interface Pins		
DIFFIO_RX[76..1]p (Note 5)	I/O, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_RX[76..1]n (Note 5)	I/O, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[77..0]p (Note 5)	I/O, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[77..0]n (Note 5)	I/O, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[17..0][T,B] (Note 7)	DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[17..0][T,B]	DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase-shift circuitry.
DQ[17..0][T,B][3..0] (Note 7)	DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DQVLD[8..0][T,B]	DQVLD	Optional data valid signal for use in external memory interfacing.
Transceiver (I/O Banks) Pins		
VCCP	Power	GX bank [17..13] PCS power. This power is connected to 1.2 V.
VCCR	Power	GX bank [17..13] receiver analog power. This power is connected to 1.2 V.
VCCT_B[17..13] (Note 3)	Power	GX bank [17..13] transmitter analog power. This power is connected to 1.2 V.
VCCA	Power	GX bank [17..13] analog power. This power is connected to 3.3 V.
VCCH_B[17..13] (Note 3)	Power	GX bank [17..13] transmitter driver analog power. This power is connected to 1.2 V or 1.5 V.
VCCL_B[17..13] (Note 3)	Power	GX bank [17..13] VCO analog power. This power is connected to 1.2 V.
GXB_RX[19..0]p (Note 2)	I, Input	High-speed positive differential receiver channels.
GXB_RX[19..0]n (Note 2)	I, Input	High-speed negative differential receiver channels.
GXB_TX[19..0]p (Note 2)	O, Output	High-speed positive differential transmitter channel.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
GXB_TX[19..0]n (Note 2)	O, Output	High-speed negative differential transmitter channels.
REFCLK[0,1]_B[17..13]p (Note 3)	I, Input	High-speed differential I/O reference clock positive. This pin is powered by 1.2-V VCCT_B[17..13].
REFCLK[0,1]_B[17..13]n (Note 3)	I, Input	High-speed differential I/O reference clock negative. This pin is powered by 1.2-V VCCT_B[17..13].
RREFB[17..13] (Note 3)	I, Input	Reference resistor for GX side banks.

Notes:

1) These descriptions are created based on the Stratix II GX130 device (EP2SGX130GF1508).

2) Transceiver signals GXB_RX[19..0] and GXB_TX[19..0] are device-specific.
EP2SGX30C and EP2SGX60C each contains 4 transceivers: GXB_RX[3..0] and GXB_TX[3..0].
EP2SGX30D and EP2SGX60D each contains 8 transceivers: GXB_RX[7..0] and GXB_TX[7..0].
EP2SGX60E and EP2SGX90E each contains 12 transceivers: GXB_RX[11..0] and GXB_TX[11..0].
EP2SGX90F contains 16 transceivers: GXB_RX[15..0] and GXB_TX[15..0].
EP2SGX130G contains 20 transceivers: GXB_RX[19..0] and GXB_TX[19..0].

3) Pins VCCT_B[17..13], VCCH_B[17..13], REFCLK[0,1]_B[17..13], RREFB[17..13], and VCCL[17..13] refer to the bank number of the transceiver.
EP2SGX30C and EP2SGX60C each consists of 4 transceivers in Bank 13.
EP2SGX30D and EP2SGX60D each consists of 8 transceivers in Banks 13 to 14.
EP2SGX60E and EP2SGX90E each consists of 12 transceivers in Banks 13 to 15.
EP2SGX90F consists of 16 transceivers in Banks 13 to 16.
EP2SGX130G consists of 20 transceivers in Banks 13 to 17.

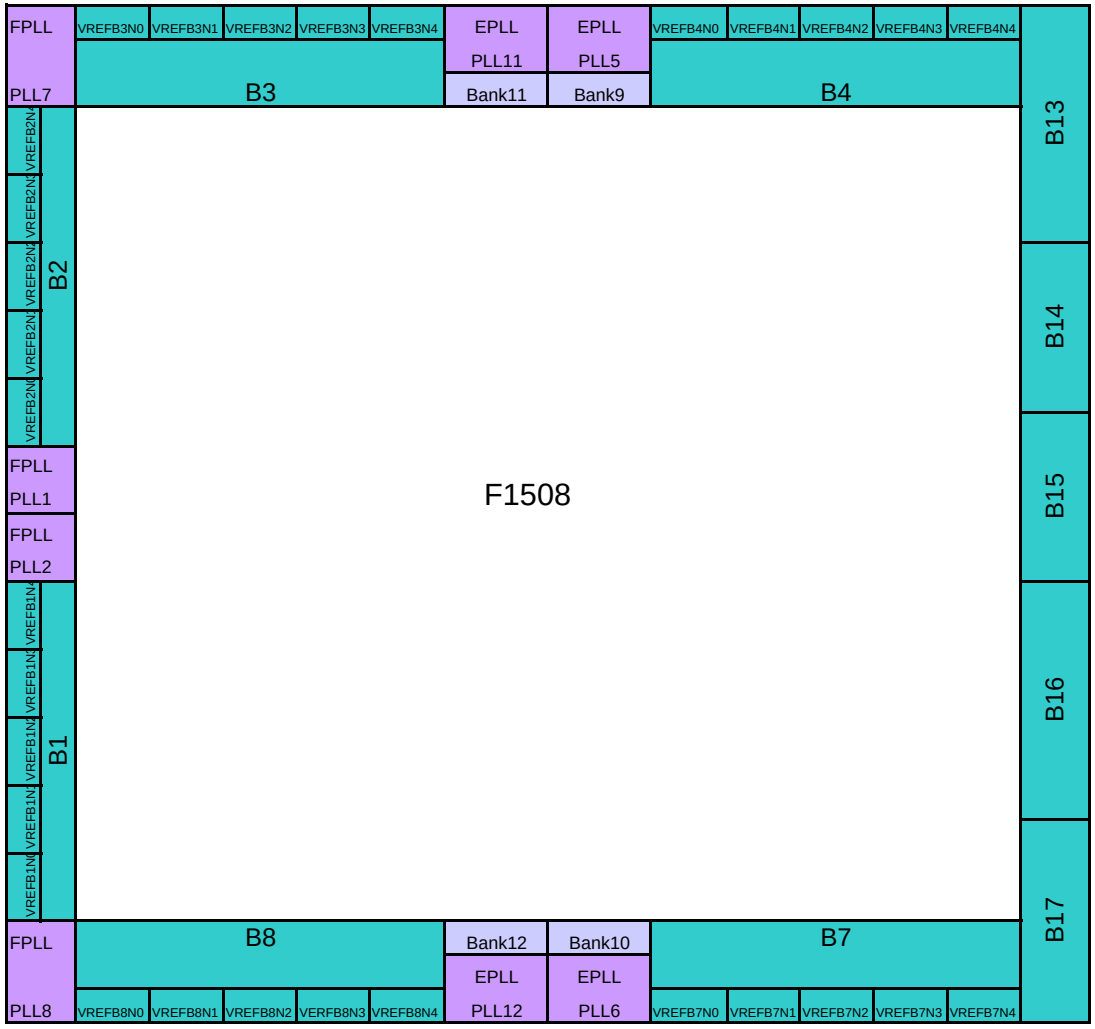
4) EP2SGX30 and EP2SGX 60C/D only have PLL(1, 2, 5 & 6). EP2SGX60E, EP2SGX90, and EP2SGX130 have PLL(1,2, 5, 6, 7, 8, 11 & 12).

5) The differential TX/RX count for each device and package is different.
EP2SGX30, EP2SGX60C, and EP2SGX60D each consists of 29 transmit and 29 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX60E consists of 42 transmit and 40 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX90E consists of 45 transmit and 45 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX90F consists of 59 transmit and 57 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
EP2SGX130G consists of 71 transmit and 71 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]). The transmit bus numbers 15-17 and 64-68 are unused. Also, the receive bus numbers 15-17, 64, and 65 are not unused.

6) EP2SGX30 does not have the following signals: FPLL[8..7]CLK, PLL11_OUT[1,0], PLL12_OUT[1,0], PLL[12..11]_FBp/OUT2, VCC_PLL11_OUT, and VCC_PLL12_OUT.
EP2SGX60C/D does not have the following signals: FPLL[8..7]CLK, PLL11_OUT[1]p/n, PLL11_OUT[0]p, PLL12_OUT[1]p/n, PLL12_OUT[0]n, PLL[11]_FBp/OUT2p/n, PLL[12]_FBp/OUT2p, VCC_PLL11_OUT, and VCC_PLL12_OUT.

7) EP2SGX30C, EP2SGX30D, EP2SGX60C, and EP2SGX60D support either (18, x4) (8, x8/x9) or (4, x16/x18) DQ and DQS bus modes.
EP2SGX60E, EP2SGX90D, EP2SGX90F, and EP2SGX130G support either (36, x4) (18, x8/x9) or (8, x16/x18) DQ and DQS bus modes.

8) The number of VREF pins varies according to the device.
EP2SGX30 has 2 VREF pins per bank, VREFB[1..4,7,8]N[1..0].
EP2SGX60 and EP2SGX90 have 3 VREF pins per bank, VREFB[1..4,7,8]N[2..0].
EP2SGX130 has 5 VREF pins per bank, VREFB[1..4,7,8]N[4..0].



Notes:

1. This is a top view of the silicon die. For flip-chip packages, the die is mounted upside-down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version History	Date	Changes Made
1.0	5/4/2006	Initial release.
1.1	8/10/2006	Updated VCCL pins to VCCL_B[17..13] in Pin List and Pin Definitions.
		Updated pin definitions for VCCPD[1..4,7,8].
		Removed Bank 7 reference for GND pin AM12 (F1508) in Pin List.
		Updated Bank & PLL Diagram with the correct number of VREFs per bank.
		Added Note 8 for VREF pin in Pin Definitions.
		Added VCCL to Note 3 in Pin Definitions.
1.2	1/15/2007	Updated pin definition for REFCLK to mention that it is powered by 1.2-V VCCT.
		Updated pin definition for VREF pins.
		Updated Note 4 in Pin Definitions.
1.3	12/28/2007	Updated pin descriptions for VCCIO, VCCINT, VCCPD, TEMPDIODEp, and TEMPDIODEn.