Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCA_PLL7			L23	D31	J31			
		GND								
		GNDA_PLL7			M23	D32	K31			
		VCCG_PLL7			J23	D30	L30			
		GNDG_PLL7			K23	E30	L31			
B2	VREF0B2	FPLL7CLKp			E31	L29	J38			
B2	VREF0B2	FPLL7CLKn			D31	L28	J39			
B2	VREF0B2	IO					N30			
B2	VREF0B2	IO					N31			
B2	VREF0B2	IO	DIFFIO_RX57p				F36			LOW
B2	VREF0B2	IO	DIFFIO_RX57n				F37			LOW
B2	VREF0B2	IO	DIFFIO_TX57p		K24	G25	M30			HIGH
B2	VREF0B2	IO	DIFFIO_TX57n		J24	G26	M31			HIGH
B2	VREF0B2	IO	DIFFIO_RX56p				D39			LOW
B2	VREF0B2	IO	DIFFIO_RX56n				D38			LOW
B2	VREF0B2	IO	DIFFIO_TX56p		K25	G28	J32			HIGH
B2	VREF0B2	IO	DIFFIO_TX56n		J25	G27	J33			HIGH
B2	VREF0B2	IO	DIFFIO_RX55p				G36			LOW
B2	VREF0B2	IO	DIFFIO_RX55n				G37			LOW
B2	VREF0B2	IO	DIFFIO_TX55p		H24	H28	K32			HIGH
B2	VREF0B2	IO	DIFFIO_TX55n		G24	H27	K33			HIGH
B2	VREF0B2	IO	DIFFIO_RX54p				E38			LOW
B2	VREF0B2	IO	DIFFIO_RX54n				E39			LOW
B2	VREF0B2	IO	DIFFIO_TX54p		H25	J27	L33			HIGH
B2	VREF0B2	IO	DIFFIO_TX54n		G25	J28	L32			HIGH
B2	VREF0B2	VREF0B2			L22	F27	M29			
B2	VREF0B2	IO	DIFFIO_RX53p				F38			LOW
B2	VREF0B2	IO	DIFFIO_RX53n				F39			LOW
B2	VREF0B2	IO	DIFFIO_TX53p		K26	H25	M32			HIGH
B2	VREF0B2	IO	DIFFIO_TX53n		L26	H26	M33			HIGH
B2	VREF0B2	IO	DIFFIO_RX52p				H37			LOW
B2	VREF0B2	IO	DIFFIO_RX52n				H36			LOW
B2	VREF0B2	IO	DIFFIO_TX52p		J26	J25	N32			HIGH
B2	VREF0B2	IO	DIFFIO_TX52n		H26	J26	N33			HIGH
B2	VREF0B2	IO	DIFFIO_RX51p			E29	G39			LOW
B2	VREF0B2	IO	DIFFIO_RX51n			F28	G38			LOW
B2	VREF0B2	IO	DIFFIO_TX51p		G26	K28	K34			HIGH
B2	VREF0B2	IO	DIFFIO_TX51n		F26	K27	K35			HIGH
B2	VREF0B2	IO	DIFFIO_RX50p			E32	H39			LOW
B2	VREF0B2	IO	DIFFIO_RX50n			E31	H38			LOW
B2	VREF0B2	IO	DIFFIO_TX50p		F27	K26	L35			HIGH
B2	VREF0B2	IO	DIFFIO_TX50n		G27	K25	L34			HIGH
B2	VREF0B2	IO	DIFFIO_RX49p		F28	F29	K36			HIGH
B2	VREF0B2	IO	DIFFIO_RX49n		G28	F30	K37			HIGH
B2	VREF0B2	IO	DIFFIO_TX49p		H27	L27	M34			HIGH
B2	VREF0B2	IO	DIFFIO_TX49n		J27	L26	M35			HIGH
B2	VREF1B2	IO	DIFFIO_RX48p		J28	F31	J36			HIGH
B2	VREF1B2	IO	DIFFIO_RX48n		H28	F32	J37			HIGH
B2	VREF1B2	IO	DIFFIO_TX48p		K27	M26	N34			HIGH
B2	VREF1B2	IO	DIFFIO_TX48n		L27	M27	N35			HIGH
B2	VREF1B2	IO	DIFFIO_RX47p		D29	G29	L37			HIGH
B2	VREF1B2	IO	DIFFIO_RX47n		E29	G30	L36			HIGH
B2	VREF1B2	IO	DIFFIO_TX47p		L24	M24	P32			HIGH
B2	VREF1B2	IO	DIFFIO_TX47n		M24	M25	P33			HIGH
B2	VREF1B2	IO	DIFFIO_RX46p		F29	H30	K38			HIGH
B2	VREF1B2	IO	DIFFIO_RX46n		G29	H29	K39			HIGH
B2	VREF1B2	IO	DIFFIO_TX46p		L25	N24	P34			HIGH
B2	VREF1B2	IO	DIFFIO_TX46n		M25	N23	P35			HIGH
B2	VREF1B2	IO	DIFFIO_RX45p		H29	G31	M36			HIGH
B2	VREF1B2	IO	DIFFIO_RX45n		J29	G32	M37			HIGH
B2	VREF1B2	IO	DIFFIO_TX45p		P24	N27	R33			HIGH
B2	VREF1B2	IO	DIFFIO_TX45n		N24	N28	R32			HIGH
B2	VREF1B2	IO	DIFFIO_RX44p		D30	H31	L38			HIGH
B2	VREF1B2	IO	DIFFIO_RX44n		E30	H32	L39			HIGH
B2	VREF1B2	IO	DIFFIO_TX44p		N25	P23	R34			HIGH
B2	VREF1B2	IO	DIFFIO_TX44n		P25	P24	R35			HIGH
B2	VREF1B2	VREF1B2			M22	L25	N29			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF1B2	IO	DIFFIO_RX43p		F30	J29	M38			HIGH
B2	VREF1B2	IO	DIFFIO_RX43n		G30	J30	M39			HIGH
B2	VREF1B2	IO	DIFFIO_TX43p		M26	N25	T33			HIGH
B2	VREF1B2	IO	DIFFIO_TX43n		N26	N26	T32			HIGH
B2	VREF1B2	IO	DIFFIO_RX42p		H30	K30	N36			HIGH
B2	VREF1B2	IO	DIFFIO_RX42n		J30	K29	N37			HIGH
B2	VREF1B2	IO	DIFFIO_TX42p		M27	P28	T30			HIGH
B2	VREF1B2	IO	DIFFIO_TX42n		N27	P27	T31			HIGH
B2	VREF1B2	IO	DIFFIO_RX41p		F31	J32	N38			HIGH
B2	VREF1B2	IO	DIFFIO_RX41n		G31	J31	P38			HIGH
B2	VREF1B2	IO	DIFFIO_TX41p		P27	R28	T34			HIGH
B2	VREF1B2	IO	DIFFIO_TX41n		R27	R27	T35			HIGH
B2	VREF1B2	IO	DIFFIO_RX40p		H31	K31	P39			HIGH
B2	VREF1B2	IO	DIFFIO_RX40n		J31	L32	R38			HIGH
B2	VREF1B2	IO	DIFFIO_TX40p		R26	P25	U35			HIGH
B2	VREF1B2	IO	DIFFIO_TX40n		P26	P26	U34			HIGH
B2	VREF1B2	IO	DIFFIO_RX39p/RUP2		K28	M28	P36			HIGH
B2	VREF1B2	IO	DIFFIO_RX39n/RDN2		K29	M29	P37			HIGH
B2	VREF1B2	IO	DIFFIO_TX39p		N23	R23	U33			HIGH
B2	VREF1B2	IO	DIFFIO_TX39n		P23	R24	U32			HIGH
B2	VREF2B2	IO	DIFFIO_RX38p		M28	L30	R36			HIGH
B2	VREF2B2	IO	DIFFIO_RX38n		L28	L31	R37			HIGH
B2	VREF2B2	IO	DIFFIO_TX38p		T25	R25	V35			HIGH
B2	VREF2B2	IO	DIFFIO_TX38n		R25	R26	V34			HIGH
B2	VREF2B2	IO	DIFFIO_RX37p		M29	M31	T36			HIGH
B2	VREF2B2	IO	DIFFIO_RX37n		L29	M30	T37			HIGH
B2	VREF2B2	IO	DIFFIO_TX37p			M23	U31			LOW
B2	VREF2B2	IO	DIFFIO_TX37n			M22	U30			LOW
B2	VREF2B2	IO	DIFFIO_RX36p		P28	N29	T39			HIGH
B2	VREF2B2	IO	DIFFIO_RX36n		N28	N30	T38			HIGH
B2	VREF2B2	IO	DIFFIO_TX36p			N22	U29			LOW
B2	VREF2B2	IO	DIFFIO_TX36n			P22	U28			LOW
B2	VREF2B2	IO	DIFFIO_RX35p		N29	N31	U36			HIGH
B2	VREF2B2	IO	DIFFIO_RX35n		P29	N32	U37			HIGH
B2	VREF2B2	IO	DIFFIO_TX35p				V32			LOW
B2	VREF2B2	IO	DIFFIO_TX35n				V31			LOW
B2	VREF2B2	IO	DIFFIO_RX34p		L30	P29	U38			HIGH
B2	VREF2B2	IO	DIFFIO_RX34n		K30	P30	U39			HIGH
B2	VREF2B2	IO	DIFFIO_TX34p				V29			LOW
B2	VREF2B2	IO	DIFFIO_TX34n				V30			LOW
B2	VREF2B2	VREF2B2			N22	R21	P29			
B2	VREF2B2	IO	DIFFIO_RX33p		N30	P31	V36			HIGH
B2	VREF2B2	IO	DIFFIO_RX33n		M30	P32	V37			HIGH
B2	VREF2B2	IO	DIFFIO_TX33p				V33			LOW
B2	VREF2B2	IO	DIFFIO_TX33n				W34			LOW
B2	VREF2B2	IO	DIFFIO_RX32p		L31	R32	V38			HIGH
B2	VREF2B2	IO	DIFFIO_RX32n		K31	R31	V39			HIGH
B2	VREF2B2	IO	DIFFIO_TX32p				W31			LOW
B2	VREF2B2	IO	DIFFIO_TX32n				W32			LOW
B2	VREF2B2	IO	DIFFIO_RX31p		R30	R30	W39			HIGH
B2	VREF2B2	IO	DIFFIO_RX31n		P30	R29	W38			HIGH
B2	VREF2B2	IO	DIFFIO_TX31p				W28			LOW
B2	VREF2B2	IO	DIFFIO_TX31n				W27			LOW
B2	VREF2B2	IO	DIFFIO_RX30p		P31	T32	W37			HIGH
B2	VREF2B2	IO	DIFFIO_RX30n		R31	T31	W36			HIGH
B2	VREF2B2	IO	DIFFIO_TX30p				W29			LOW
B2	VREF2B2	IO	DIFFIO_TX30n				W30			LOW
B2	VREF2B2	CLK0n			R28	T30	Y39			
B2	VREF2B2	CLK0p			R29	T29	Y38			
B2	VREF2B2	IO	CLK1n		T30	T28	Y34			
B2	VREF2B2	CLK1p			T31	T27	Y35			
		VCCA_PLL1			R24	T25	AA32			
		GND								
		GNDA_PLL1			T24	T26	Y31			
		VCCG_PLL1			R22	R22	Y28			
		GNDG_PLL1			R23	T22	Y29			
		VCCA_PLL2			U24	U25	AA30			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND								
		GNDA_PLL2			V24	U26	AA31			
		VCCG_PLL2			U23	U24	AA28			
		GNDG_PLL2			V23	T24	AA29			
B1	VREF0B1	CLK2p			T29	U31	Y37			
B1	VREF0B1	CLK2n			T28	U32	Y36			
B1	VREF0B1	CLK3p			U29	U29	AA35			
B1	VREF0B1	IO	CLK3n		U28	U30	AA34			
B1	VREF0B1	IO	DIFFIO_RX29p		U31	U28	AA39			HIGH
B1	VREF0B1	IO	DIFFIO_RX29n		V31	U27	AA38			HIGH
B1	VREF0B1	IO	DIFFIO_TX29p				AA27			LOW
B1	VREF0B1	IO	DIFFIO_TX29n				AA26			LOW
B1	VREF0B1	IO	DIFFIO_RX28p		AB31	V32	AA37			HIGH
B1	VREF0B1	IO	DIFFIO_RX28n		AA31	V31	AA36			HIGH
B1	VREF0B1	IO	DIFFIO_TX28p				AB27			LOW
B1	VREF0B1	IO	DIFFIO_TX28n				AB26			LOW
B1	VREF0B1	IO	DIFFIO_RX27p		V30	V30	AB38			HIGH
B1	VREF0B1	IO	DIFFIO_RX27n		U30	V29	AB39			HIGH
B1	VREF0B1	IO	DIFFIO_TX27p				Y33			LOW
B1	VREF0B1	IO	DIFFIO_TX27n				AA33			LOW
B1	VREF0B1	VREF0B1			V22	V21	AE29			
B1	VREF0B1	IO	DIFFIO_RX26p		W30	W32	AB37			HIGH
B1	VREF0B1	IO	DIFFIO_RX26n		Y30	W31	AB36			HIGH
B1	VREF0B1	IO	DIFFIO_TX26p				AB33			LOW
B1	VREF0B1	IO	DIFFIO_TX26n				AB32			LOW
B1	VREF0B1	IO	DIFFIO_RX25p		AA30	W30	AC39			HIGH
B1	VREF0B1	IO	DIFFIO_RX25n		AB30	W29	AC38			HIGH
B1	VREF0B1	IO	DIFFIO_TX25p				AB28			LOW
B1	VREF0B1	IO	DIFFIO_TX25n				AB29			LOW
B1	VREF0B1	IO	DIFFIO_RX24p		V29	Y32	AC37			HIGH
B1	VREF0B1	IO	DIFFIO_RX24n		W29	Y31	AC36			HIGH
B1	VREF0B1	IO	DIFFIO_TX24p				AB31			LOW
B1	VREF0B1	IO	DIFFIO_TX24n				AB30			LOW
B1	VREF0B1	IO	DIFFIO_RX23p		Y29	Y30	AD39			HIGH
B1	VREF0B1	IO	DIFFIO_RX23n		AA29	Y29	AD38			HIGH
B1	VREF0B1	IO	DIFFIO_TX23p			U22	AC26			LOW
B1	VREF0B1	IO	DIFFIO_TX23n			V22	AC27			LOW
B1	VREF1B1	IO	DIFFIO_RX22p		V28	AA31	AD37			HIGH
B1	VREF1B1	IO	DIFFIO_RX22n		W28	AA30	AD36			HIGH
B1	VREF1B1	IO	DIFFIO_TX22p			W21	AC31			LOW
B1	VREF1B1	IO	DIFFIO_TX22n			W22	AC30			LOW
B1	VREF1B1	IO	DIFFIO_RX21p		Y28	AB31	AE37			HIGH
B1	VREF1B1	IO	DIFFIO_RX21n		AA28	AB30	AE36			HIGH
B1	VREF1B1	IO	DIFFIO_TX21p			Y21	AC28			LOW
B1	VREF1B1	IO	DIFFIO_TX21n			Y22	AC29			LOW
B1	VREF1B1	IO	DIFFIO_RX20p/RUP1		AB29	AA28	AF37			HIGH
B1	VREF1B1	IO	DIFFIO_RX20n/RDN1		AB28	AA29	AF36			HIGH
B1	VREF1B1	IO	DIFFIO_TX20p			AA22	AD29			LOW
B1	VREF1B1	IO	DIFFIO_TX20n			AB23	AD28			LOW
B1	VREF1B1	IO	DIFFIO_RX19p		AC31	AB32	AE38			HIGH
B1	VREF1B1	IO	DIFFIO_RX19n		AD31	AC31	AF39			HIGH
B1	VREF1B1	IO	DIFFIO_TX19p		V25	V26	AB34			HIGH
B1	VREF1B1	IO	DIFFIO_TX19n		U25	V25	AB35			HIGH
B1	VREF1B1	VREF1B1			W22	AA23	AF29			
B1	VREF1B1	IO	DIFFIO_RX18p		AE31	AD32	AF38			HIGH
B1	VREF1B1	IO	DIFFIO_RX18n		AF31	AD31	AG38			HIGH
B1	VREF1B1	IO	DIFFIO_TX18p		U26	V28	AC32			HIGH
B1	VREF1B1	IO	DIFFIO_TX18n		T26	V27	AC33			HIGH
B1	VREF1B1	IO	DIFFIO_RX17p		AC30	AC29	AG37			HIGH
B1	VREF1B1	IO	DIFFIO_RX17n		AD30	AC30	AG36			HIGH
B1	VREF1B1	IO	DIFFIO_TX17p		T27	W25	AC34			HIGH
B1	VREF1B1	IO	DIFFIO_TX17n		U27	W26	AC35			HIGH
B1	VREF1B1	IO	DIFFIO_RX16p		AF30	AD30	AH39			HIGH
B1	VREF1B1	IO	DIFFIO_RX16n		AE30	AD29	AH38			HIGH
B1	VREF1B1	IO	DIFFIO_TX16p		V26	W27	AD34			HIGH
B1	VREF1B1	IO	DIFFIO_TX16n		W26	W28	AD35			HIGH
B1	VREF1B1	IO	DIFFIO_RX15p		AG30	AE32	AH37			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_RX15n		AH30	AE31	AH36			HIGH
B1	VREF1B1	IO	DIFFIO_TX15p		W24	V24	AD33			HIGH
B1	VREF1B1	IO	DIFFIO_TX15n		Y24	V23	AD32			HIGH
B1	VREF2B1	IO	DIFFIO_RX14p		AC29	AE30	AJ39			HIGH
B1	VREF2B1	IO	DIFFIO_RX14n		AD29	AE29	AJ38			HIGH
B1	VREF2B1	IO	DIFFIO_TX14p		W25	Y26	AD31			HIGH
B1	VREF2B1	IO	DIFFIO_TX14n		Y25	Y25	AD30			HIGH
B1	VREF2B1	IO	DIFFIO_RX13p		AE29	AF32	AJ37			HIGH
B1	VREF2B1	IO	DIFFIO_RX13n		AF29	AF31	AJ36			HIGH
B1	VREF2B1	IO	DIFFIO_TX13p		Y26	Y28	AE35			HIGH
B1	VREF2B1	IO	DIFFIO_TX13n		AA26	Y27	AE34			HIGH
B1	VREF2B1	IO	DIFFIO_RX12p		AH29	AF30	AK38			HIGH
B1	VREF2B1	IO	DIFFIO_RX12n		AG29	AF29	AK39			HIGH
B1	VREF2B1	IO	DIFFIO_TX12p		W23	W23	AE33			HIGH
B1	VREF2B1	IO	DIFFIO_TX12n		Y23	W24	AE32			HIGH
B1	VREF2B1	IO	DIFFIO_RX11p		AC28	AG31	AK37			HIGH
B1	VREF2B1	IO	DIFFIO_RX11n		AD28	AG32	AK36			HIGH
B1	VREF2B1	IO	DIFFIO_TX11p		V27	Y23	AF35			HIGH
B1	VREF2B1	IO	DIFFIO_TX11n		W27	Y24	AF34			HIGH
B1	VREF2B1	VREF2B1			Y22	AB25	AG29			
B1	VREF2B1	IO	DIFFIO_RX10p		AE28	AG30	AL37			HIGH
B1	VREF2B1	IO	DIFFIO_RX10n		AF28	AG29	AL36			HIGH
B1	VREF2B1	IO	DIFFIO_TX10p		Y27	AA25	AF33			HIGH
B1	VREF2B1	IO	DIFFIO_TX10n		AA27	AA24	AF32			HIGH
B1	VREF2B1	IO	DIFFIO_RX9p			AH32	AM39			LOW
B1	VREF2B1	IO	DIFFIO_RX9n			AH31	AM38			LOW
B1	VREF2B1	IO	DIFFIO_TX9p		AB27	AA27	AG35			HIGH
B1	VREF2B1	IO	DIFFIO_TX9n		AC27	AA26	AG34			HIGH
B1	VREF2B1	IO	DIFFIO_RX8p			AH29	AN39			LOW
B1	VREF2B1	IO	DIFFIO_RX8n			AG28	AN38			LOW
B1	VREF2B1	IO	DIFFIO_TX8p		AE27	AB27	AG33			HIGH
B1	VREF2B1	IO	DIFFIO_TX8n		AD27	AB26	AG32			HIGH
B1	VREF2B1	IO	DIFFIO_RX7p			AG25	AM37			LOW
B1	VREF2B1	IO	DIFFIO_RX7n			AG26	AM36			LOW
B1	VREF2B1	IO	DIFFIO_TX7p		AG27	AC25	AH34			HIGH
B1	VREF2B1	IO	DIFFIO_TX7n		AF27	AC26	AH35			HIGH
B1	VREF3B1	IO	DIFFIO_RX6p				AP38			LOW
B1	VREF3B1	IO	DIFFIO_RX6n				AP39			LOW
B1	VREF3B1	IO	DIFFIO_TX6p		AB26	AC27	AK35			HIGH
B1	VREF3B1	IO	DIFFIO_TX6n		AC26	AC28	AK34			HIGH
B1	VREF3B1	IO	DIFFIO_RX5p				AN37			LOW
B1	VREF3B1	IO	DIFFIO_RX5n				AN36			LOW
B1	VREF3B1	IO	DIFFIO_TX5p		AD26	AD28	AH33			HIGH
B1	VREF3B1	IO	DIFFIO_TX5n		AE26	AD27	AH32			HIGH
B1	VREF3B1	IO	DIFFIO_RX4p				AR38			LOW
B1	VREF3B1	IO	DIFFIO_RX4n				AR39			LOW
B1	VREF3B1	IO	DIFFIO_TX4p		AA25	AD26	AJ35			HIGH
B1	VREF3B1	IO	DIFFIO_TX4n		AB25	AD25	AJ34			HIGH
B1	VREF3B1	IO	DIFFIO_RX3p				AT39			LOW
B1	VREF3B1	IO	DIFFIO_RX3n				AT38			LOW
B1	VREF3B1	IO	DIFFIO_TX3p		AD25	AE28	AJ33			HIGH
B1	VREF3B1	IO	DIFFIO_TX3n		AC25	AE27	AJ32			HIGH
B1	VREF3B1	VREF3B1			AA22	AG27	AH29			
B1	VREF3B1	IO	DIFFIO_RX2p				AM35			LOW
B1	VREF3B1	IO	DIFFIO_RX2n				AM34			LOW
B1	VREF3B1	IO	DIFFIO_TX2p		AA24	AE25	AK32			HIGH
B1	VREF3B1	IO	DIFFIO_TX2n		AB24	AE26	AK33			HIGH
B1	VREF3B1	IO	DIFFIO_RX1p				AP36			LOW
B1	VREF3B1	IO	DIFFIO_RX1n				AP37			LOW
B1	VREF3B1	IO	DIFFIO_TX1p		AD24	AF27	AL33			HIGH
B1	VREF3B1	IO	DIFFIO_TX1n		AC24	AF28	AL32			HIGH
B1	VREF3B1	IO	DIFFIO_RX0p				AR37			LOW
B1	VREF3B1	IO	DIFFIO_RX0n				AR36			LOW
B1	VREF3B1	IO	DIFFIO_TX0p		AE25	AF26	AH31			HIGH
B1	VREF3B1	IO	DIFFIO_TX0n		AF25	AF25	AH30			HIGH
B1	VREF3B1	FPLL8CLKn			AG31	AB29	AL38			
B1	VREF3B1	FPLL8CLKp			AH31	AB28	AL39			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF3B1	IO					AG30			
B1	VREF3B1	IO					AG31			
		VCCA_PLL8			AB23	AJ31	AJ30			
		GND								
		GNDA_PLL8			AA23	AJ32	AJ31			
		VCCG_PLL8			AD23	AJ30	AL31			
		GNDG_PLL8			AC23	AH30	AK31			
B8	VREF0B8	IO			AG28	AB24	AR35			
B8	VREF0B8	IO					AU36			
B8	VREF0B8	IO					AT35			
B8	VREF0B8	IO					AN32			
B8	VREF0B8	IO					AV36			
B8	VREF0B8	IO					AT34			
B8	VREF0B8	IO			AJ30	AC24	AN33			
B8	VREF0B8	IO	DQ9B7		AK29	AH28	AV34	DQ3B15	DQ1B31	
B8	VREF0B8	IO					AP33			
B8	VREF0B8	IO	DQ9B6		AJ29	AK30	AU34	DQ3B14	DQ1B30	
B8	VREF0B8	IO			AE24	AG24	AL30			
B8	VREF0B8	IO	DQ9B5		AJ28	AJ28	AU33	DQ3B13	DQ1B29	
B8	VREF0B8	IO			AF26	AC23	AR34			
B8	VREF0B8	IO	DQ9B4		AL28	AJ29	AW33	DQ3B12	DQ1B28	
B8	VREF0B8	IO				AE24	AU35			
B8	VREF0B8	IO	DQ9B3		AH27	AK29	AW34	DQ3B11	DQ1B27	
B8	VREF0B8	IO				AG23	AW36			
B8	VREF0B8	IO	DQS9B		AK28	AK28	AV33			
B8	VREF0B8	VREF0B8			AB22	AH27	AJ29			
B8	VREF0B8	IO			AH28	AD24	AM31			
B8	VREF0B8	IO	DQ9B2		AL27	AL30	AV32	DQ3B10	DQ1B26	
B8	VREF0B8	IO				AF24	AK29			
B8	VREF0B8	IO	DQ9B1		AJ27	AL29	AU32	DQ3B9	DQ1B25	
B8	VREF0B8	IO					AN31			
B8	VREF0B8	IO	DQ9B0		AK27	AM29	AW32	DQ3B8	DQ1B24	
B8	VREF0B8	IO			AC22	AD23	AR33			
B8	VREF0B8	IO					AP32			
B8	VREF0B8	IO					AV35			
B8	VREF0B8	IO					AR32			
B8	VREF0B8	IO					AL29			
B8	VREF0B8	IO	DQ8B7		AH26	AH26	AU31	DQ3B7	DQ1B23	
B8	VREF0B8	IO					AT33			
B8	VREF0B8	IO	DQ8B6		AG26	AJ27	AV31	DQ3B6	DQ1B22	
B8	VREF0B8	IO			AD22	AE23	AK28			
B8	VREF0B8	IO	DQ8B5		AK26	AL28	AW31	DQ3B5	DQ1B21	
B8	VREF0B8	IO				AF23	AP31			
B8	VREF0B8	IO	DQ8B4		AL26	AK27	AW30	DQ3B4	DQ1B20	
B8	VREF1B8	IO				AB22	AW35			
B8	VREF1B8	IO	DQ8B3		AH25	AJ26	AU30	DQ3B3	DQ1B19	
B8	VREF1B8	IO			AC21	AC22	AM29			
B8	VREF1B8	IO	DQS8B		AJ26	AL27	AV30	DQS3B		
B8	VREF1B8	IO				AG22	AK27			
B8	VREF1B8	IO	DQ8B2		AK25	AM27	AU29	DQ3B2	DQ1B18	
B8	VREF1B8	IO					AN30			
B8	VREF1B8	IO	DQ8B1		AJ25	AM28	AV29	DQ3B1	DQ1B17	
B8	VREF1B8	IO			AA21	AD22	AT32			
B8	VREF1B8	IO	DQ8B0		AL25	AK26	AW29	DQ3B0	DQ1B16	
B8	VREF1B8	IO			AE22	AF22	AT31			
B8	VREF1B8	IO					AP29			
B8	VREF1B8	IO					AL28			
B8	VREF1B8	IO					AP30			
B8	VREF1B8	IO					AN29			
B8	VREF1B8	IO	DQ7B7		AG24	AH24	AR28	DQ2B15	DQ1B15	
B8	VREF1B8	IO					AL27			
B8	VREF1B8	IO	DQ7B6		AH23	AJ24	AT28	DQ2B14	DQ1B14	
B8	VREF1B8	VREF1B8			AB21	AH25	AJ28			
B8	VREF1B8	IO			AA19	AE22	AR31			
B8	VREF1B8	IO	DQ7B5		AK24	AJ25	AU28	DQ2B13	DQ1B13	
B8	VREF1B8	IO				AA21	AR30			
B8	VREF1B8	IO	DQ7B4		AH24	AK25	AV28	DQ2B12	DQ1B12	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF1B8	IO			AD21	AB21	AK26			
B8	VREF1B8	IO	DQ7B3		AJ23	AL25	AR27	DQ2B11	DQ1B11	
B8	VREF1B8	IO					AM28			
B8	VREF1B8	IO	DQS7B		AJ24	AL26	AT27		DQS1B	
B8	VREF1B8	IO				AC21	AN28			
B8	VREF1B8	IO	DQ7B2		AL24	AK24	AW28	DQ2B10	DQ1B10	
B8	VREF1B8	IO			AC20	AG21	AP28			
B8	VREF1B8	IO	DQ7B1		AK23	AM25	AU27	DQ2B9	DQ1B9	
B8	VREF1B8	IO					AT30			
B8	VREF1B8	IO	DQ7B0		AL23	AM26	AV27	DQ2B8	DQ1B8	
B8	VREF1B8	IO					AM27			
B8	VREF1B8	IO					AL26			
B8	VREF1B8	IO	FCLK3		AF23	AE21	AT29			
B8	VREF1B8	IO	FCLK2		AF22	AF21	AN26			
B8	VREF2B8	IO					AR29			
B8	VREF2B8	IO	DQ6B7		AG22	AJ23	AR26	DQ2B7	DQ1B7	
B8	VREF2B8	IO					AN27			
B8	VREF2B8	IO	DQ6B6		AH22	AL24	AT26	DQ2B6	DQ1B6	
B8	VREF2B8	IO					AK25			
B8	VREF2B8	IO	DQ6B5		AK22	AH22	AU26	DQ2B5	DQ1B5	
B8	VREF2B8	IO				AD21	AP27			
B8	VREF2B8	IO	DQ6B4		AG21	AM24	AV26	DQ2B4	DQ1B4	
B8	VREF2B8	IO		PGM2	AF24	AA20	AL25			
B8	VREF2B8	IO	DQ6B3		AH21	AK23	AW26	DQ2B3	DQ1B3	
B8	VREF2B8	IO			AD20	AG20	AP26			
B8	VREF2B8	IO	DQS6B		AJ22	AJ22	AU25	DQS2B		
B8	VREF2B8	IO				AB20	AM26			
B8	VREF2B8	IO	DQ6B2		AL22	AL23	AT25	DQ2B2	DQ1B2	
B8	VREF2B8	IO		CRC_ERROR	AE21	AF20	AN25			
B8	VREF2B8	IO	DQ6B1		AJ21	AK22	AR25	DQ2B1	DQ1B1	
B8	VREF2B8	IO					AM25			
B8	VREF2B8	IO	DQ6B0		AK21	AL22	AV25	DQ2B0	DQ1B0	
B8	VREF2B8	VREF2B8			AB20	AH23	AJ27			
B8	VREF2B8	IO	RDN8		AE23	AC20	AH24			
B8	VREF2B8	IO			AC19	AD20	AK24			
B8	VREF2B8	IO					AJ24			
B8	VREF2B8	IO					AL24			
B8	VREF2B8	IO	RUP8		AG25	AH19	AF23			
B8	VREF2B8	IO	DQ5B7		AG20	AM22	AT24			
B8	VREF2B8	IO					AP25			
B8	VREF2B8	IO	DQ5B6		AH20	AJ21	AU24			
B8	VREF2B8	IO			AE20	AE20	AM24			
B8	VREF2B8	IO	DQ5B5		AK20	AK21	AV24			
B8	VREF2B8	IO			AD19	AK18	AN24			
B8	VREF2B8	IO	DQ5B4		AL20	AL21	AW24			
B8	VREF2B8	IO		RDYnBSY	AG23	AA19	AH23			
B8	VREF2B8	IO	DQ5B3		AG19	AH20	AW23			
B8	VREF2B8	IO			AE19	AB19	AP24			
B8	VREF2B8	IO	DQS5B		AJ20	AJ20	AU23			
B8	VREF2B8	IO				AJ18	AR24			
B8	VREF2B8	IO	DQ5B2		AH19	AK20	AR23			
B8	VREF3B8	IO		nCS	AF20	AC19	AL23			
B8	VREF3B8	IO	DQ5B1		AJ19	AL20	AV23			
B8	VREF3B8	IO				AD19	AK23			
B8	VREF3B8	IO	DQ5B0		AK19	AM20	AT23			
B8	VREF3B8	IO					AM23			
B8	VREF3B8	IO		CS	AF21	AG19	AJ23			
B8	VREF3B8	IO					AR22			
B8	VREF3B8	IO					AL22			
B8	VREF3B8	IO					AN23			
B8	VREF3B8	IO					AN22			
B8	VREF3B8	IO					AP23			
B8	VREF3B8	IO			AE18	AH18	AP22			
B8	VREF3B8	VREF3B8			AB19	AH21	AJ26			
B8	VREF3B8	IO	CLK5n		AH18	AJ19	AU22			
B8	VREF3B8	CLK5p			AJ18	AK19	AT22			
B8	VREF3B8	IO	CLK4n		AK18	AL19	AW22			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF3B8	CLK4p			AL18	AM19	AV22			
B8	VREF3B8	PLL_ENA		PLL_ENA	AF19	AF19	AM22			
B8	VREF3B8	MSEL0		MSEL0	AF18	AG18	AP21			
B8	VREF3B8	MSEL1		MSEL1	AG18	AE18	AG21			
B8	VREF3B8	MSEL2		MSEL2	AG17	AE19	AM21			
B12	VREF3B8	IO	PLL6_OUT3n		AL17	AM18	AV20			
B12	VREF3B8	IO	PLL6_OUT3p		AK17	AL18	AW20			
B12	VREF3B8	IO	PLL6_OUT2n		AJ17	AK17	AW21			
B12	VREF3B8	IO	PLL6_OUT2p		AH17	AJ17	AV21			
B11	VREF3B8	IO	PLL6_FBn		AJ15	AM17	AU20			
B11	VREF3B8	IO	PLL6_FBp		AH15	AL17	AT20			
B11	VREF3B8	IO	PLL6_OUT1n		AL15	AK16	AU21			
B11	VREF3B8	IO	PLL6_OUT1p		AK15	AJ16	AT21			
B11	VREF3B8	IO	PLL6_OUT0n		AL16	AM16	AU19			
B11	VREF3B8	IO	PLL6_OUT0p		AK16	AL16	AT19			
B12		VCC_PLL6_OUTB			AC18	AB17	AH21			
B11		VCC_PLL6_OUTA			AD17	AE17	AJ21			
		VCCA_PLL6			AB17	AG17	AK21			
		GND								
		GNDA_PLL6			AC17	AH17	AL20			
		VCCG_PLL6			AD15	AD16	AJ20			
		GNDG_PLL6			AD16	AB16	AH20			
		VCCA_PLL12			AC14	AG16	AK19			
		GND								
		GNDA_PLL12			AD14	AH16	AL19			
		VCCG_PLL12			AC15	AF16	AJ19			
		GNDG_PLL12			AB15	AE16	AH19			
B7	VREF0B7	CLK7p			AJ14	AM15	AW18			
B7	VREF0B7	IO	CLK7n		AH14	AL15	AV18			
B7	VREF0B7	CLK6p			AL14	AK15	AW19			
B7	VREF0B7	IO	CLK6n/PLL12_OUT		AK14	AJ15	AV19			
B7	VREF0B7	nCE		nCE	AF17	AF18	AN20			
B7	VREF0B7	nCEO		nCEO	AF16	AH15	AP20			
B7	VREF0B7	IO					AP19			
B7	VREF0B7	IO					AR19			
B7	VREF0B7	IO		PGM0	AE17	AD18	AG20			
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	AE16	AF15	AR20			
B7	VREF0B7	VCCSEL		VCCSEL	AE15	AJ14	AM19			
B7	VREF0B7	PORSEL		PORSEL	AG16	AG15	AN19			
B7	VREF0B7	IO					AH18			
B7	VREF0B7	IO					AJ18			
B7	VREF0B7	IO		INIT_DONE	AF15	AE15	AL18			
B7	VREF0B7	IO					AM18			
B7	VREF0B7	IO					AK18			
B7	VREF0B7	IO					AN18			
B7	VREF0B7	VREF0B7			AB14	AH12	AJ15			
B7	VREF0B7	IO			AA16	AC18	AP18			
B7	VREF0B7	IO					AR16			
B7	VREF0B7	IO					AR18			
B7	VREF0B7	IO					AM17			
B7	VREF0B7	IO					AT18			
B7	VREF0B7	IO					AU18			
B7	VREF0B7	IO		nRS	AE14	AB18	AL17			
B7	VREF0B7	IO				AA18	AH17			
B7	VREF0B7	IO	DQ4B7		AK13	AL13	AU17			
B7	VREF0B7	IO			AH16	AE14	AJ17			
B7	VREF0B7	IO	DQ4B6		AG13	AM13	AR17			
B7	VREF0B7	IO		RUnLU	AJ16	AF14	AK17			
B7	VREF0B7	IO	DQ4B5		AH13	AH13	AT17			
B7	VREF0B7	IO			AA15	AD14	AM16			
B7	VREF0B7	IO	DQ4B4		AJ13	AJ13	AV17			
B7	VREF0B7	IO				AD15	AP16			
B7	VREF0B7	IO	DQ4B3		AK12	AK13	AV16			
B7	VREF0B7	IO		PGM1	AG15	AG14	AF16			
B7	VREF1B7	IO	DQS4B		AJ12	AJ12	AU16			
B7	VREF1B7	IO			AA13	AB15	AH16			
B7	VREF1B7	IO	DQ4B2		AL12	AK12	AW17			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF1B7	IO				AC15	AP15			
B7	VREF1B7	IO	DQ4B1		AG12	AL12	AT16			
B7	VREF1B7	IO	DEV_CLRn		AF14	AH14	AN17			
B7	VREF1B7	IO	DQ4B0		AH12	AM11	AW16			
B7	VREF1B7	IO	RDN7		AG14	AC14	AP17			
B7	VREF1B7	IO					AK16			
B7	VREF1B7	IO					AJ16			
B7	VREF1B7	IO			AD13	AK14	AL16			
B7	VREF1B7	IO	RUP7		AF13	AF13	AN16			
B7	VREF1B7	IO	DQ3B7		AL10	AL10	AT15	DQ1B15	DQ0B31	
B7	VREF1B7	IO				AA15	AL15			
B7	VREF1B7	IO	DQ3B6		AJ11	AK11	AR15	DQ1B14	DQ0B30	
B7	VREF1B7	IO			AC13	AE13	AM15			
B7	VREF1B7	IO	DQ3B5		AK11	AL11	AV15	DQ1B13	DQ0B29	
B7	VREF1B7	IO			AE13	AG13	AN15			
B7	VREF1B7	VREF1B7			AB13	AH10	AJ14			
B7	VREF1B7	IO	DQ3B4		AG11	AK10	AV14	DQ1B12	DQ0B28	
B7	VREF1B7	IO					AP13			
B7	VREF1B7	IO	DQ3B3		AH11	AM9	AW14	DQ1B11	DQ0B27	
B7	VREF1B7	IO			AD12	AD13	AM14			
B7	VREF1B7	IO	DQS3B		AJ10	AJ11	AU15	DQS1B		
B7	VREF1B7	IO			AE12	AL14	AP14			
B7	VREF1B7	IO	DQ3B2		AG10	AL9	AR14	DQ1B10	DQ0B26	
B7	VREF1B7	IO			AC12	AE12	AR11			
B7	VREF1B7	IO	DQ3B1		AH10	AJ10	AT14	DQ1B9	DQ0B25	
B7	VREF1B7	IO				AB14	AN13			
B7	VREF1B7	IO	DQ3B0		AK10	AH11	AU14	DQ1B8	DQ0B24	
B7	VREF1B7	IO					AK15			
B7	VREF1B7	IO					AM13			
B7	VREF1B7	IO					AP11			
B7	VREF1B7	IO					AL14			
B7	VREF1B7	IO	DQ2B7		AL8	AL8	AT13	DQ1B7	DQ0B23	
B7	VREF1B7	IO	FCLK5		AF12	AM14	AN14			
B7	VREF1B7	IO	FCLK4		AF11	AF12	AT11			
B7	VREF2B7	IO	DQ2B6		AK9	AJ9	AU13	DQ1B6	DQ0B22	
B7	VREF2B7	IO				AB13	AM12			
B7	VREF2B7	IO	DQ2B5		AL9	AK9	AV13	DQ1B5	DQ0B21	
B7	VREF2B7	IO			AG9	AA14	AT10			
B7	VREF2B7	IO	DQ2B4		AH8	AM8	AV12	DQ1B4	DQ0B20	
B7	VREF2B7	IO			AE11	AC13	AP12			
B7	VREF2B7	IO	DQ2B3		AK8	AH9	AR13	DQ1B3	DQ0B19	
B7	VREF2B7	IO					AP10			
B7	VREF2B7	IO	DQS2B		AJ8	AK8	AU12		DQS0B	
B7	VREF2B7	IO			AE10	AE11	AR10			
B7	VREF2B7	IO	DQ2B2		AG8	AM7	AR12	DQ1B2	DQ0B18	
B7	VREF2B7	IO			AF10	AD12	AK14			
B7	VREF2B7	IO	DQ2B1		AH9	AJ8	AT12	DQ1B1	DQ0B17	
B7	VREF2B7	IO				AC12	AL12			
B7	VREF2B7	IO	DQ2B0		AJ9	AL7	AW12	DQ1B0	DQ0B16	
B7	VREF2B7	IO					AN11			
B7	VREF2B7	IO					AN12			
B7	VREF2B7	IO			AD11	AG12	AL13			
B7	VREF2B7	VREF2B7			AB12	AH8	AJ13			
B7	VREF2B7	IO					AT8			
B7	VREF2B7	IO			AA11	AD11	AN10			
B7	VREF2B7	IO	DQ1B7		AK7	AL6	AV11	DQ0B15	DQ0B15	
B7	VREF2B7	IO				AA13	AK13			
B7	VREF2B7	IO	DQ1B6		AL7	AM6	AW11	DQ0B14	DQ0B14	
B7	VREF2B7	IO			AF9	AF11	AT9			
B7	VREF2B7	IO	DQ1B5		AH6	AJ7	AU10	DQ0B13	DQ0B13	
B7	VREF2B7	IO			AD10	AB12	AW5			
B7	VREF2B7	IO	DQ1B4		AK6	AM5	AW10	DQ0B12	DQ0B12	
B7	VREF2B7	IO			AC11	AE10	AM11			
B7	VREF2B7	IO	DQ1B3		AL6	AK7	AU11	DQ0B11	DQ0B11	
B7	VREF2B7	IO					AR9			
B7	VREF2B7	IO	DQS1B		AJ6	AH7	AV10	DQS0B		
B7	VREF2B7	IO			AC10	AD10	AV5			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF2B7	IO	DQ1B2		AH7	AL5	AW9	DQ0B10	DQ0B10	
B7	VREF2B7	IO			AE9	AC11	AR8			
B7	VREF2B7	IO	DQ1B1		AJ7	AK6	AV9	DQ0B9	DQ0B9	
B7	VREF2B7	IO				AF10	AP9			
B7	VREF3B7	IO	DQ1B0		AG6	AJ6	AU9	DQ0B8	DQ0B8	
B7	VREF3B7	IO					AR7			
B7	VREF3B7	IO					AT7			
B7	VREF3B7	IO					AW4			
B7	VREF3B7	IO					AK12			
B7	VREF3B7	IO			AF8	AG11	AL11			
B7	VREF3B7	IO	DQ0B7		AL4	AL3	AV8	DQ0B7	DQ0B7	
B7	VREF3B7	IO				AB11	AM9			
B7	VREF3B7	IO	DQ0B6		AL5	AL4	AW8	DQ0B6	DQ0B6	
B7	VREF3B7	IO			AH4	AE9	AK11			
B7	VREF3B7	IO	DQ0B5		AJ4	AM4	AW6	DQ0B5	DQ0B5	
B7	VREF3B7	IO			AG7	AF9	AN9			
B7	VREF3B7	VREF3B7			AB11	AH6	AJ12			
B7	VREF3B7	IO	DQ0B4		AK3	AJ4	AU8	DQ0B4	DQ0B4	
B7	VREF3B7	IO					AR6			
B7	VREF3B7	IO	DQ0B3		AK5	AJ5	AW7	DQ0B3	DQ0B3	
B7	VREF3B7	IO			AF6	AA12	AU5			
B7	VREF3B7	IO	DQS0B		AK4	AK5	AV7			
B7	VREF3B7	IO			AE8	AG10	AP8			
B7	VREF3B7	IO	DQ0B2		AH5	AH5	AU7	DQ0B2	DQ0B2	
B7	VREF3B7	IO			AG4	AC9	AN7			
B7	VREF3B7	IO	DQ0B1		AJ5	AK3	AV6	DQ0B1	DQ0B1	
B7	VREF3B7	IO				AD9	AP7			
B7	VREF3B7	IO	DQ0B0		AJ3	AK4	AU6	DQ0B0	DQ0B0	
B7	VREF3B7	IO					AL10			
B7	VREF3B7	IO					AU4			
B7	VREF3B7	IO					AR5			
B7	VREF3B7	IO					AN8			
B7	VREF3B7	IO					AT5			
B7	VREF3B7	IO					AT6			
B7	VREF3B7	IO			AJ2	AG9	AV4			
		GNDG_PLL9			AC9	AH3	AK9			
		VCCG_PLL9			AD9	AJ3	AL9			
		GNDA_PLL9			AA9	AJ1	AJ9			
		GND								
		VCCA_PLL9			AB9	AJ2	AJ10			
B6	VREF0B6	IO					AG10			
B6	VREF0B6	IO					AG9			
B6	VREF0B6	FPLL9CLKp			AH1	AB5	AL1			
B6	VREF0B6	FPLL9CLKn			AG1	AB4	AL2			
B6	VREF0B6	IO	DIFFIO_TX115n		AC8	AF8	AH10			HIGH
B6	VREF0B6	IO	DIFFIO_TX115p		AD8	AF7	AH9			HIGH
B6	VREF0B6	IO	DIFFIO_RX115n				AR4			LOW
B6	VREF0B6	IO	DIFFIO_RX115p				AR3			LOW
B6	VREF0B6	IO	DIFFIO_TX114n		AF7	AF5	AL8			HIGH
B6	VREF0B6	IO	DIFFIO_TX114p		AE7	AF6	AL7			HIGH
B6	VREF0B6	IO	DIFFIO_RX114n				AP3			LOW
B6	VREF0B6	IO	DIFFIO_RX114p				AP4			LOW
B6	VREF0B6	IO	DIFFIO_TX113n		AB8	AE7	AK7			HIGH
B6	VREF0B6	IO	DIFFIO_TX113p		AA8	AE8	AK8			HIGH
B6	VREF0B6	IO	DIFFIO_RX113n				AM6			LOW
B6	VREF0B6	IO	DIFFIO_RX113p				AM5			LOW
B6	VREF0B6	VREF0B6			AA10	AG6	AH11			
B6	VREF0B6	IO	DIFFIO_TX112n		AC7	AD6	AJ7			HIGH
B6	VREF0B6	IO	DIFFIO_TX112p		AD7	AD5	AJ8			HIGH
B6	VREF0B6	IO	DIFFIO_RX112n				AT2			LOW
B6	VREF0B6	IO	DIFFIO_RX112p				AT1			LOW
B6	VREF0B6	IO	DIFFIO_TX111n		AB7	AE6	AH8			HIGH
B6	VREF0B6	IO	DIFFIO_TX111p		AA7	AE5	AH7			HIGH
B6	VREF0B6	IO	DIFFIO_RX111n				AR2			LOW
B6	VREF0B6	IO	DIFFIO_RX111p				AR1			LOW
B6	VREF0B6	IO	DIFFIO_TX110n		AE6	AD8	AG8			HIGH
B6	VREF0B6	IO	DIFFIO_TX110p		AD6	AD7	AG7			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF0B6	IO	DIFFIO_RX110n				AN4			LOW
B6	VREF0B6	IO	DIFFIO_RX110p				AN3			LOW
B6	VREF0B6	IO	DIFFIO_TX109n		AC6	AC5	AK6			HIGH
B6	VREF0B6	IO	DIFFIO_TX109p		AB6	AC6	AK5			HIGH
B6	VREF0B6	IO	DIFFIO_RX109n				AP1			LOW
B6	VREF0B6	IO	DIFFIO_RX109p				AP2			LOW
B6	VREF1B6	IO	DIFFIO_TX108n		AF5	AC7	AJ5			HIGH
B6	VREF1B6	IO	DIFFIO_TX108p		AG5	AC8	AJ6			HIGH
B6	VREF1B6	IO	DIFFIO_RX108n			AG7	AM4			LOW
B6	VREF1B6	IO	DIFFIO_RX108p			AG8	AM3			LOW
B6	VREF1B6	IO	DIFFIO_TX107n		AD5	AB7	AH5			HIGH
B6	VREF1B6	IO	DIFFIO_TX107p		AE5	AB6	AH6			HIGH
B6	VREF1B6	IO	DIFFIO_RX107n			AG5	AN2			LOW
B6	VREF1B6	IO	DIFFIO_RX107p			AH4	AN1			LOW
B6	VREF1B6	IO	DIFFIO_TX106n		AC5	AA6	AG6			HIGH
B6	VREF1B6	IO	DIFFIO_TX106p		AB5	AA7	AG5			HIGH
B6	VREF1B6	IO	DIFFIO_RX106n			AH2	AM2			LOW
B6	VREF1B6	IO	DIFFIO_RX106p			AH1	AM1			LOW
B6	VREF1B6	IO	DIFFIO_TX105n		AA6	AA9	AF8			HIGH
B6	VREF1B6	IO	DIFFIO_TX105p		Y6	AA8	AF7			HIGH
B6	VREF1B6	IO	DIFFIO_RX105n		AF4	AG4	AL4			HIGH
B6	VREF1B6	IO	DIFFIO_RX105p		AE4	AG3	AL3			HIGH
B6	VREF1B6	VREF1B6			Y10	AB8	AG11			
B6	VREF1B6	IO	DIFFIO_TX104n		Y9	Y5	AF6			HIGH
B6	VREF1B6	IO	DIFFIO_TX104p		W9	Y6	AF5			HIGH
B6	VREF1B6	IO	DIFFIO_RX104n		AD4	AG1	AK4			HIGH
B6	VREF1B6	IO	DIFFIO_RX104p		AC4	AG2	AK3			HIGH
B6	VREF1B6	IO	DIFFIO_TX103n		Y8	Y7	AE8			HIGH
B6	VREF1B6	IO	DIFFIO_TX103p		W8	Y8	AE7			HIGH
B6	VREF1B6	IO	DIFFIO_RX103n		AG3	AF4	AK1			HIGH
B6	VREF1B6	IO	DIFFIO_RX103p		AH3	AF3	AK2			HIGH
B6	VREF1B6	IO	DIFFIO_TX102n		AA5	W5	AE6			HIGH
B6	VREF1B6	IO	DIFFIO_TX102p		Y5	W6	AE5			HIGH
B6	VREF1B6	IO	DIFFIO_RX102n		AF3	AF2	AJ4			HIGH
B6	VREF1B6	IO	DIFFIO_RX102p		AE3	AF1	AJ3			HIGH
B6	VREF1B6	IO	DIFFIO_TX101n		Y7	Y10	AD10			HIGH
B6	VREF1B6	IO	DIFFIO_TX101p		W7	Y9	AD9			HIGH
B6	VREF1B6	IO	DIFFIO_RX101n		AD3	AE4	AJ2			HIGH
B6	VREF1B6	IO	DIFFIO_RX101p		AC3	AE3	AJ1			HIGH
B6	VREF2B6	IO	DIFFIO_TX100n		U7	W10	AD8			HIGH
B6	VREF2B6	IO	DIFFIO_TX100p		V7	W9	AD7			HIGH
B6	VREF2B6	IO	DIFFIO_RX100n		AH2	AE2	AH4			HIGH
B6	VREF2B6	IO	DIFFIO_RX100p		AG2	AE1	AH3			HIGH
B6	VREF2B6	IO	DIFFIO_TX99n		W6	V9	AD5			HIGH
B6	VREF2B6	IO	DIFFIO_TX99p		V6	V10	AD6			HIGH
B6	VREF2B6	IO	DIFFIO_RX99n		AE2	AC3	AH1			HIGH
B6	VREF2B6	IO	DIFFIO_RX99p		AF2	AC4	AH2			HIGH
B6	VREF2B6	IO	DIFFIO_TX98n		U6	V5	AC5			HIGH
B6	VREF2B6	IO	DIFFIO_TX98p		T6	V6	AC6			HIGH
B6	VREF2B6	IO	DIFFIO_RX98n		AD2	AD3	AG4			HIGH
B6	VREF2B6	IO	DIFFIO_RX98p		AC2	AD4	AG3			HIGH
B6	VREF2B6	IO	DIFFIO_TX97n		W5	V8	AC7			HIGH
B6	VREF2B6	IO	DIFFIO_TX97p		V5	V7	AC8			HIGH
B6	VREF2B6	IO	DIFFIO_RX97n		AF1	AD2	AG2			HIGH
B6	VREF2B6	IO	DIFFIO_RX97p		AE1	AD1	AF2			HIGH
B6	VREF2B6	VREF2B6			W10	AA10	AF11			
B6	VREF2B6	IO	DIFFIO_TX96n		T5	W8	AB5			HIGH
B6	VREF2B6	IO	DIFFIO_TX96p		U5	W7	AB6			HIGH
B6	VREF2B6	IO	DIFFIO_RX96n		AD1	AC2	AF1			HIGH
B6	VREF2B6	IO	DIFFIO_RX96p		AC1	AB1	AE2			HIGH
B6	VREF2B6	IO	DIFFIO_TX95n			AB9	AD12			LOW
B6	VREF2B6	IO	DIFFIO_TX95p			AC10	AD11			LOW
B6	VREF2B6	IO	DIFFIO_RX95n/RDN6		AB4	AA4	AF4			HIGH
B6	VREF2B6	IO	DIFFIO_RX95p/RUP6		AB3	AA5	AF3			HIGH
B6	VREF2B6	IO	DIFFIO_TX94n			AB10	AC11			LOW
B6	VREF2B6	IO	DIFFIO_TX94p			AA11	AC12			LOW
B6	VREF2B6	IO	DIFFIO_RX94n		Y4	AB3	AE4			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF2B6	IO	DIFFIO_RX94p		AA4	AB2	AE3			HIGH
B6	VREF2B6	IO	DIFFIO_TX93n			Y11	AC9			LOW
B6	VREF2B6	IO	DIFFIO_TX93p			Y12	AC10			LOW
B6	VREF2B6	IO	DIFFIO_RX93n		W4	AA3	AD4			HIGH
B6	VREF2B6	IO	DIFFIO_RX93p		V4	AA2	AD3			HIGH
B6	VREF3B6	IO	DIFFIO_TX92n			W11	AB10			LOW
B6	VREF3B6	IO	DIFFIO_TX92p			W12	AB11			LOW
B6	VREF3B6	IO	DIFFIO_RX92n		AA3	Y4	AD2			HIGH
B6	VREF3B6	IO	DIFFIO_RX92p		Y3	Y3	AD1			HIGH
B6	VREF3B6	IO	DIFFIO_TX91n				AB13			LOW
B6	VREF3B6	IO	DIFFIO_TX91p				AB12			LOW
B6	VREF3B6	IO	DIFFIO_RX91n		W3	Y2	AC4			HIGH
B6	VREF3B6	IO	DIFFIO_RX91p		V3	Y1	AC3			HIGH
B6	VREF3B6	IO	DIFFIO_TX90n				AB8			LOW
B6	VREF3B6	IO	DIFFIO_TX90p				AB9			LOW
B6	VREF3B6	IO	DIFFIO_RX90n		AB2	W4	AC2			HIGH
B6	VREF3B6	IO	DIFFIO_RX90p		AA2	W3	AC1			HIGH
B6	VREF3B6	IO	DIFFIO_TX89n				AB7			LOW
B6	VREF3B6	IO	DIFFIO_TX89p				AA6			LOW
B6	VREF3B6	IO	DIFFIO_RX89n		Y2	W2	AB4			HIGH
B6	VREF3B6	IO	DIFFIO_RX89p		W2	W1	AB3			HIGH
B6	VREF3B6	VREF3B6			V10	V12	AE11			
B6	VREF3B6	IO	DIFFIO_TX88n				AA12			LOW
B6	VREF3B6	IO	DIFFIO_TX88p				AA13			LOW
B6	VREF3B6	IO	DIFFIO_RX88n		AA1	V4	AB1			HIGH
B6	VREF3B6	IO	DIFFIO_RX88p		AB1	V3	AB2			HIGH
B6	VREF3B6	IO	DIFFIO_TX87n				AA11			LOW
B6	VREF3B6	IO	DIFFIO_TX87p				AA10			LOW
B6	VREF3B6	IO	DIFFIO_RX87n		V2	V2	AA4			HIGH
B6	VREF3B6	IO	DIFFIO_RX87p		U2	V1	AA3			HIGH
B6	VREF3B6	IO	DIFFIO_TX86n				AA9			LOW
B6	VREF3B6	IO	DIFFIO_TX86p				AA8			LOW
B6	VREF3B6	IO	DIFFIO_RX86n		V1	U5	AA2			HIGH
B6	VREF3B6	IO	DIFFIO_RX86p		U1	U6	AA1			HIGH
B6	VREF3B6	IO	CLK8n		U4	U3	Y5			
B6	VREF3B6	CLK8p			U3	U4	Y6			
B6	VREF3B6	CLK9n			T3	U1	Y2			
B6	VREF3B6	CLK9p			T4	U2	Y1			
		GNDG_PLL3			V9	U11	Y11			
		VCCG_PLL3			U9	V11	Y12			
		GNDA_PLL3			V8	U7	Y9			
		GND								
		VCCA_PLL3			U8	U8	W8			
		GNDG_PLL4			R9	U9	W11			
		VCCG_PLL4			R10	T9	W12			
		GNDA_PLL4			R8	T7	W9			
		GND								
		VCCA_PLL4			T8	T8	W10			
B5	VREF0B5	CLK10p			T1	T6	Y3			
B5	VREF0B5	IO	CLK10n		T2	T5	Y4			
B5	VREF0B5	CLK11p			R3	T4	W5			
B5	VREF0B5	CLK11n			R4	T3	W6			
B5	VREF0B5	IO	DIFFIO_TX85n				Y7			LOW
B5	VREF0B5	IO	DIFFIO_TX85p				W7			LOW
B5	VREF0B5	IO	DIFFIO_RX85n		R1	T2	W1			HIGH
B5	VREF0B5	IO	DIFFIO_RX85p		P1	T1	W2			HIGH
B5	VREF0B5	IO	DIFFIO_TX84n				V7			LOW
B5	VREF0B5	IO	DIFFIO_TX84p				V8			LOW
B5	VREF0B5	IO	DIFFIO_RX84n		P2	R1	W4			HIGH
B5	VREF0B5	IO	DIFFIO_RX84p		R2	R2	W3			HIGH
B5	VREF0B5	IO	DIFFIO_TX83n				V9			LOW
B5	VREF0B5	IO	DIFFIO_TX83p				V10			LOW
B5	VREF0B5	IO	DIFFIO_RX83n		K1	R3	V1			HIGH
B5	VREF0B5	IO	DIFFIO_RX83p		L1	R4	V2			HIGH
B5	VREF0B5	IO	DIFFIO_TX82n				W14			LOW
B5	VREF0B5	IO	DIFFIO_TX82p				V14			LOW
B5	VREF0B5	IO	DIFFIO_RX82n		N2	P1	V3			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF0B5	IO	DIFFIO_RX82p		M2	P2	V4			HIGH
B5	VREF0B5	VREF0B5			P10	R12	R11			
B5	VREF0B5	IO	DIFFIO_TX81n				V11			LOW
B5	VREF0B5	IO	DIFFIO_TX81p				V12			LOW
B5	VREF0B5	IO	DIFFIO_RX81n		L2	P3	U1			HIGH
B5	VREF0B5	IO	DIFFIO_RX81p		K2	P4	U2			HIGH
B5	VREF0B5	IO	DIFFIO_TX80n				U13			LOW
B5	VREF0B5	IO	DIFFIO_TX80p				V13			LOW
B5	VREF0B5	IO	DIFFIO_RX80n		P3	N1	U3			HIGH
B5	VREF0B5	IO	DIFFIO_RX80p		N3	N2	U4			HIGH
B5	VREF0B5	IO	DIFFIO_TX79n			T11	U12			LOW
B5	VREF0B5	IO	DIFFIO_TX79p			R11	U11			LOW
B5	VREF0B5	IO	DIFFIO_RX79n		L3	N3	T2			HIGH
B5	VREF0B5	IO	DIFFIO_RX79p		M3	N4	T1			HIGH
B5	VREF0B5	IO	DIFFIO_TX78n			P11	U9			LOW
B5	VREF0B5	IO	DIFFIO_TX78p			N11	U10			LOW
B5	VREF0B5	IO	DIFFIO_RX78n		P4	M2	T3			HIGH
B5	VREF0B5	IO	DIFFIO_RX78p		N4	M3	T4			HIGH
B5	VREF0B5	IO	DIFFIO_TX77n		R7	R7	V6			HIGH
B5	VREF0B5	IO	DIFFIO_TX77p		T7	R8	V5			HIGH
B5	VREF0B5	IO	DIFFIO_RX77n		M4	L2	R3			HIGH
B5	VREF0B5	IO	DIFFIO_RX77p		L4	L3	R4			HIGH
B5	VREF1B5	IO	DIFFIO_TX76n		P8	P7	U8			HIGH
B5	VREF1B5	IO	DIFFIO_TX76p		N8	P8	U7			HIGH
B5	VREF1B5	IO	DIFFIO_RX76n/RDN5		K3	M4	P3			HIGH
B5	VREF1B5	IO	DIFFIO_RX76p/RUP5		K4	M5	P4			HIGH
B5	VREF1B5	IO	DIFFIO_TX75n		R6	R5	U6			HIGH
B5	VREF1B5	IO	DIFFIO_TX75p		P6	R6	U5			HIGH
B5	VREF1B5	IO	DIFFIO_RX75n		J1	L1	R2			HIGH
B5	VREF1B5	IO	DIFFIO_RX75p		H1	K2	P1			HIGH
B5	VREF1B5	IO	DIFFIO_TX74n		P9	R10	T5			HIGH
B5	VREF1B5	IO	DIFFIO_TX74p		N9	R9	T6			HIGH
B5	VREF1B5	IO	DIFFIO_RX74n		G1	J2	P2			HIGH
B5	VREF1B5	IO	DIFFIO_RX74p		F1	J1	N2			HIGH
B5	VREF1B5	IO	DIFFIO_TX73n		P7	P6	T7			HIGH
B5	VREF1B5	IO	DIFFIO_TX73p		N7	P5	T8			HIGH
B5	VREF1B5	IO	DIFFIO_RX73n		H2	K4	N4			HIGH
B5	VREF1B5	IO	DIFFIO_RX73p		J2	K3	N3			HIGH
B5	VREF1B5	IO	DIFFIO_TX72n		N6	N7	T9			HIGH
B5	VREF1B5	IO	DIFFIO_TX72p		M6	N8	T10			HIGH
B5	VREF1B5	IO	DIFFIO_RX72n		G2	J3	M1			HIGH
B5	VREF1B5	IO	DIFFIO_RX72p		F2	J4	M2			HIGH
B5	VREF1B5	VREF1B5			N10	L8	P11			
B5	VREF1B5	IO	DIFFIO_TX71n		R5	P9	R5			HIGH
B5	VREF1B5	IO	DIFFIO_TX71p		P5	P10	R6			HIGH
B5	VREF1B5	IO	DIFFIO_RX71n		J3	H1	M3			HIGH
B5	VREF1B5	IO	DIFFIO_RX71p		H3	H2	M4			HIGH
B5	VREF1B5	IO	DIFFIO_TX70n		M5	N5	R8			HIGH
B5	VREF1B5	IO	DIFFIO_TX70p		N5	N6	R7			HIGH
B5	VREF1B5	IO	DIFFIO_RX70n		G3	G1	L1			HIGH
B5	VREF1B5	IO	DIFFIO_RX70p		F3	G2	L2			HIGH
B5	VREF1B5	IO	DIFFIO_TX69n		M8	N10	P5			HIGH
B5	VREF1B5	IO	DIFFIO_TX69p		L8	N9	P6			HIGH
B5	VREF1B5	IO	DIFFIO_RX69n		J4	H3	L3			HIGH
B5	VREF1B5	IO	DIFFIO_RX69p		H4	H4	L4			HIGH
B5	VREF1B5	IO	DIFFIO_TX68n		M7	M8	P7			HIGH
B5	VREF1B5	IO	DIFFIO_TX68p		L7	M9	P8			HIGH
B5	VREF1B5	IO	DIFFIO_RX68n		G4	F1	K2			HIGH
B5	VREF1B5	IO	DIFFIO_RX68p		F4	F2	K1			HIGH
B5	VREF1B5	IO	DIFFIO_TX67n		L5	M6	N5			HIGH
B5	VREF1B5	IO	DIFFIO_TX67p		K5	M7	N6			HIGH
B5	VREF1B5	IO	DIFFIO_RX67n		E2	G3	K3			HIGH
B5	VREF1B5	IO	DIFFIO_RX67p		D2	G4	K4			HIGH
B5	VREF2B5	IO	DIFFIO_TX66n		H5	L6	N8			HIGH
B5	VREF2B5	IO	DIFFIO_TX66p		J5	L7	N7			HIGH
B5	VREF2B5	IO	DIFFIO_RX66n		E3	F3	J3			HIGH
B5	VREF2B5	IO	DIFFIO_RX66p		D3	F4	J4			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF2B5	IO	DIFFIO_TX65n		F5	K5	M6			HIGH
B5	VREF2B5	IO	DIFFIO_TX65p		G5	K6	M5			HIGH
B5	VREF2B5	IO	DIFFIO_RX65n			E2	H2			LOW
B5	VREF2B5	IO	DIFFIO_RX65p			E1	H1			LOW
B5	VREF2B5	IO	DIFFIO_TX64n		L6	K8	L5			HIGH
B5	VREF2B5	IO	DIFFIO_TX64p		K6	K7	L6			HIGH
B5	VREF2B5	IO	DIFFIO_RX64n			F5	G2			LOW
B5	VREF2B5	IO	DIFFIO_RX64p			E4	G1			LOW
B5	VREF2B5	IO	DIFFIO_TX63n		J6	J5	M7			HIGH
B5	VREF2B5	IO	DIFFIO_TX63p		H6	J6	M8			HIGH
B5	VREF2B5	IO	DIFFIO_RX63n				H3			LOW
B5	VREF2B5	IO	DIFFIO_RX63p				H4			LOW
B5	VREF2B5	IO	DIFFIO_TX62n		G6	J7	K5			HIGH
B5	VREF2B5	IO	DIFFIO_TX62p		F6	J8	K6			HIGH
B5	VREF2B5	IO	DIFFIO_RX62n				F1			LOW
B5	VREF2B5	IO	DIFFIO_RX62p				F2			LOW
B5	VREF2B5	VREF2B5			M10	F6	N11			
B5	VREF2B5	IO	DIFFIO_TX61n		K8	H5	L8			HIGH
B5	VREF2B5	IO	DIFFIO_TX61p		J8	H6	L7			HIGH
B5	VREF2B5	IO	DIFFIO_RX61n				E1			LOW
B5	VREF2B5	IO	DIFFIO_RX61p				E2			LOW
B5	VREF2B5	IO	DIFFIO_TX60n		K7	H8	K7			HIGH
B5	VREF2B5	IO	DIFFIO_TX60p		J7	H7	K8			HIGH
B5	VREF2B5	IO	DIFFIO_RX60n				G4			LOW
B5	VREF2B5	IO	DIFFIO_RX60p				G3			LOW
B5	VREF2B5	IO	DIFFIO_TX59n		H7	G6	J7			HIGH
B5	VREF2B5	IO	DIFFIO_TX59p		G7	G5	J8			HIGH
B5	VREF2B5	IO	DIFFIO_RX59n				D1			LOW
B5	VREF2B5	IO	DIFFIO_RX59p				D2			LOW
B5	VREF2B5	IO	DIFFIO_TX58n		G8	G7	M9			HIGH
B5	VREF2B5	IO	DIFFIO_TX58p		H8	G8	M10			HIGH
B5	VREF2B5	IO	DIFFIO_RX58n				F3			LOW
B5	VREF2B5	IO	DIFFIO_RX58p				F4			LOW
B5	VREF2B5	IO					N9			
B5	VREF2B5	IO					N10			
B5	VREF2B5	FPLL10CLKn			D1	L5	J1			
B5	VREF2B5	FPLL10CLKp			E1	L4	J2			
		GNDG_PLL10			K9	E3	L9			
		VCCG_PLL10			J9	D3	L10			
		GNDA_PLL10			M9	D1	K9			
		GND								
		VCCA_PLL10			L9	D2	J9			
B4	VREF0B4	IO			C2	F7	B4			
B4	VREF0B4	IO					D6			
B4	VREF0B4	IO					D5			
B4	VREF0B4	IO					G8			
B4	VREF0B4	IO					E5			
B4	VREF0B4	IO					C4			
B4	VREF0B4	IO			D4	F8	J10			
B4	VREF0B4	IO	DQ0T0		C4	D5	C6	DQ0T0	DQ0T0	
B4	VREF0B4	IO				K9	F7			
B4	VREF0B4	IO	DQ0T1		C5	C3	B6	DQ0T1	DQ0T1	
B4	VREF0B4	IO			E4	L9	G7			
B4	VREF0B4	IO	DQ0T2		D5	E5	C7	DQ0T2	DQ0T2	
B4	VREF0B4	IO			H9	F9	F8			
B4	VREF0B4	IO	DQS0T		B4	C5	B7			
B4	VREF0B4	IO			E5	M10	C5			
B4	VREF0B4	IO	DQ0T3		B5	C4	A7	DQ0T3	DQ0T3	
B4	VREF0B4	IO					E6			
B4	VREF0B4	IO	DQ0T4		B3	D4	C8	DQ0T4	DQ0T4	
B4	VREF0B4	VREF0B4			K10	E6	L11			
B4	VREF0B4	IO			E7	G9	G9			
B4	VREF0B4	IO	DQ0T5		C3	A4	A6	DQ0T5	DQ0T5	
B4	VREF0B4	IO			F7	H9	E7			
B4	VREF0B4	IO	DQ0T6		A5	B4	A8	DQ0T6	DQ0T6	
B4	VREF0B4	IO				J9	H9			
B4	VREF0B4	IO	DQ0T7		A4	B3	B8	DQ0T7	DQ0T7	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF0B4	IO			F8	F10	J11			
B4	VREF0B4	IO					K12			
B4	VREF0B4	IO					A4			
B4	VREF0B4	IO					D7			
B4	VREF0B4	IO					K11			
B4	VREF0B4	IO	DQ1T0		E6	D6	C9	DQ0T8	DQ0T8	
B4	VREF1B4	IO				G10	F9			
B4	VREF1B4	IO	DQ1T1		C7	C6	B9	DQ0T9	DQ0T9	
B4	VREF1B4	IO			J10	L10	E8			
B4	VREF1B4	IO	DQ1T2		D7	B5	A9	DQ0T10	DQ0T10	
B4	VREF1B4	IO					B5			
B4	VREF1B4	IO	DQS1T		C6	E7	B10	DQS0T		
B4	VREF1B4	IO			G10	F11	D8			
B4	VREF1B4	IO	DQ1T3		A6	C7	C11	DQ0T11	DQ0T11	
B4	VREF1B4	IO			J11	H10	H11			
B4	VREF1B4	IO	DQ1T4		B6	A5	A10	DQ0T12	DQ0T12	
B4	VREF1B4	IO			G9	J10	A5			
B4	VREF1B4	IO	DQ1T5		D6	D7	C10	DQ0T13	DQ0T13	
B4	VREF1B4	IO				G11	G11			
B4	VREF1B4	IO	DQ1T6		A7	A6	A11	DQ0T14	DQ0T14	
B4	VREF1B4	IO			F9	K10	K13			
B4	VREF1B4	IO	DQ1T7		B7	B6	B11	DQ0T15	DQ0T15	
B4	VREF1B4	IO			H10	M11	G10			
B4	VREF1B4	IO					J12			
B4	VREF1B4	VREF1B4			K11	E8	L12			
B4	VREF1B4	IO					E10			
B4	VREF1B4	IO					G12			
B4	VREF1B4	IO					F10			
B4	VREF1B4	IO	DQ2T0		B8	B7	A12	DQ1T0	DQ0T16	
B4	VREF1B4	IO				L11	M14			
B4	VREF1B4	IO	DQ2T1		D9	D8	D12	DQ1T1	DQ0T17	
B4	VREF1B4	IO			E9	F12	K14			
B4	VREF1B4	IO	DQ2T2		E8	B8	E12	DQ1T2	DQ0T18	
B4	VREF1B4	IO			H11	H11	D9			
B4	VREF1B4	IO	DQS2T		C8	A7	C12		DQS0T	
B4	VREF1B4	IO			L11	K11	E9			
B4	VREF1B4	IO	DQ2T3		C9	E9	E13	DQ1T3	DQ0T19	
B4	VREF1B4	IO					H13			
B4	VREF1B4	IO	DQ2T4		D8	A8	B12	DQ1T4	DQ0T20	
B4	VREF1B4	IO			J12	L12	F11			
B4	VREF1B4	IO	DQ2T5		A9	C9	B13	DQ1T5	DQ0T21	
B4	VREF1B4	IO				J11	H12			
B4	VREF1B4	IO	DQ2T6		B9	C8	C13	DQ1T6	DQ0T22	
B4	VREF2B4	IO	FCLK6		F10	G12	D11			
B4	VREF2B4	IO	FCLK7		F11	A14	G14			
B4	VREF2B4	IO	DQ2T7		A8	D9	D13	DQ1T7	DQ0T23	
B4	VREF2B4	IO					J14			
B4	VREF2B4	IO					J13			
B4	VREF2B4	IO					D10			
B4	VREF2B4	IO					G13			
B4	VREF2B4	IO	DQ3T0		B10	E11	C14	DQ1T8	DQ0T24	
B4	VREF2B4	IO				H12	F12			
B4	VREF2B4	IO	DQ3T1		D10	B9	D14	DQ1T9	DQ0T25	
B4	VREF2B4	IO			L12	K12	M15			
B4	VREF2B4	IO	DQ3T2		E10	D10	E14	DQ1T10	DQ0T26	
B4	VREF2B4	IO			H12	B14	H14			
B4	VREF2B4	IO	DQS3T		C10	D11	C15	DQS1T		
B4	VREF2B4	IO			G11	J12	K15			
B4	VREF2B4	IO	DQ3T3		D11	C10	A14	DQ1T11	DQ0T27	
B4	VREF2B4	IO					E11			
B4	VREF2B4	IO	DQ3T4		E11	A9	B14	DQ1T12	DQ0T28	
B4	VREF2B4	VREF2B4			K12	E10	L13			
B4	VREF2B4	IO			G12	C14	J15			
B4	VREF2B4	IO	DQ3T5		B11	B11	B15	DQ1T13	DQ0T29	
B4	VREF2B4	IO				K13	F13			
B4	VREF2B4	IO	DQ3T6		C11	C11	E15	DQ1T14	DQ0T30	
B4	VREF2B4	IO	DEV_OE		F12	L13	P16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF2B4	IO	DQ3T7		A10	B10	D15	DQ1T15	DQ0T31	
B4	VREF2B4	IO	RUP4		F13	G13	F15			
B4	VREF2B4	IO			H13	F13	G15			
B4	VREF2B4	IO					L16			
B4	VREF2B4	IO					F14			
B4	VREF2B4	IO	RDN4		E14	J13	E16			
B4	VREF2B4	IO	DQ4T0		D12	A11	A16			
B4	VREF2B4	IO		nWS	F14	D14	F16			
B4	VREF2B4	IO	DQ4T1		E12	B12	D16			
B4	VREF2B4	IO					H15			
B4	VREF2B4	IO	DQ4T2		A12	C12	A17			
B4	VREF2B4	IO			J13	H13	M16			
B4	VREF2B4	IO	DQS4T		C12	D12	C16			
B4	VREF3B4	IO		DATA0	E15	E14	M17			
B4	VREF3B4	IO	DQ4T3		B12	C13	B16			
B4	VREF3B4	IO			G13	K14	J16			
B4	VREF3B4	IO	DQ4T4		C13	D13	B17			
B4	VREF3B4	IO			L14	L14	K16			
B4	VREF3B4	IO	DQ4T5		D13	E13	D17			
B4	VREF3B4	IO		DATA1	C16	F14	J17			
B4	VREF3B4	IO	DQ4T6		E13	A13	E17			
B4	VREF3B4	IO				H14	L17			
B4	VREF3B4	IO	DQ4T7		B13	B13	C17			
B4	VREF3B4	IO			L16	J14	H16			
B4	VREF3B4	IO					G16			
B4	VREF3B4	IO					G17			
B4	VREF3B4	IO					E18			
B4	VREF3B4	IO					H17			
B4	VREF3B4	IO			G14	L15	F18			
B4	VREF3B4	IO					K17			
B4	VREF3B4	IO					F17			
B4	VREF3B4	VREF3B4			K13	E12	L14			
B4	VREF3B4	IO					G18			
B4	VREF3B4	IO					J18			
B4	VREF3B4	IO					H18			
B4	VREF3B4	IO		DATA2	F15	F15	K18			
B4	VREF3B4	IO					L18			
B4	VREF3B4	IO					M18			
B4	VREF3B4	TMS		TMS	D16	E15	F19			
B4	VREF3B4	TRST		TRST	G15	G15	H19			
B4	VREF3B4	TCK		TCK	F16	G14	E20			
B4	VREF3B4	IO		DATA3	G17	C16	P21			
B4	VREF3B4	IO				J15	D18			
B4	VREF3B4	IO				K15	C18			
B4	VREF3B4	TDI		TDI	E16	D16	F20			
B4	VREF3B4	TDO		TDO	G16	F16	G20			
B4	VREF3B4	IO	CLK12n		B14	A15	A18			
B4	VREF3B4	CLK12p			A14	B15	B18			
B4	VREF3B4	IO	CLK13n/PLL11_OUT		D14	C15	C19			
B4	VREF3B4	CLK13p			C14	D15	D19			
		VCCA_PLL11			J14	E16	K19			
		GND								
		GNDA_PLL11			H14	E17	J19			
		VCCG_PLL11			H15	H16	L19			
		GNDG_PLL11			J15	H15	M19			
		TEMPDIODEp			E17	E18	F21			
		TEMPDIODEn			F17	F18	H21			
		VCCA_PLL5			J17	G17	L21			
		GND								
		GNDA_PLL5			H16	F17	M21			
		VCCG_PLL5			K15	J16	L20			
		GNDG_PLL5			K17	L16	M20			
B9		VCC_PLL5_OUTA			L18	H17	J20			
B10		VCC_PLL5_OUTB			J18	L17	K21			
B9	VREF0B3	IO	PLL5_OUT0p		B16	B16	C21			
B9	VREF0B3	IO	PLL5_OUT0n		A16	A16	D21			
B9	VREF0B3	IO	PLL5_OUT1p		B15	B17	C20			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B9	VREF0B3	IO	PLL5_OUT1n		A15	A17	D20			
B9	VREF0B3	IO	PLL5_FBp		D15	D17	B19			
B9	VREF0B3	IO	PLL5_FBn		C15	C17	A19			
B10	VREF0B3	IO	PLL5_OUT2p		D17	B18	B21			
B10	VREF0B3	IO	PLL5_OUT2n		C17	A18	A21			
B10	VREF0B3	IO	PLL5_OUT3p		B17	D18	A20			
B10	VREF0B3	IO	PLL5_OUT3n		A17	C18	B20			
B3	VREF0B3	nSTATUS		nSTATUS	E18	G16	N21			
B3	VREF0B3	nCONFIG		nCONFIG	F19	J18	L22			
B3	VREF0B3	DCLK		DCLK	F18	E19	G21			
B3	VREF0B3	CONF_DONE		CONF_DONE	G18	G18	H22			
B3	VREF0B3	CLK14p			A18	A19	B22			
B3	VREF0B3	IO	CLK14n		B18	B19	A22			
B3	VREF0B3	CLK15p			C18	C19	D22			
B3	VREF0B3	IO	CLK15n		D18	D19	C22			
B3	VREF0B3	VREF0B3			K18	E21	L25			
B3	VREF0B3	IO					G22			
B3	VREF0B3	IO					E22			
B3	VREF0B3	IO					E21			
B3	VREF0B3	IO					F22			
B3	VREF0B3	IO					J22			
B3	VREF0B3	IO			L19	K18	N22			
B3	VREF0B3	IO		DATA4	G19	G19	L23			
B3	VREF0B3	IO					H23			
B3	VREF0B3	IO	DQ5T0		B19	A20	B23			
B3	VREF0B3	IO			H19	H19	K23			
B3	VREF0B3	IO	DQ5T1		C19	B20	E23			
B3	VREF0B3	IO		DATA5	F20	J19	J23			
B3	VREF1B3	IO	DQ5T2		D19	C20	D23			
B3	VREF1B3	IO				F19	F23			
B3	VREF1B3	IO	DQS5T		C20	D20	C23			
B3	VREF1B3	IO			G21	L18	G23			
B3	VREF1B3	IO	DQ5T3		E19	E20	A23			
B3	VREF1B3	IO		DATA6	F21	K19	E24			
B3	VREF1B3	IO	DQ5T4		A20	B21	A24			
B3	VREF1B3	IO				F20	F24			
B3	VREF1B3	IO	DQ5T5		B20	C21	B24			
B3	VREF1B3	IO			J19	G20	G24			
B3	VREF1B3	IO	DQ5T6		D20	D21	C24			
B3	VREF1B3	IO					N23			
B3	VREF1B3	IO	DQ5T7		E20	A22	D24			
B3	VREF1B3	IO	RUP3		F22	F21	P23			
B3	VREF1B3	IO					H24			
B3	VREF1B3	IO					K24			
B3	VREF1B3	IO			H21	H20	J24			
B3	VREF1B3	IO	RDN3		F24	L19	M24			
B3	VREF1B3	VREF1B3			K19	E23	L26			
B3	VREF1B3	IO	DQ6T0		B21	B22	B25	DQ2T0	DQ1T0	
B3	VREF1B3	IO					F25			
B3	VREF1B3	IO	DQ6T1		C21	C22	E25	DQ2T1	DQ1T1	
B3	VREF1B3	IO		DATA7	G20	J20	P25			
B3	VREF1B3	IO	DQ6T2		A22	B23	D25	DQ2T2	DQ1T2	
B3	VREF1B3	IO				K20	L24			
B3	VREF1B3	IO	DQS6T		C22	D22	C25	DQS2T		
B3	VREF1B3	IO			H20	G21	G25			
B3	VREF1B3	IO	DQ6T3		D21	C23	A26	DQ2T3	DQ1T3	
B3	VREF1B3	IO		CLKUSR	F23	H21	J25			
B3	VREF1B3	IO	DQ6T4		E21	A24	B26	DQ2T4	DQ1T4	
B3	VREF1B3	IO				L20	H25			
B3	VREF1B3	IO	DQ6T5		B22	E22	C26	DQ2T5	DQ1T5	
B3	VREF1B3	IO					F26			
B3	VREF1B3	IO	DQ6T6		D22	B24	D26	DQ2T6	DQ1T6	
B3	VREF1B3	IO			J20	J21	K25			
B3	VREF1B3	IO	DQ6T7		E22	D23	E26	DQ2T7	DQ1T7	
B3	VREF1B3	IO					F27			
B3	VREF2B3	IO	FCLK0		E23	F22	G26			
B3	VREF2B3	IO	FCLK1		E25	G22	D29			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF2B3	IO					H26			
B3	VREF2B3	IO					J26			
B3	VREF2B3	IO	DQ7T0		A23	D24	B27	DQ2T8	DQ1T8	
B3	VREF2B3	IO			L21	K21	F28			
B3	VREF2B3	IO	DQ7T1		B23	A25	C27	DQ2T9	DQ1T9	
B3	VREF2B3	IO					G27			
B3	VREF2B3	IO	DQ7T2		A24	C24	D27	DQ2T10	DQ1T10	
B3	VREF2B3	IO				L21	H27			
B3	VREF2B3	IO	DQS7T		C24	B26	C28		DQS1T	
B3	VREF2B3	IO					J27			
B3	VREF2B3	IO	DQ7T3		C23	B25	E27	DQ2T11	DQ1T11	
B3	VREF2B3	IO				H22	K26			
B3	VREF2B3	IO	DQ7T4		D24	C25	B28	DQ2T12	DQ1T12	
B3	VREF2B3	IO					E29			
B3	VREF2B3	IO	DQ7T5		B24	D25	A28	DQ2T13	DQ1T13	
B3	VREF2B3	IO				J22	D31			
B3	VREF2B3	VREF2B3			K20	E25	L27			
B3	VREF2B3	IO	DQ7T6		D23	A26	D28	DQ2T14	DQ1T14	
B3	VREF2B3	IO					D30			
B3	VREF2B3	IO	DQ7T7		E24	E24	E28	DQ2T15	DQ1T15	
B3	VREF2B3	IO					E30			
B3	VREF2B3	IO					H28			
B3	VREF2B3	IO					K27			
B3	VREF2B3	IO					G28			
B3	VREF2B3	IO			G22	F23	F29			
B3	VREF2B3	IO	DQ8T0		A25	C26	A29	DQ3T0	DQ1T16	
B3	VREF2B3	IO			J21	K22	F30			
B3	VREF2B3	IO	DQ8T1		C25	A28	B29	DQ3T1	DQ1T17	
B3	VREF2B3	IO					E31			
B3	VREF2B3	IO	DQ8T2		B25	A27	C29	DQ3T2	DQ1T18	
B3	VREF2B3	IO			H22	G23	G29			
B3	VREF2B3	IO	DQS8T		C26	B27	B30	DQS3T		
B3	VREF2B3	IO				L22	J28			
B3	VREF2B3	IO	DQ8T3		D25	D26	C30	DQ3T3	DQ1T19	
B3	VREF2B3	IO					H29			
		GND			D28	H24	E32			
B3	VREF3B3	IO	DQ8T4		A26	C27	A30	DQ3T4	DQ1T20	
B3	VREF3B3	IO			G23	F24	D32			
B3	VREF3B3	IO	DQ8T5		B26	B28	A31	DQ3T5	DQ1T21	
B3	VREF3B3	IO				H23	K28			
B3	VREF3B3	IO	DQ8T6		E26	D27	B31	DQ3T6	DQ1T22	
B3	VREF3B3	IO					J29			
B3	VREF3B3	IO	DQ8T7		D26	E26	C31	DQ3T7	DQ1T23	
B3	VREF3B3	IO					G30			
B3	VREF3B3	IO					F31			
B3	VREF3B3	IO					D33			
B3	VREF3B3	IO					G31			
B3	VREF3B3	IO			J22	K23	K29			
B3	VREF3B3	IO	DQ9T0		B27	A29	A32	DQ3T8	DQ1T24	
B3	VREF3B3	IO					A35			
B3	VREF3B3	IO	DQ9T1		C27	B29	C32	DQ3T9	DQ1T25	
B3	VREF3B3	IO			H23	J23	F32			
B3	VREF3B3	IO	DQ9T2		A27	B30	B32	DQ3T10	DQ1T26	
B3	VREF3B3	IO			F25	J24	C35			
B3	VREF3B3	VREF3B3			K21	E27	L28			
B3	VREF3B3	IO	DQS9T		B28	C28	B33			
B3	VREF3B3	IO				F25	B35			
B3	VREF3B3	IO	DQ9T3		D27	C29	A34	DQ3T11	DQ1T27	
B3	VREF3B3	IO				G24	D34			
B3	VREF3B3	IO	DQ9T4		A28	D29	A33	DQ3T12	DQ1T28	
B3	VREF3B3	IO			E27	L23	E34			
B3	VREF3B3	IO	DQ9T5		C28	D28	C33	DQ3T13	DQ1T29	
B3	VREF3B3	IO				F26	E33			
B3	VREF3B3	IO	DQ9T6		C29	C30	C34	DQ3T14	DQ1T30	
B3	VREF3B3	IO					F33			
B3	VREF3B3	IO	DQ9T7		B29	E28	B34	DQ3T15	DQ1T31	
B3	VREF3B3	IO			C30	K24	G33			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF3B3	IO					A36			
B3	VREF3B3	IO					B36			
B3	VREF3B3	IO					G32			
B3	VREF3B3	IO					D35			
B3	VREF3B3	IO					C36			
B3	VREF3B3	IO			E28	L24	E35			
		VCCIO2			C31	C31	C39			
		VCCIO2			N31	C32	R39			
		VCCIO2			T23	M32	W35			
		VCCIO2				T23	V25			
		VCCIO2					H33			
		VCCIO1			U20	AA32	AA25			
		VCCIO1			W31	AK31	Y32			
		VCCIO1			AJ31	AK32	AE39			
		VCCIO1				U23	AU39			
		VCCIO1					AM33			
		VCCIO8			AL29	AC17	AW37			
		VCCIO8			AL19	AM21	AW25			
		VCCIO8			Y17	AM30	AR21			
		VCCIO8					AE22			
		VCCIO8					AM30			
		VCCIO7			AC16	AC16	AE19			
		VCCIO7			AL13	AM12	AM20			
		VCCIO7			AL3	AM3	AW15			
		VCCIO7					AW3			
		VCCIO7					AM10			
		VCCIO6			AJ1	AA1	AU1			
		VCCIO6			W1	AK1	AM7			
		VCCIO6			U12	AK2	AE1			
		VCCIO6				U10	AA5			
		VCCIO6					AB15			
		VCCIO5			T9	C1	W15			
		VCCIO5			N1	C2	Y8			
		VCCIO5			C1	M1	R1			
		VCCIO5				T10	H7			
		VCCIO5					C1			
		VCCIO4			A3	A12	A3			
		VCCIO4			A13	A3	A15			
		VCCIO4			J16	K16	E19			
		VCCIO4					R18			
		VCCIO4					H10			
		VCCIO3			M17	A21	H20			
		VCCIO3			A19	A30	R21			
		VCCIO3			A29	K17	A25			
		VCCIO3					A37			
		VCCIO3					H30			
		VCCINT			M11	M12	R16			
		VCCINT			M13	M14	R20			
		VCCINT			M15	M19	R22			
		VCCINT			M19	M21	R24			
		VCCINT			M21	N13	T15			
		VCCINT			N12	N15	T17			
		VCCINT			N14	N18	T19			
		VCCINT			N16	N20	T21			
		VCCINT			N18	P12	T23			
		VCCINT			N20	P14	T25			
		VCCINT			Y11	P16	U16			
		VCCINT			Y13	P17	U18			
		VCCINT			Y15	P19	U20			
		VCCINT			Y19	P21	U22			
		VCCINT			Y21	R13	U24			
		VCCINT			W12	R15	V15			
		VCCINT			W14	R18	V17			
		VCCINT			W16	R20	V19			
		VCCINT			W18	T14	V21			
		VCCINT			W20	T16	V23			
		VCCINT			V11	T17	W16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT			V13	T19	W18			
		VCCINT			V15	U14	W22			
		VCCINT			V17	U16	W24			
		VCCINT			V19	U17	Y15			
		VCCINT			V21	U19	Y17			
		VCCINT			U10	V13	Y23			
		VCCINT			U14	V15	Y25			
		VCCINT			U18	V18	AA16			
		VCCINT			U22	V20	AA18			
		VCCINT			T11	W14	AA22			
		VCCINT			T13	W16	AA24			
		VCCINT			T19	W17	AB17			
		VCCINT			T21	W19	AB19			
		VCCINT			P11	Y13	AB21			
		VCCINT			P13	Y15	AB23			
		VCCINT			P14	Y18	AB25			
		VCCINT			P15	Y20	AC16			
		VCCINT			P17		AC18			
		VCCINT			P19		AC20			
		VCCINT			P21		AC22			
		VCCINT			R12		AC24			
		VCCINT			R13		AD15			
		VCCINT			R14		AD17			
		VCCINT			R18		AD19			
		VCCINT			R19		AD21			
		VCCINT			R20		AD23			
		VCCINT			L20		AD25			
		VCCINT			L13		AE16			
		VCCINT			AA20		AE18			
		VCCINT			AA12		AE20			
		VCCINT			AA14		AE24			
		GND			AD18	AD17				
		GND			AA18	AF17	AK22			
		GND			H17	J17				
		GND			H18	H18	AL21			
		GND			AL30	A10	J21			
		GND			AK30	A2				
		GND			AK31	A23	K22			
		GND			AL31	A31				
		GND			A30	AA16	A2			
		GND			A31	AA17	B2			
		GND			B31	AC1	B1			
		GND			B30	AC32	A38			
		GND			A1	AL1	B38			
		GND			B1	AL2	B39			
		GND			B2	AL31	AV39			
		GND			A2	AL32	AV38			
		GND			AL1	AM10	AW38			
		GND			AK1	AM2	AV1			
		GND			AK2	AM23	AV2			
		GND			AL2	AM31	AW2			
		GND			AL11	B1	AW13			
		GND			AL21	B2	A13			
		GND			A21	B31	A27			
		GND			A11	B32	AW27			
		GND			Y31	K1	N1			
		GND			M31	K32	N39			
		GND			M1	M13	AG39			
		GND			Y1	M15	AG1			
		GND				M16	Y10			
		GND				M17	AA7			
		GND				M18	Y30			
		GND				M20	W33			
		GND				N12	G19			
		GND				N14	K20			
		GND				N16	AK20			
		GND				N17	AN21			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND				N19	AU37			
		GND				N21	C37			
		GND				P13	C3			
		GND				P15	AU3			
		GND				P18	AK30			
		GND				P20	K30			
		GND				R14	K10			
		GND				R16	AK10			
		GND				R17	AM32			
		GND				R19	H32			
		GND				T12	H8			
		GND				T13	AM8			
		GND				T15				
		GND				T18				
		GND				T20				
		GND				T21				
		GND				U12				
		GND				U13				
		GND				U15				
		GND				U18				
		GND				U20				
		GND				U21				
		GND				V14				
		GND				V16				
		GND				V17				
		GND				V19				
		GND				W13				
		GND				W15				
		GND				W18				
		GND				W20				
		GND				Y14				
		GND				Y16				
		GND				Y17				
		GND				Y19				
		GND			AB16					
		GND			Y16					
		GND			V16					
		GND			AA17					
		GND			W17					
		GND			U17					
		GND			K16					
		GND			M16					
		GND			P16					
		GND			L17					
		GND			N17					
		GND			R17					
		GND			T10					
		GND			T12					
		GND			T14					
		GND			U11					
		GND			U13					
		GND			U15					
		GND			T22					
		GND			T20					
		GND			T18					
		GND			U21					
		GND			U19					
		GND			V12					
		GND			V14					
		GND			V18					
		GND			V20					
		GND			M18					
		GND			P18					
		GND			L15					
		GND			N15					
		GND			R15					
		GND			W11					

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			W13					
		GND			W15					
		GND			Y12					
		GND			Y14					
		GND			W21					
		GND			W19					
		GND			Y18					
		GND			Y20					
		GND			M20					
		GND			M14					
		GND			M12					
		GND			N11					
		GND			N13					
		GND			N19					
		GND			N21					
		GND			P12					
		GND			R11					
		GND			R21					
		GND			P20					
		GND					R15			
		GND					R17			
		GND					R19			
		GND					R23			
		GND					R25			
		GND					T16			
		GND					T18			
		GND					T20			
		GND					T22			
		GND					T24			
		GND					U15			
		GND					U17			
		GND					U19			
		GND					U21			
		GND					U23			
		GND					U25			
		GND					V16			
		GND					V18			
		GND					V20			
		GND					V22			
		GND					V24			
		GND					W17			
		GND					W23			
		GND					W25			
		GND					Y16			
		GND					Y18			
		GND					Y22			
		GND					Y24			
		GND					AA15			
		GND					AA17			
		GND					AA23			
		GND					AB16			
		GND					AB18			
		GND					AB20			
		GND					AB22			
		GND					AB24			
		GND					AC15			
		GND					AC17			
		GND					AC19			
		GND					AC21			
		GND					AC23			
		GND					AC25			
		GND					AD16			
		GND					AD18			
		GND					AD20			
		GND					AD22			
		GND					AD24			
		GND					AE15			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND					AE17			
		GND					AE21			
		GND					AE23			
		GND					AE25			
		NC			AB18		AA14			
		NC			AB10		AE10			
		NC			K14		AE31			
		NC			K22		AF18			
		NC			L10		AF27			
		NC			P22		AG16			
		NC					AG26			
		NC					AH25			
		NC					AL6			
		NC					AP34			
		NC					AV37			
		NC					E4			
		NC					G35			
		NC					J35			
		NC					M26			
		NC					N17			
		NC					N27			
		NC					P18			
		NC					P31			
		NC					R30			
		NC					T29			
		NC					Y13			
		NC					AB14			
		NC					AE12			
		NC					AF9			
		NC					AF19			
		NC					AF28			
		NC					AG17			
		NC					AG27			
		NC					AH26			
		NC					AL34			
		NC					AP35			
		NC					B3			
		NC					E36			
		NC					H5			
		NC					L15			
		NC					M27			
		NC					N18			
		NC					N28			
		NC					P19			
		NC					R9			
		NC					R31			
		NC					U26			
		NC					Y14			
		NC					AC13			
		NC					AE13			
		NC					AF10			
		NC					AF20			
		NC					AF30			
		NC					AG18			
		NC					AG28			
		NC					AH27			
		NC					AL35			
		NC					AT3			
		NC					B37			
		NC					E37			
		NC					H6			
		NC					L29			
		NC					M28			
		NC					N19			
		NC					P9			
		NC					P20			
		NC					R10			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC					T11			
		NC					U27			
		NC					Y26			
		NC					AC14			
		NC					AE14			
		NC					AF12			
		NC					AF21			
		NC					AF31			
		NC					AG19			
		NC					AH12			
		NC					AH28			
		NC					AN5			
		NC					AT4			
		NC					C2			
		NC					F5			
		NC					H31			
		NC					M11			
		NC					R29			
		NC					N20			
		NC					P10			
		NC					P22			
		NC					R12			
		NC					T12			
		NC					V26			
		NC					Y27			
		NC					AD13			
		NC					AE26			
		NC					AF13			
		NC					AF22			
		NC					AG12			
		NC					AG22			
		NC					AH13			
		NC					AJ11			
		NC					AN6			
		NC					AT36			
		NC					C38			
		NC					F6			
		NC					H34			
		NC					M12			
		NC					N12			
		NC					P12			
		NC					P24			
		NC					R13			
		NC					T13			
		NC					V27			
		NC					AD14			
		NC					AE27			
		NC					AF14			
		NC					AF24			
		NC					AG13			
		NC					AG23			
		NC					AH14			
		NC					AJ22			
		NC					AN34			
		NC					AT37			
		NC					D3			
		NC					F34			
		NC					H35			
		NC					M13			
		NC					N13			
		NC					P13			
		NC					P26			
		NC					R14			
		NC					T14			
		NC					W13			
		NC					AD26			
		NC					AE28			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC					AF15			
		NC					AF25			
		NC					AG14			
		NC					AG24			
		NC					AH15			
		NC					AJ25			
		NC					AN35			
		NC					AU2			
		NC					D4			
		NC					F35			
		NC					J5			
		NC					M22			
		NC					N14			
		NC					N24			
		NC					P14			
		NC					P27			
		NC					R26			
		NC					T26			
		NC					U14			
		NC					AD27			
		NC					AE30			
		NC					AF17			
		NC					AF26			
		NC					AG15			
		NC					AG25			
		NC					AH22			
		NC					AL5			
		NC					AP5			
		NC					AU38			
		NC					D36			
		NC					G5			
		NC					J6			
		NC					M23			
		NC					N15			
		NC					N25			
		NC					P15			
		NC					P28			
		NC					R27			
		NC					T27			
		NC					W26			
		NC					AE9			
		NC					AP6			
		NC					AV3			
		NC					D37			
		NC					G6			
		NC					J30			
		NC					M25			
		NC					N16			
		NC					N26			
		NC					P17			
		NC					P30			
		NC					R28			
		NC					T28			
		NC					V28			
		NC					E3			
		NC					G34			
		NC					J34			
Note to Pin-List:										

1) The wire bond and flip-chip packages will have different data rates for the high speed differential I/O channels. The following table shows the data rates as supported for each package.

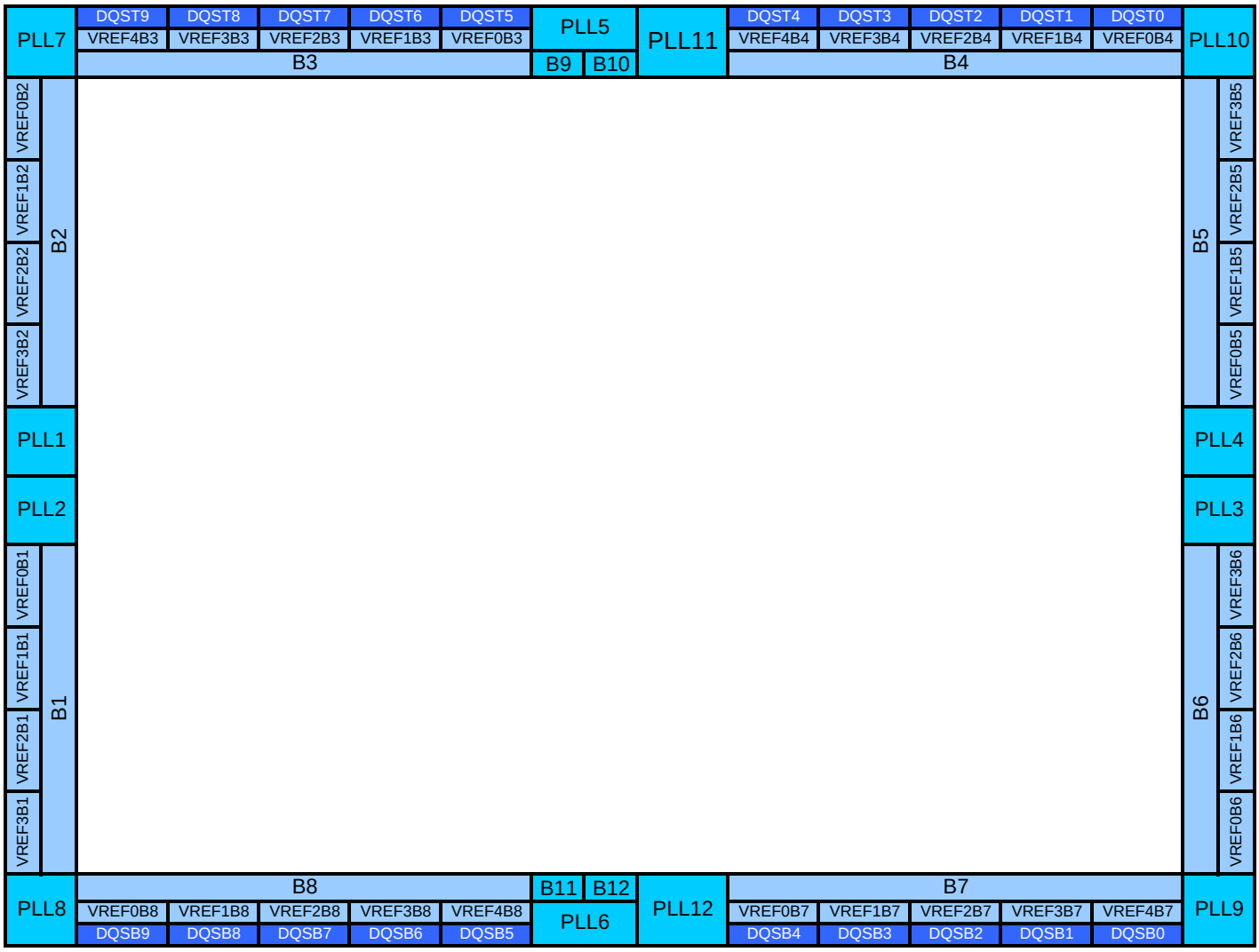
Package	Package Type	High Speed Differential I/O Channel Performance (DIFFIO Speed)		Units
		High	Low	
B956	flip chip	840	N/A	Mbps
F1020	flip chip	840	462	Mbps

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
F1508	flip chip	840	462	Mbps						

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..8]	Input	Input reference voltage for bank 1. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, designers should connect them to either VCC or Gnd.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1..12]	Power	Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1..12]	Ground	Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA.
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
		Clock and PLL Pins

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Dedicated fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins.
FPLL[10..7]CLKp	Input	Dedicated global clock inputs for fast PLLs (PLLs 7 through 10).
FPLL[10..7]CLKn	Input	Dedicated negative terminal associated with FPLL[10..7]CLKp pins.
CLK[15..0]p	Input	Dedicated global clock inputs 0 to 15.
CLK[15..0]n	I/O, Input	Optional negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6).
PLL6_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL5_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5).
PLL5_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
Optional/Dual-Purpose Pins		
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete.
DIFFIO_TX[0..115]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_RX[0..115]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
CLK6n, PLL12_OUT	I/O, Input (CLK6n), Output (PLL12_OUT)	This pin can be used as an I/O pin, CLK6n, as the PLL12_OUT pin. Only the EP1S40 and larger devices have this pin.
CLK13n, PLL11_OUT	I/O, Input (CLK13n), Output (PLL11_OUT)	This pin can be used as an I/O pin, CLK13n, or used as the PLL11_OUT pin. Only the EP1S40 and larger devices have this pin.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2=0, the RUnLU pin is a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.

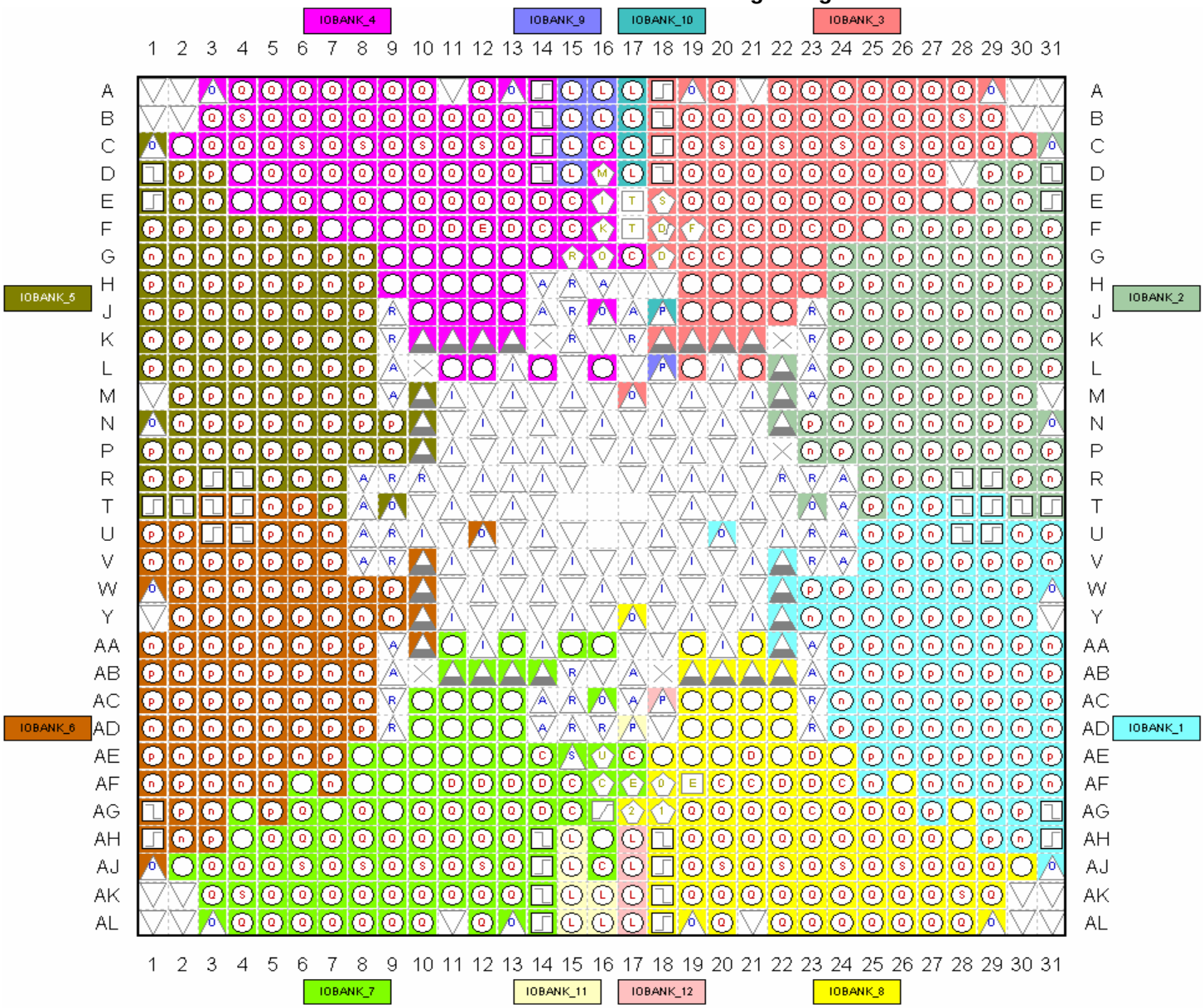


Notes:

1.This is a top view of the silicon die. For flip chip packages the die is mounted up-side down in the package.

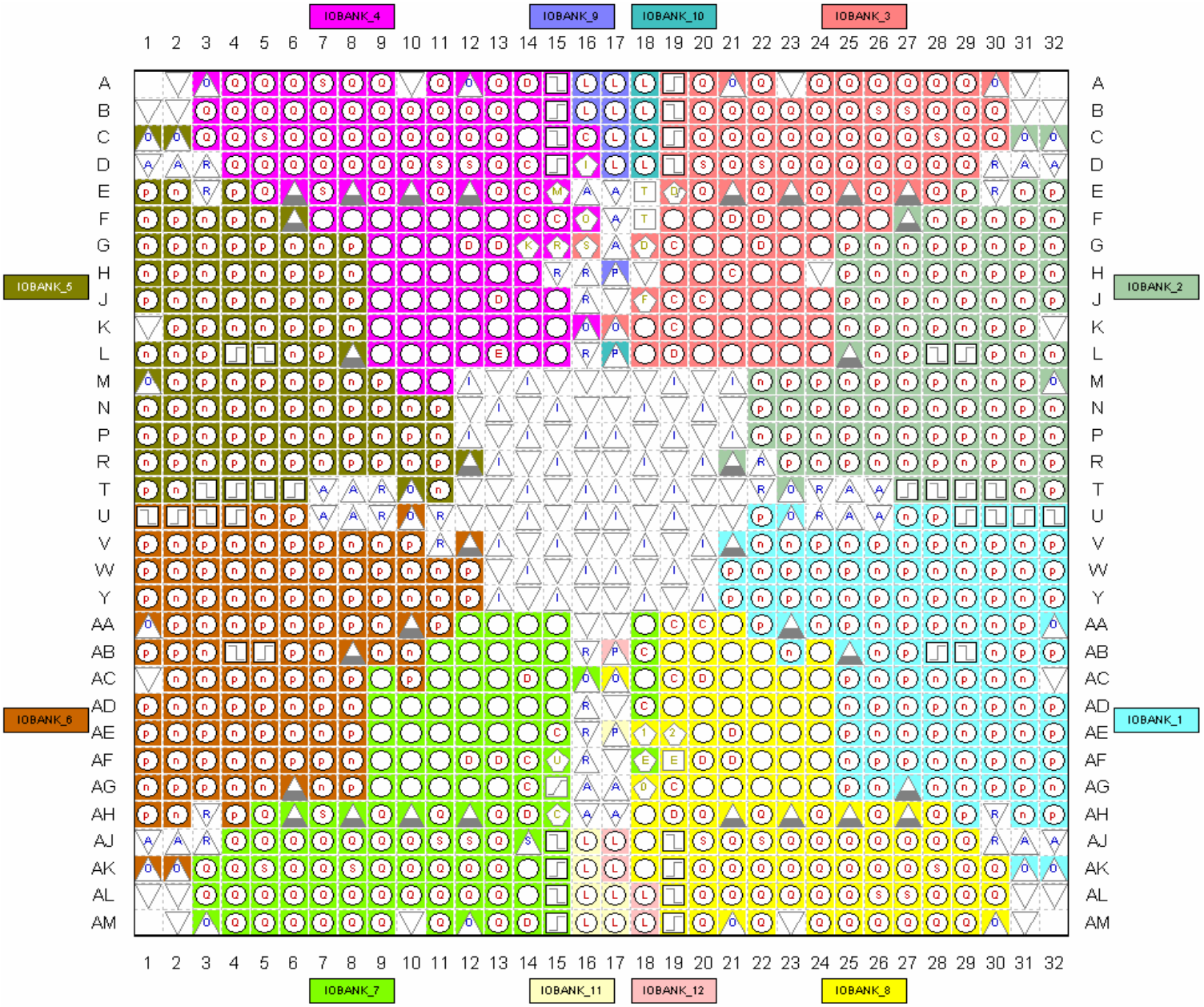
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

STRATIX EP1S60 B956 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

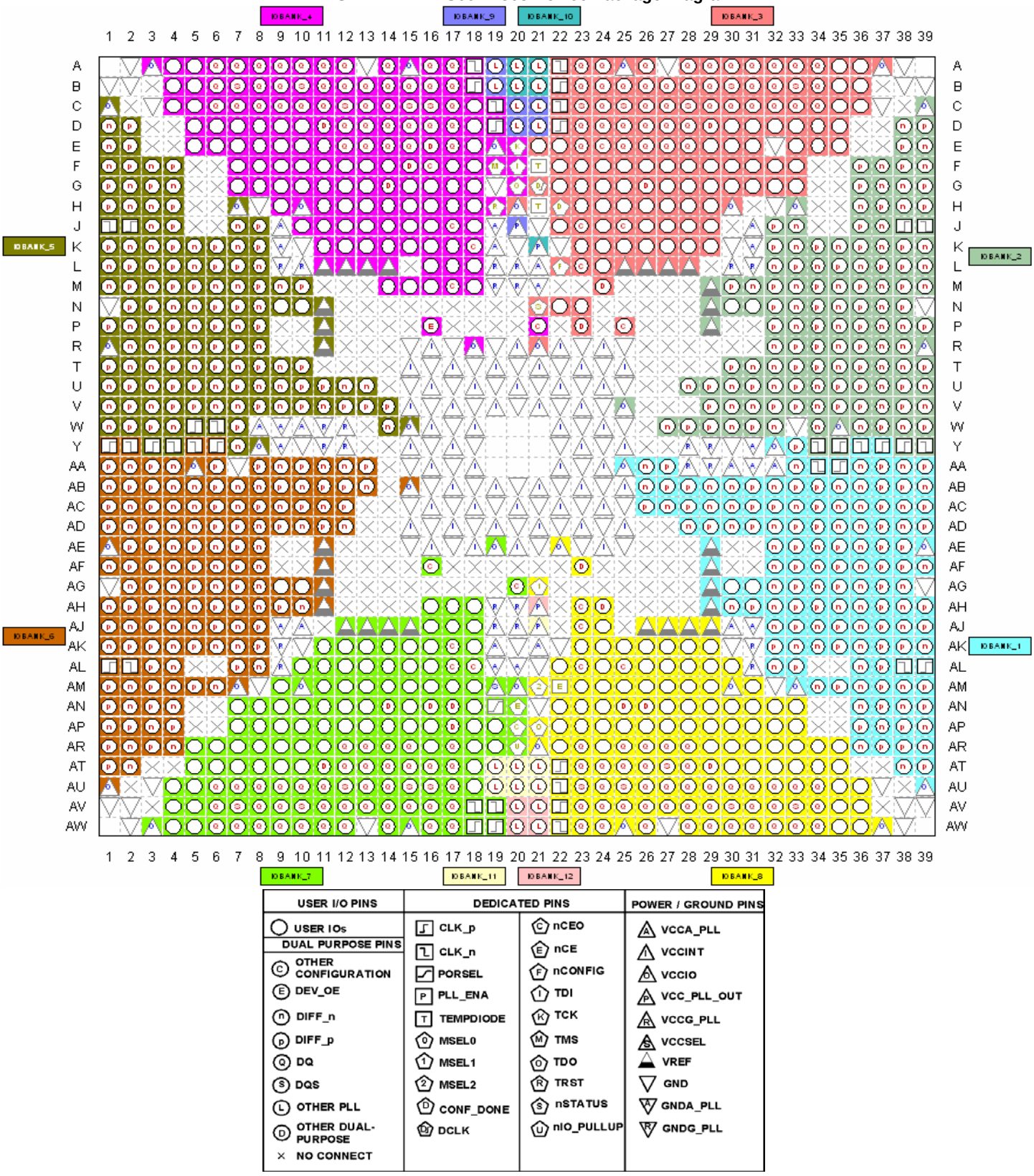
STRATIX EP1S60 F1020 Device Package Diagram



F1020 Package Diagram

× NO CONNECT			

STRATIX EP1S60 F1508 Device Package Diagram



F1508 Package Diagram

Clock Resources for High Speed Differential I/O (DIFFIO) Receiver and Transmitter channels. *Notes (5), (7)*										
Device	**Pin Count**	**Source FAST PLL**	**Rx Channels** ***Note (1)***		**Tx channels** ***Note (2)***		**Overlapped Rx Channels** ***Note (3)***		**Overlapped Tx Channels** ***Note (4)***	
			High *(6)*	**Low *(6)***	**High *(6)***	**Low *(6)***	**High *(6)***	**Low *(6)***	**High *(6)***	**Low *(6)***
EP1S60	956	PLL1	[30-49]	-	[38-49]	-	[38-49]	-	[38-49]	-
		PLL2	[10-29]	-	[10-19]	-	[10-19]	-	[10-19]	-
		PLL3	[86-105]	-	[96-105]	-	[96-105]	-	[96-105]	-
		PLL4	[66-85]	-	[66-77]	-	[66-77]	-	[66-77]	-
		PLL7	[38-49]	-	[38-57]	-	[38-49]	-	[38-49]	-
		PLL8	[10-19]	-	[0-19]	-	[10-19]	-	[10-19]	-
		PLL9	[96-105]	-	[96-115]	-	[96-105]	-	[96-105]	-
		PLL10	[66-77]	-	[58-77]	-	[66-77]	-	[66-77]	-
	1020	PLL1	[30-49]	-	[38-49]	[36-37]	[38-49]	-	[38-49]	-
		PLL2	[10-29]	-	[10-19]	[20-23]	[10-19]	-	[10-19]	-
		PLL3	[86-105]	-	[96-105]	[92-95]	[96-105]	-	[96-105]	-
		PLL4	[66-85]	-	[66-77]	[78-79]	[66-77]	-	[66-77]	-
		PLL7	[38-49]	[50-51]	[38-57]	-	[38-49]	-	[38-49]	-
		PLL8	[10-19]	[7-9]	[0-19]	-	[10-19]	-	[10-19]	-
		PLL9	[96-105]	[106-108]	[96-115]	-	[96-105]	-	[96-105]	-
		PLL10	[66-77]	[64-65]	[58-77]	-	[66-77]	-	[66-77]	-
	1508	PLL1	[30-49]	-	[38-49]	[30-37]	[38-49]	-	[38-49]	-
		PLL2	[10-29]	-	[10-19]	[20-29]	[10-19]	-	[10-19]	-
		PLL3	[86-105]	-	[96-105]	[86-95]	[96-105]	-	[96-105]	-
		PLL4	[66-85]	-	[66-77]	[78-85]	[66-77]	-	[66-77]	-
		PLL7	[38-49]	[50-57]	[38-57]	-	[38-49]	-	[38-49]	-
		PLL8	[10-19]	[0-9]	[0-19]	-	[10-19]	-	[10-19]	-
		PLL9	[96-105]	[106-115]	[96-115]	-	[96-105]	-	[96-105]	-
		PLL10	[66-77]	[58-65]	[58-77]	-	[66-77]	-	[66-77]	-

Notes:

1. These Rx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
2. These Tx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
3. These Rx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.
4. These Tx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.
5. Each range of channel numbers are shown in [ ] brackets.
6. Data channels designated as "high" speed support a maximum data rate of 840 Mbps for -5 and -6 speed grade devices and 624 Mbps for -7 speed grade devices. Data channels designated as "low" speed support a maximum data rate of 462 Mbps for all speed grades.
7. The high speed differential I/O (DIFFIO) channels span across two banks on both sides of the device. Each Fast PLL can normally only feed channels in one bank. However, the center PLLs can also clock the channels associated with the adjacent center PLL on the same side of the device through a mux that is shown in figures 5-16 and 5-17 in volume 2 of the Stratix Device Handbook. These channels are called "cross-bank" channels. When cross-bank channels are used only one center PLL on each side can be used.

Version Number	Date	Changes Made
3.4	2/4/2005	Revised package diagrams.
3.5	11/14/2005	Update all package diagram for EP1S60.
3.6	3/2/2006	Added CRC_ERROR pin in Pin List and Pin Definition