Pin Information For The Stratix™ EP1S30 Device, ver 3.6

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCA_PLL7				L23	D31			
		GND								
		GNDA_PLL7				M23	D32			
		VCCG_PLL7				J23	D30			
		GNDG_PLL7				K23	E30			
B2	VREF0B2	FPLL7CLKp				E31	L29			
B2	VREF0B2	FPLL7CLKn				D31	L28			
B2	VREF0B2	IO	DIFFIO_RX40p				E32			LOW
B2	VREF0B2	IO	DIFFIO_RX40n				E31			LOW
B2	VREF0B2	IO	DIFFIO_TX40p			K24	G25			HIGH
B2	VREF0B2	IO	DIFFIO_TX40n			J24	G26			HIGH
B2	VREF0B2	IO	DIFFIO_RX39p			F28	F29			HIGH
B2	VREF0B2	IO	DIFFIO_RX39n			G28	F30			HIGH
B2	VREF0B2	IO	DIFFIO_TX39p			K25	G28			HIGH
B2	VREF0B2	IO	DIFFIO_TX39n			J25	G27			HIGH
B2	VREF0B2	IO	DIFFIO_RX38p			J28	F31			HIGH
B2	VREF0B2	IO	DIFFIO_RX38n			H28	F32			HIGH
B2	VREF0B2	IO	DIFFIO_TX38p		F24	H24	H28			HIGH
B2	VREF0B2	IO	DIFFIO_TX38n		F23	G24	H27			HIGH
B2	VREF0B2	VREF0B2			E24	L22	F27			
B2	VREF0B2	IO	DIFFIO_RX37p			D29	G29			HIGH
B2	VREF0B2	IO	DIFFIO_RX37n			E29	G30			HIGH
B2	VREF0B2	IO	DIFFIO_TX37p		G23	H25	J27			HIGH
B2	VREF0B2	IO	DIFFIO_TX37n		G24	G25	J28			HIGH
B2	VREF0B2	IO	DIFFIO_RX36p		C27	F29	H30			HIGH
B2	VREF0B2	IO	DIFFIO_RX36n		C28	G29	H29			HIGH
B2	VREF0B2	IO	DIFFIO_TX36p		H24	K26	H25			HIGH
B2	VREF0B2	IO	DIFFIO_TX36n		H23	L26	H26			HIGH
B2	VREF0B2	IO	DIFFIO_RX35p		D27	H29	G31			HIGH
B2	VREF0B2	IO	DIFFIO_RX35n		D28	J29	G32			HIGH
B2	VREF0B2	IO	DIFFIO_TX35p		H22	J26	J25			HIGH

Pin Information For The Stratix™ EP1S30 Device, ver 3.6

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF0B2	IO	DIFFIO_TX35n		H21	H26	J26			HIGH
B2	VREF0B2	IO	DIFFIO_RX34p		E27	D30	H31			HIGH
B2	VREF0B2	IO	DIFFIO_RX34n		E28	E30	H32			HIGH
B2	VREF0B2	IO	DIFFIO_TX34p		J24	G26	K28			HIGH
B2	VREF0B2	IO	DIFFIO_TX34n		J23	F26	K27			HIGH
B2	VREF1B2	IO	DIFFIO_RX33p		F25	F30	J29			HIGH
B2	VREF1B2	IO	DIFFIO_RX33n		F26	G30	J30			HIGH
B2	VREF1B2	IO	DIFFIO_TX33p		K23	F27	K26			HIGH
B2	VREF1B2	IO	DIFFIO_TX33n		K24	G27	K25			HIGH
B2	VREF1B2	IO	DIFFIO_RX32p		F27	H30	K30			HIGH
B2	VREF1B2	IO	DIFFIO_RX32n		F28	J30	K29			HIGH
B2	VREF1B2	IO	DIFFIO_TX32p		J21	H27	L27			HIGH
B2	VREF1B2	IO	DIFFIO_TX32n		J22	J27	L26			HIGH
B2	VREF1B2	IO	DIFFIO_RX31p		G26	F31	J32			HIGH
B2	VREF1B2	IO	DIFFIO_RX31n		G25	G31	J31			HIGH
B2	VREF1B2	IO	DIFFIO_TX31p		K21	K27	M26			HIGH
B2	VREF1B2	IO	DIFFIO_TX31n		K22	L27	M27			HIGH
B2	VREF1B2	IO	DIFFIO_RX30p		G27	H31	K31			HIGH
B2	VREF1B2	IO	DIFFIO_RX30n		G28	J31	L32			HIGH
B2	VREF1B2	IO	DIFFIO_TX30p		L22	L24	M24			HIGH
B2	VREF1B2	IO	DIFFIO_TX30n		L21	M24	M25			HIGH
B2	VREF1B2	VREF1B2			K20	M22	L25			
B2	VREF1B2	IO	DIFFIO_RX29p/RUP2		H26	K28	M28			HIGH
B2	VREF1B2	IO	DIFFIO_RX29n/RDN2		H25	K29	M29			HIGH
B2	VREF1B2	IO	DIFFIO_TX29p		L23	L25	N24			HIGH
B2	VREF1B2	IO	DIFFIO_TX29n		L24	M25	N23			HIGH
B2	VREF1B2	IO	DIFFIO_RX28p		H27	M28	L30			HIGH
B2	VREF1B2	IO	DIFFIO_RX28n		H28	L28	L31			HIGH
B2	VREF1B2	IO	DIFFIO_TX28p		L20	P24	N27			HIGH
B2	VREF1B2	IO	DIFFIO_TX28n		L19	N24	N28			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF1B2	IO	DIFFIO_RX27p		J25	M29	M31			HIGH
B2	VREF1B2	IO	DIFFIO_RX27n		J26	L29	M30			HIGH
B2	VREF1B2	IO	DIFFIO_TX27p		M22	N25	P23			HIGH
B2	VREF1B2	IO	DIFFIO_TX27n		M21	P25	P24			HIGH
B2	VREF1B2	IO	DIFFIO_RX26p		J27	P28	N29			HIGH
B2	VREF1B2	IO	DIFFIO_RX26n		J28	N28	N30			HIGH
B2	VREF1B2	IO	DIFFIO_TX26p		M24	M26	N25			HIGH
B2	VREF1B2	IO	DIFFIO_TX26n		M23	N26	N26			HIGH
B2	VREF2B2	IO	DIFFIO_RX25p		K26	N29	N31			HIGH
B2	VREF2B2	IO	DIFFIO_RX25n		K25	P29	N32			HIGH
B2	VREF2B2	IO	DIFFIO_TX25p		M20	M27	P28			HIGH
B2	VREF2B2	IO	DIFFIO_TX25n		M19	N27	P27			HIGH
B2	VREF2B2	IO	DIFFIO_RX24p		K27	L30	P29			HIGH
B2	VREF2B2	IO	DIFFIO_RX24n		K28	K30	P30			HIGH
B2	VREF2B2	IO	DIFFIO_TX24p		N26	P27	R28			HIGH
B2	VREF2B2	IO	DIFFIO_TX24n		N25	R27	R27			HIGH
B2	VREF2B2	IO	DIFFIO_RX23p		L25	N30	P31			HIGH
B2	VREF2B2	IO	DIFFIO_RX23n		L26	M30	P32			HIGH
B2	VREF2B2	IO	DIFFIO_TX23p		N24	R26	P25			HIGH
B2	VREF2B2	IO	DIFFIO_TX23n		N23	P26	P26			HIGH
B2	VREF2B2	IO	DIFFIO_RX22p		L27	L31	R32			HIGH
B2	VREF2B2	IO	DIFFIO_RX22n		L28	K31	R31			HIGH
B2	VREF2B2	IO	DIFFIO_TX22p		N22	N23	R23			HIGH
B2	VREF2B2	IO	DIFFIO_TX22n		N21	P23	R24			HIGH
B2	VREF2B2	VREF2B2			P19	N22	R21			
B2	VREF2B2	IO	DIFFIO_RX21p		M25	R30	R30			HIGH
B2	VREF2B2	IO	DIFFIO_RX21n		M26	P30	R29			HIGH
B2	VREF2B2	IO	DIFFIO_TX21p		N20	T25	R25			HIGH
B2	VREF2B2	IO	DIFFIO_TX21n		N19	R25	R26			HIGH
B2	VREF2B2	IO	DIFFIO_RX20p		M27	P31	T32			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF2B2	IO	DIFFIO_RX20n		N28	R31	T31			HIGH
B2	VREF2B2	IO	DIFFIO_TX20p				M23			LOW
B2	VREF2B2	IO	DIFFIO_TX20n				M22			LOW
B2	VREF2B2	CLK0n			N27	R28	T30			
B2	VREF2B2	CLK0p			P27	R29	T29			
B2	VREF2B2	IO	CLK1n		P26	T30	T28			
B2	VREF2B2	CLK1p			P25	T31	T27			
		VCCA_PLL1			P23	R24	T25			
		GND								
		GNDA_PLL1			P24	T24	T26			
		VCCG_PLL1			P21	R22	R22			
		GNDG_PLL1			P22	R23	T22			
		VCCA_PLL2			R23	U24	U25			
		GND								
		GNDA_PLL2			R24	V24	U26			
		VCCG_PLL2			R21	U23	U24			
		GNDG_PLL2			R22	V23	T24			
B1	VREF0B1	CLK2p			R27	T29	U31			
B1	VREF0B1	CLK2n			T27	T28	U32			
B1	VREF0B1	CLK3p			R25	U29	U29			
B1	VREF0B1	IO	CLK3n		R26	U28	U30			
B1	VREF0B1	IO	DIFFIO_RX19p		T28	U31	U28			HIGH
B1	VREF0B1	IO	DIFFIO_RX19n		U27	V31	U27			HIGH
B1	VREF0B1	IO	DIFFIO_TX19p		T21	V25	V26			HIGH
B1	VREF0B1	IO	DIFFIO_TX19n		T22	U25	V25			HIGH
B1	VREF0B1	IO	DIFFIO_RX18p		U26	AB31	V32			HIGH
B1	VREF0B1	IO	DIFFIO_RX18n		U25	AA31	V31			HIGH
B1	VREF0B1	IO	DIFFIO_TX18p		T19	U26	V28			HIGH
B1	VREF0B1	IO	DIFFIO_TX18n		T20	T26	V27			HIGH
B1	VREF0B1	VREF0B1			R19	V22	V21			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF0B1	IO	DIFFIO_RX17p		V27	V30	V30			HIGH
B1	VREF0B1	IO	DIFFIO_RX17n		V28	U30	V29			HIGH
B1	VREF0B1	IO	DIFFIO_TX17p		T23	T27	W25			HIGH
B1	VREF0B1	IO	DIFFIO_TX17n		T24	U27	W26			HIGH
B1	VREF0B1	IO	DIFFIO_RX16p		V26	W30	W32			HIGH
B1	VREF0B1	IO	DIFFIO_RX16n		V25	Y30	W31			HIGH
B1	VREF0B1	IO	DIFFIO_TX16p		T26	V26	W27			HIGH
B1	VREF0B1	IO	DIFFIO_TX16n		T25	W26	W28			HIGH
B1	VREF0B1	IO	DIFFIO_RX15p		W28	AA30	W30			HIGH
B1	VREF0B1	IO	DIFFIO_RX15n		W27	AB30	W29			HIGH
B1	VREF0B1	IO	DIFFIO_TX15p		U19	W24	V24			HIGH
B1	VREF0B1	IO	DIFFIO_TX15n		U20	Y24	V23			HIGH
B1	VREF0B1	IO	DIFFIO_RX14p		W26	V29	Y32			HIGH
B1	VREF0B1	IO	DIFFIO_RX14n		W25	W29	Y31			HIGH
B1	VREF0B1	IO	DIFFIO_TX14p		U24	W25	Y26			HIGH
B1	VREF0B1	IO	DIFFIO_TX14n		U23	Y25	Y25			HIGH
B1	VREF1B1	IO	DIFFIO_RX13p		Y28	Y29	Y30			HIGH
B1	VREF1B1	IO	DIFFIO_RX13n		Y27	AA29	Y29			HIGH
B1	VREF1B1	IO	DIFFIO_TX13p		U21	Y26	Y28			HIGH
B1	VREF1B1	IO	DIFFIO_TX13n		U22	AA26	Y27			HIGH
B1	VREF1B1	IO	DIFFIO_RX12p		Y26	V28	AA31			HIGH
B1	VREF1B1	IO	DIFFIO_RX12n		Y25	W28	AA30			HIGH
B1	VREF1B1	IO	DIFFIO_TX12p		V19	W23	W23			HIGH
B1	VREF1B1	IO	DIFFIO_TX12n		V20	Y23	W24			HIGH
B1	VREF1B1	IO	DIFFIO_RX11p		AA28	Y28	AB31			HIGH
B1	VREF1B1	IO	DIFFIO_RX11n		AA27	AA28	AB30			HIGH
B1	VREF1B1	IO	DIFFIO_TX11p		V24	V27	Y23			HIGH
B1	VREF1B1	IO	DIFFIO_TX11n		V23	W27	Y24			HIGH
B1	VREF1B1	IO	DIFFIO_RX10p/RUP1		AA25	AB29	AA28			HIGH
B1	VREF1B1	IO	DIFFIO_RX10n/RDN1		AA26	AB28	AA29			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_TX10p		V22	Y27	AA25			HIGH
B1	VREF1B1	IO	DIFFIO_TX10n		V21	AA27	AA24			HIGH
B1	VREF1B1	VREF1B1			W20	W22	AA23			
B1	VREF1B1	IO	DIFFIO_RX9p		AB28	AC31	AB32			HIGH
B1	VREF1B1	IO	DIFFIO_RX9n		AB27	AD31	AC31			HIGH
B1	VREF1B1	IO	DIFFIO_TX9p		W23	AB27	AA27			HIGH
B1	VREF1B1	IO	DIFFIO_TX9n		W24	AC27	AA26			HIGH
B1	VREF1B1	IO	DIFFIO_RX8p		AB26	AE31	AD32			HIGH
B1	VREF1B1	IO	DIFFIO_RX8n		AB25	AF31	AD31			HIGH
B1	VREF1B1	IO	DIFFIO_TX8p		W21	AE27	AB27			HIGH
B1	VREF1B1	IO	DIFFIO_TX8n		W22	AD27	AB26			HIGH
B1	VREF1B1	IO	DIFFIO_RX7p		AC28	AC30	AC29			HIGH
B1	VREF1B1	IO	DIFFIO_RX7n		AC27	AD30	AC30			HIGH
B1	VREF1B1	IO	DIFFIO_TX7p		Y21	AG27	AC25			HIGH
B1	VREF1B1	IO	DIFFIO_TX7n		Y22	AF27	AC26			HIGH
B1	VREF1B1	IO	DIFFIO_RX6p		AD28	AF30	AD30			HIGH
B1	VREF1B1	IO	DIFFIO_RX6n		AD27	AE30	AD29			HIGH
B1	VREF1B1	IO	DIFFIO_TX6p		Y24	AB26	AC27			HIGH
B1	VREF1B1	IO	DIFFIO_TX6n		Y23	AC26	AC28			HIGH
B1	VREF2B1	IO	DIFFIO_RX5p		AE28	AG30	AE32			HIGH
B1	VREF2B1	IO	DIFFIO_RX5n		AE27	AH30	AE31			HIGH
B1	VREF2B1	IO	DIFFIO_TX5p		AA23	AD26	AD28			HIGH
B1	VREF2B1	IO	DIFFIO_TX5n		AA24	AE26	AD27			HIGH
B1	VREF2B1	IO	DIFFIO_RX4p		AF28	AC29	AE30			HIGH
B1	VREF2B1	IO	DIFFIO_RX4n		AF27	AD29	AE29			HIGH
B1	VREF2B1	IO	DIFFIO_TX4p		AA21	AA25	AD26			HIGH
B1	VREF2B1	IO	DIFFIO_TX4n		AA22	AB25	AD25			HIGH
B1	VREF2B1	IO	DIFFIO_RX3p			AE29	AF32			HIGH
B1	VREF2B1	IO	DIFFIO_RX3n			AF29	AF31			HIGH
B1	VREF2B1	IO	DIFFIO_TX3p		AB23	AD25	AE28			HIGH

Pin Information For The Stratix™ EP1S30 Device, ver 3.6

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF2B1	IO	DIFFIO_TX3n		AB24	AC25	AE27			HIGH
B1	VREF2B1	IO	DIFFIO_RX2p			AH29	AF30			HIGH
B1	VREF2B1	IO	DIFFIO_RX2n			AG29	AF29			HIGH
B1	VREF2B1	IO	DIFFIO_TX2p			AA24	AE25			HIGH
B1	VREF2B1	IO	DIFFIO_TX2n			AB24	AE26			HIGH
B1	VREF2B1	VREF2B1			AE26	Y22	AB25			
B1	VREF2B1	IO	DIFFIO_RX1p			AC28	AG31			HIGH
B1	VREF2B1	IO	DIFFIO_RX1n			AD28	AG32			HIGH
B1	VREF2B1	IO	DIFFIO_TX1p			AD24	AF27			HIGH
B1	VREF2B1	IO	DIFFIO_TX1n			AC24	AF28			HIGH
B1	VREF2B1	IO	DIFFIO_RX0p			AE28	AG30			HIGH
B1	VREF2B1	IO	DIFFIO_RX0n			AF28	AG29			HIGH
B1	VREF2B1	IO	DIFFIO_TX0p			AE25	AF26			HIGH
B1	VREF2B1	IO	DIFFIO_TX0n			AF25	AF25			HIGH
B1	VREF2B1	FPLL8CLKn				AG31	AB29			
B1	VREF2B1	FPLL8CLKp				AH31	AB28			
B1	VREF2B1	IO					AA22			
B1	VREF2B1	IO					AB23			
		VCCA_PLL8				AB23	AJ31			
		GND								
		GNDA_PLL8				AA23	AJ32			
		VCCG_PLL8				AD23	AJ30			
		GNDG_PLL8				AC23	AH30			
B8	VREF0B8	IO			AC24	AG28	AC24			
B8	VREF0B8	IO	DQ9B7		AG26	AK29	AH28	DQ3B15	DQ1B31	
B8	VREF0B8	IO			AC23	AJ30	AD24			
B8	VREF0B8	IO	DQ9B6		AH26	AJ29	AK30	DQ3B14	DQ1B30	
B8	VREF0B8	IO	DQ9B5		AG25	AJ28	AJ28	DQ3B13	DQ1B29	
B8	VREF0B8	IO	DQ9B4		AH25	AL28	AJ29	DQ3B12	DQ1B28	
B8	VREF0B8	IO			AB22	AA21	AB24			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF0B8	IO	DQ9B3		AF25	AH27	AK29	DQ3B11	DQ1B27	
B8	VREF0B8	IO				AF26	AE24			
B8	VREF0B8	IO	DQS9B		AF24	AK28	AK28			
B8	VREF0B8	IO	DQ9B2		AG24	AL27	AL30	DQ3B10	DQ1B26	
B8	VREF0B8	IO			AE25	AE24	AF24			
B8	VREF0B8	IO	DQ9B1		AE24	AJ27	AL29	DQ3B9	DQ1B25	
B8	VREF0B8	IO					AC23			
B8	VREF0B8	IO	DQ9B0		AH24	AK27	AM29	DQ3B8	DQ1B24	
B8	VREF0B8	IO			AD24	AC22	AE23			
B8	VREF0B8	IO				AD22	AG24			
B8	VREF0B8	IO	DQ8B7		AG23	AH26	AH26	DQ3B7	DQ1B23	
B8	VREF0B8	VREF0B8			AD22	AB22	AH27			
B8	VREF0B8	IO	DQ8B6		AD23	AG26	AJ27	DQ3B6	DQ1B22	
B8	VREF0B8	IO	DQ8B5		AF23	AK26	AL28	DQ3B5	DQ1B21	
B8	VREF0B8	IO			AB21	AH28	AD23			
B8	VREF0B8	IO	DQ8B4		AH23	AL26	AK27	DQ3B4	DQ1B20	
B8	VREF0B8	IO	DQ8B3		AE22	AH25	AJ26	DQ3B3	DQ1B19	
B8	VREF0B8	IO				AE22	AF23			
B8	VREF0B8	IO	DQS8B		AE23	AJ26	AL27	DQS3B		
B8	VREF0B8	IO	DQ8B2		AF22	AK25	AM27	DQ3B2	DQ1B18	
B8	VREF0B8	IO			AB20	AC21	AC22			
B8	VREF0B8	IO	DQ8B1		AH22	AJ25	AM28	DQ3B1	DQ1B17	
B8	VREF0B8	IO	DQ8B0		AG22	AL25	AK26	DQ3B0	DQ1B16	
B8	VREF0B8	IO					AG23			
B8	VREF1B8	IO			Y20	AD21	AB22			
B8	VREF1B8	IO	DQ7B7		AD21	AG24	AH24	DQ2B15	DQ1B15	
B8	VREF1B8	IO				AC20	AD22			
B8	VREF1B8	IO	DQ7B6		AE21	AH23	AJ24	DQ2B14	DQ1B14	
B8	VREF1B8	IO	DQ7B5		AG21	AK24	AJ25	DQ2B13	DQ1B13	
B8	VREF1B8	IO			AC22	AD20	AF22			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF1B8	IO	DQ7B4		AF21	AH24	AK25	DQ2B12	DQ1B12	
B8	VREF1B8	IO	DQ7B3		AE20	AJ23	AL25	DQ2B11	DQ1B11	
B8	VREF1B8	IO					AC21			
B8	VREF1B8	IO	DQS7B		AG20	AJ24	AL26		DQS1B	
B8	VREF1B8	IO	DQ7B2		AF20	AL24	AK24	DQ2B10	DQ1B10	
B8	VREF1B8	IO			AC20	AE20	AG22			
B8	VREF1B8	IO	DQ7B1		AH21	AK23	AM25	DQ2B9	DQ1B9	
B8	VREF1B8	IO					AB21			
B8	VREF1B8	IO	DQ7B0		AH20	AL23	AM26	DQ2B8	DQ1B8	
B8	VREF1B8	IO	DQ6B7		AE19	AG22	AJ23	DQ2B7	DQ1B7	
B8	VREF1B8	IO	FCLK3		AC21	AF23	AE21			
B8	VREF1B8	IO	FCLK2		AC19	AF22	AF21			
B8	VREF1B8	VREF1B8			AD20	AB21	AH25			
B8	VREF1B8	IO	DQ6B6		AD19	AH22	AL24	DQ2B6	DQ1B6	
B8	VREF1B8	IO	DQ6B5		AF19	AK22	AH22	DQ2B5	DQ1B5	
B8	VREF1B8	IO				AC19	AD21			
B8	VREF1B8	IO	DQ6B4		AG19	AG21	AM24	DQ2B4	DQ1B4	
B8	VREF1B8	IO		PGM2	AB19	AF24	AA20			
B8	VREF1B8	IO	DQ6B3		AH19	AH21	AK23	DQ2B3	DQ1B3	
B8	VREF1B8	IO				AA19	AA21			
B8	VREF1B8	IO	DQS6B		AF18	AJ22	AJ22	DQS2B		
B8	VREF1B8	IO	DQ6B2		AD18	AL22	AL23	DQ2B2	DQ1B2	
B8	VREF1B8	IO		CRC_ERROR	AA20	AE21	AF20			
B8	VREF1B8	IO	DQ6B1		AE18	AJ21	AK22	DQ2B1	DQ1B1	
B8	VREF1B8	IO	DQ6B0		AG18	AK21	AL22	DQ2B0	DQ1B0	
B8	VREF1B8	IO	RDN8		Y19	AE23	AC20			
B8	VREF1B8	IO	RUP8		W19	AG25	AH19			
B8	VREF1B8	IO	DQ5B7		AF17	AG20	AM22			
B8	VREF1B8	IO				AE19	AD20			
B8	VREF1B8	IO	DQ5B6		AG17	AH20	AJ21			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF1B8	IO	DQ5B5		AE17	AK20	AK21			
B8	VREF2B8	IO				AD19	AB20			
B8	VREF2B8	IO	DQ5B4		AD17	AL20	AL21			
B8	VREF2B8	IO		RDYnBSY	AA19	AG23	AA19			
B8	VREF2B8	IO	DQ5B3		AG16	AG19	AH20			
B8	VREF2B8	IO			AB18	AE18	AE20			
B8	VREF2B8	IO	DQS5B		AH16	AJ20	AJ20			
B8	VREF2B8	IO	DQ5B2		AD16	AH19	AK20			
B8	VREF2B8	IO		nCS	Y18	AF20	AC19			
B8	VREF2B8	IO	DQ5B1		AF16	AJ19	AL20			
B8	VREF2B8	IO	DQ5B0		AE16	AK19	AM20			
B8	VREF2B8	IO					AG21			
B8	VREF2B8	IO					AG20			
B8	VREF2B8	IO			V18		AB19			
B8	VREF2B8	IO			W18		AD19			
B8	VREF2B8	IO		CS	AA18	AF21	AG19			
B8	VREF2B8	IO					AJ18			
B8	VREF2B8	IO					AH18			
B8	VREF2B8	IO					AK18			
B8	VREF2B8	VREF2B8			AH18	AB20	AH23			
B8	VREF2B8	IO	CLK5n		Y17	AH18	AJ19			
B8	VREF2B8	CLK5p			AA17	AJ18	AK19			
B8	VREF2B8	IO	CLK4n		AB17	AK18	AL19			
B8	VREF2B8	CLK4p			AC17	AL18	AM19			
B8	VREF2B8	PLL_ENA		PLL_ENA	AC18	AF19	AF19			
B8	VREF2B8	MSEL0		MSEL0	AC16	AF18	AG18			
B8	VREF2B8	MSEL1		MSEL1	W17	AG18	AE18			
B8	VREF2B8	MSEL2		MSEL2	AB15	AG17	AE19			
B12	VREF2B8	IO	PLL6_OUT3n		Y16	AL17	AM18			
B12	VREF2B8	IO	PLL6_OUT3p		W16	AK17	AL18			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B12	VREF2B8	IO	PLL6_OUT2n		AG15	AJ17	AK17			
B12	VREF2B8	IO	PLL6_OUT2p		AF15	AH17	AJ17			
B11	VREF2B8	IO	PLL6_FBn		AA15	AJ15	AM17			
B11	VREF2B8	IO	PLL6_FBp		AA14	AH15	AL17			
B11	VREF2B8	IO	PLL6_OUT1n		W15	AL15	AK16			
B11	VREF2B8	IO	PLL6_OUT1p		W14	AK15	AJ16			
B11	VREF2B8	IO	PLL6_OUT0n		AE15	AL16	AM16			
B11	VREF2B8	IO	PLL6_OUT0p		AD15	AK16	AL16			
B12		VCC_PLL6_OUTB			AB16	AC18	AB17			
B11		VCC_PLL6_OUTA			AC14	AD17	AE17			
		VCCA_PLL6			AG14	AB17	AG17			
		GND								
		GNDA_PLL6			AF14	AC17	AH17			
		VCCG_PLL6			AA13	AD15	AD16			
		GNDG_PLL6			AB14	AD16	AB16			
B7	VREF0B7	CLK7p			W13	AJ14	AM15			
B7	VREF0B7	IO	CLK7n		Y13	AH14	AL15			
B7	VREF0B7	CLK6p			AD14	AL14	AK15			
B7	VREF0B7	IO	CLK6n		AE14	AK14	AJ15			
B7	VREF0B7	nCE		nCE	AB13	AF17	AF18			
B7	VREF0B7	nCEO		nCEO	AC13	AF16	AH15			
B7	VREF0B7	IO				AA16	AA18			
B7	VREF0B7	IO				AA15	AC18			
B7	VREF0B7	IO		PGM0	W12	AE17	AD18			
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	Y12	AE16	AF15			
B7	VREF0B7	VCCSEL		VCCSEL	AA12	AE15	AJ14			
B7	VREF0B7	PORSEL		PORSEL	AC12	AG16	AG15			
B7	VREF0B7	IO				AH16	AC15			
B7	VREF0B7	IO					AB15			
B7	VREF0B7	IO					AD15			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF0B7	IO					AE14			
B7	VREF0B7	IO					AL14			
B7	VREF0B7	IO				AE13	AK14			
B7	VREF0B7	VREF0B7			AD11	AB14	AH12			
B7	VREF0B7	IO		INIT_DONE	W11	AF15	AE15			
B7	VREF0B7	IO			V11	AC13	AA15			
B7	VREF0B7	IO	DQ4B7		AD13	AK13	AL13			
B7	VREF0B7	IO	DQ4B6		AE13	AG13	AM13			
B7	VREF0B7	IO		nRS	AC11	AE14	AB18			
B7	VREF0B7	IO	DQ4B5		AF13	AH13	AH13			
B7	VREF0B7	IO			Y11	AE12	AB14			
B7	VREF0B7	IO	DQ4B4		AD12	AJ13	AJ13			
B7	VREF0B7	IO	DQ4B3		AG13	AK12	AK13			
B7	VREF0B7	IO		RUnLU	W10	AJ16	AF14			
B7	VREF0B7	IO	DQS4B		AH13	AJ12	AJ12			
B7	VREF0B7	IO			AB12	AD13	AD14			
B7	VREF1B7	IO	DQ4B2		AE12	AL12	AK12			
B7	VREF1B7	IO	DQ4B1		AF12	AG12	AL12			
B7	VREF1B7	IO		PGM1	AA11	AG15	AG14			
B7	VREF1B7	IO	DQ4B0		AG12	AH12	AM11			
B7	VREF1B7	IO	RDN7		AC10	AG14	AC14			
B7	VREF1B7	IO	RUP7		AB11	AF13	AF13			
B7	VREF1B7	IO	DQ3B7		AG11	AL10	AL10	DQ1B15	DQ0B31	
B7	VREF1B7	IO				AE11	AA14			
B7	VREF1B7	IO	DQ3B6		AH11	AJ11	AK11	DQ1B14	DQ0B30	
B7	VREF1B7	IO	DQ3B5		AE11	AK11	AL11	DQ1B13	DQ0B29	
B7	VREF1B7	IO	DEV_CLRn		AC9	AF14	AH14			
B7	VREF1B7	IO	DQ3B4		AF11	AG11	AK10	DQ1B12	DQ0B28	
B7	VREF1B7	IO	DQ3B3		AE10	AH11	AM9	DQ1B11	DQ0B27	
B7	VREF1B7	IO				AD11	AB13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF1B7	IO	DQS3B		AG10	AJ10	AJ11	DQS1B		
B7	VREF1B7	IO			Y10	AD12	AD13			
B7	VREF1B7	IO	DQ3B2		AH10	AG10	AL9	DQ1B10	DQ0B26	
B7	VREF1B7	IO	DQ3B1		AF10	AH10	AJ10	DQ1B9	DQ0B25	
B7	VREF1B7	VREF1B7			AD9	AB13	AH10			
B7	VREF1B7	IO	DQ3B0		AD10	AK10	AH11	DQ1B8	DQ0B24	
B7	VREF1B7	IO				AA13	AC13			
B7	VREF1B7	IO			AA10	AF10	AG13			
B7	VREF1B7	IO	DQ2B7		AG9	AL8	AL8	DQ1B7	DQ0B23	
B7	VREF1B7	IO	FCLK5		AC8	AF12	AM14			
B7	VREF1B7	IO	FCLK4		AB10	AF11	AF12			
B7	VREF1B7	IO	DQ2B6		AF9	AK9	AJ9	DQ1B6	DQ0B22	
B7	VREF1B7	IO	DQ2B5		AE9	AL9	AK9	DQ1B5	DQ0B21	
B7	VREF1B7	IO			AB9	AC12	AE13			
B7	VREF1B7	IO	DQ2B4		AH8	AH8	AM8	DQ1B4	DQ0B20	
B7	VREF1B7	IO	DQ2B3		AH9	AK8	AH9	DQ1B3	DQ0B19	
B7	VREF1B7	IO				AG9	AG12			
B7	VREF2B7	IO	DQS2B		AE8	AJ8	AK8		DQS0B	
B7	VREF2B7	IO	DQ2B2		AD8	AG8	AM7	DQ1B2	DQ0B18	
B7	VREF2B7	IO			AA9	AC11	AD12			
B7	VREF2B7	IO	DQ2B1		AF8	AH9	AJ8	DQ1B1	DQ0B17	
B7	VREF2B7	IO	DQ2B0		AG8	AJ9	AL7	DQ1B0	DQ0B16	
B7	VREF2B7	IO				AE10	AE12			
B7	VREF2B7	IO			AB8	AE9	AC12			
B7	VREF2B7	IO	DQ1B7		AF6	AK7	AL6	DQ0B15	DQ0B15	
B7	VREF2B7	IO	DQ1B6		AG7	AL7	AM6	DQ0B14	DQ0B14	
B7	VREF2B7	IO			AC7	AD10	AG11			
B7	VREF2B7	IO	DQ1B5		AH7	AH6	AJ7	DQ0B13	DQ0B13	
B7	VREF2B7	IO	DQ1B4		AF7	AK6	AM5	DQ0B12	DQ0B12	
B7	VREF2B7	IO				AC10	AA12			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF2B7	IO	DQ1B3		AD6	AL6	AK7	DQ0B11	DQ0B11	
B7	VREF2B7	IO	DQS1B		AE7	AJ6	AH7	DQS0B		
B7	VREF2B7	IO			AD5	AG7	AE11			
B7	VREF2B7	IO	DQ1B2		AH6	AH7	AL5	DQ0B10	DQ0B10	
B7	VREF2B7	IO	DQ1B1		AG6	AJ7	AK6	DQ0B9	DQ0B9	
B7	VREF2B7	VREF2B7			AD7	AB12	AH8			
B7	VREF2B7	IO	DQ1B0		AE6	AG6	AJ6	DQ0B8	DQ0B8	
B7	VREF2B7	IO			Y9	AA11	AB11			
B7	VREF2B7	IO				AF8	AF10			
B7	VREF2B7	IO	DQ0B7		AF5	AL4	AL3	DQ0B7	DQ0B7	
B7	VREF2B7	IO			AE4	AF9	AG10			
B7	VREF2B7	IO	DQ0B6		AH5	AL5	AL4	DQ0B6	DQ0B6	
B7	VREF2B7	IO			AC6	AF6	AC9			
B7	VREF2B7	IO	DQ0B5		AF4	AJ4	AM4	DQ0B5	DQ0B5	
B7	VREF2B7	IO	DQ0B4		AG4	AK3	AJ4	DQ0B4	DQ0B4	
B7	VREF2B7	IO				AH4	AG9			
B7	VREF2B7	IO	DQ0B3		AG5	AK5	AJ5	DQ0B3	DQ0B3	
B7	VREF2B7	IO	DQS0B		AH3	AK4	AK5			
B7	VREF2B7	IO			AC5	AG4	AD9			
B7	VREF2B7	IO	DQ0B2		AG3	AH5	AH5	DQ0B2	DQ0B2	
B7	VREF2B7	IO	DQ0B1		AE5	AJ5	AK3	DQ0B1	DQ0B1	
B7	VREF2B7	IO			AB7	AJ2	AE9			
B7	VREF2B7	IO	DQ0B0		AH4	AJ3	AK4	DQ0B0	DQ0B0	
B7	VREF2B7	IO				AE8	AF9			
		GNDG_PLL9				AC9	AH3			
		VCCG_PLL9				AD9	AJ3			
		GNDA_PLL9				AA9	AJ1			
		GND								
		VCCA_PLL9				AB9	AJ2			
B6	VREF0B6	IO					AB9			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF0B6	IO					AC10			
B6	VREF0B6	FPLL9CLKp				AH1	AB5			
B6	VREF0B6	FPLL9CLKn				AG1	AB4			
B6	VREF0B6	IO	DIFFIO_TX81n			AC8	AF8			HIGH
B6	VREF0B6	IO	DIFFIO_TX81p			AD8	AF7			HIGH
B6	VREF0B6	IO	DIFFIO_RX81n			AF4	AG4			HIGH
B6	VREF0B6	IO	DIFFIO_RX81p			AE4	AG3			HIGH
B6	VREF0B6	IO	DIFFIO_TX80n			AF7	AF5			HIGH
B6	VREF0B6	IO	DIFFIO_TX80p			AE7	AF6			HIGH
B6	VREF0B6	IO	DIFFIO_RX80n			AD4	AG1			HIGH
B6	VREF0B6	IO	DIFFIO_RX80p			AC4	AG2			HIGH
B6	VREF0B6	VREF0B6			AE3	AA10	AG6			
B6	VREF0B6	IO	DIFFIO_TX79n			AB8	AE7			HIGH
B6	VREF0B6	IO	DIFFIO_TX79p			AA8	AE8			HIGH
B6	VREF0B6	IO	DIFFIO_RX79n			AG3	AF4			HIGH
B6	VREF0B6	IO	DIFFIO_RX79p			AH3	AF3			HIGH
B6	VREF0B6	IO	DIFFIO_TX78n		AB5	AC7	AD6			HIGH
B6	VREF0B6	IO	DIFFIO_TX78p		AB6	AD7	AD5			HIGH
B6	VREF0B6	IO	DIFFIO_RX78n			AF3	AF2			HIGH
B6	VREF0B6	IO	DIFFIO_RX78p			AE3	AF1			HIGH
B6	VREF0B6	IO	DIFFIO_TX77n		AA7	AB7	AE6			HIGH
B6	VREF0B6	IO	DIFFIO_TX77p		AA8	AA7	AE5			HIGH
B6	VREF0B6	IO	DIFFIO_RX77n		AF2	AD3	AE4			HIGH
B6	VREF0B6	IO	DIFFIO_RX77p		AF1	AC3	AE3			HIGH
B6	VREF0B6	IO	DIFFIO_TX76n		AA5	AE6	AD8			HIGH
B6	VREF0B6	IO	DIFFIO_TX76p		AA6	AD6	AD7			HIGH
B6	VREF0B6	IO	DIFFIO_RX76n		AE2	AH2	AE2			HIGH
B6	VREF0B6	IO	DIFFIO_RX76p		AE1	AG2	AE1			HIGH
B6	VREF1B6	IO	DIFFIO_TX75n		Y6	AC6	AC5			HIGH
B6	VREF1B6	IO	DIFFIO_TX75p		Y5	AB6	AC6			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF1B6	IO	DIFFIO_RX75n		AD2	AE2	AC3			HIGH
B6	VREF1B6	IO	DIFFIO_RX75p		AD1	AF2	AC4			HIGH
B6	VREF1B6	IO	DIFFIO_TX74n		Y7	AF5	AC7			HIGH
B6	VREF1B6	IO	DIFFIO_TX74p		Y8	AG5	AC8			HIGH
B6	VREF1B6	IO	DIFFIO_RX74n		AC2	AD2	AD3			HIGH
B6	VREF1B6	IO	DIFFIO_RX74p		AC1	AC2	AD4			HIGH
B6	VREF1B6	IO	DIFFIO_TX73n		W7	AD5	AB7			HIGH
B6	VREF1B6	IO	DIFFIO_TX73p		W8	AE5	AB6			HIGH
B6	VREF1B6	IO	DIFFIO_RX73n		AB4	AF1	AD2			HIGH
B6	VREF1B6	IO	DIFFIO_RX73p		AB3	AE1	AD1			HIGH
B6	VREF1B6	IO	DIFFIO_TX72n		W5	AC5	AA6			HIGH
B6	VREF1B6	IO	DIFFIO_TX72p		W6	AB5	AA7			HIGH
B6	VREF1B6	IO	DIFFIO_RX72n		AB2	AD1	AC2			HIGH
B6	VREF1B6	IO	DIFFIO_RX72p		AB1	AC1	AB1			HIGH
B6	VREF1B6	VREF1B6			W9	Y10	AB8			
B6	VREF1B6	IO	DIFFIO_TX71n		V8	AA6	AA9			HIGH
B6	VREF1B6	IO	DIFFIO_TX71p		V7	Y6	AA8			HIGH
B6	VREF1B6	IO	DIFFIO_RX71n/RDN6		AA3	AB4	AA4			HIGH
B6	VREF1B6	IO	DIFFIO_RX71p/RUP6		AA4	AB3	AA5			HIGH
B6	VREF1B6	IO	DIFFIO_TX70n		V6	Y9	Y5			HIGH
B6	VREF1B6	IO	DIFFIO_TX70p		V5	W9	Y6			HIGH
B6	VREF1B6	IO	DIFFIO_RX70n		AA2	Y4	AB3			HIGH
B6	VREF1B6	IO	DIFFIO_RX70p		AA1	AA4	AB2			HIGH
B6	VREF1B6	IO	DIFFIO_TX69n		V9	Y8	Y7			HIGH
B6	VREF1B6	IO	DIFFIO_TX69p		V10	W8	Y8			HIGH
B6	VREF1B6	IO	DIFFIO_RX69n		Y4	W4	AA3			HIGH
B6	VREF1B6	IO	DIFFIO_RX69p		Y3	V4	AA2			HIGH
B6	VREF1B6	IO	DIFFIO_TX68n		U7	AA5	W5			HIGH
B6	VREF1B6	IO	DIFFIO_TX68p		U8	Y5	W6			HIGH
B6	VREF1B6	IO	DIFFIO_RX68n		Y2	AA3	Y4			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF1B6	IO	DIFFIO_RX68p		Y1	Y3	Y3			HIGH
B6	VREF2B6	IO	DIFFIO_TX67n		U6	Y7	Y10			HIGH
B6	VREF2B6	IO	DIFFIO_TX67p		U5	W7	Y9			HIGH
B6	VREF2B6	IO	DIFFIO_RX67n		W4	W3	Y2			HIGH
B6	VREF2B6	IO	DIFFIO_RX67p		W3	V3	Y1			HIGH
B6	VREF2B6	IO	DIFFIO_TX66n		U9	U7	W10			HIGH
B6	VREF2B6	IO	DIFFIO_TX66p		U10	V7	W9			HIGH
B6	VREF2B6	IO	DIFFIO_RX66n		W2	AB2	W4			HIGH
B6	VREF2B6	IO	DIFFIO_RX66p		W1	AA2	W3			HIGH
B6	VREF2B6	IO	DIFFIO_TX65n		T6	W6	V9			HIGH
B6	VREF2B6	IO	DIFFIO_TX65p		T5	V6	V10			HIGH
B6	VREF2B6	IO	DIFFIO_RX65n		V4	Y2	W2			HIGH
B6	VREF2B6	IO	DIFFIO_RX65p		V3	W2	W1			HIGH
B6	VREF2B6	IO	DIFFIO_TX64n		T10	U6	V5			HIGH
B6	VREF2B6	IO	DIFFIO_TX64p		T9	T6	V6			HIGH
B6	VREF2B6	IO	DIFFIO_RX64n		V1	AA1	V4			HIGH
B6	VREF2B6	IO	DIFFIO_RX64p		V2	AB1	V3			HIGH
B6	VREF2B6	VREF2B6			R10	W10	AA10			
B6	VREF2B6	IO	DIFFIO_TX63n		T7	W5	V8			HIGH
B6	VREF2B6	IO	DIFFIO_TX63p		T8	V5	V7			HIGH
B6	VREF2B6	IO	DIFFIO_RX63n		U4	V2	V2			HIGH
B6	VREF2B6	IO	DIFFIO_RX63p		U3	U2	V1			HIGH
B6	VREF2B6	IO	DIFFIO_TX62n		T4	T5	W8			HIGH
B6	VREF2B6	IO	DIFFIO_TX62p		T3	U5	W7			HIGH
B6	VREF2B6	IO	DIFFIO_RX62n		U2	V1	U5			HIGH
B6	VREF2B6	IO	DIFFIO_RX62p		T1	U1	U6			HIGH
B6	VREF2B6	IO	CLK8n		R3	U4	U3			
B6	VREF2B6	CLK8p			R4	U3	U4			
B6	VREF2B6	CLK9n			T2	T3	U1			
B6	VREF2B6	CLK9p			R2	T4	U2			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GNDG_PLL3			R7	V9	U11			
		VCCG_PLL3			R8	U9	V11			
		GNDA_PLL3			R5	V8	U7			
		GND								
		VCCA_PLL3			R6	U8	U8			
		GNDG_PLL4			P7	R9	U9			
		VCCG_PLL4			P8	R10	T9			
		GNDA_PLL4			P5	R8	T7			
		GND								
		VCCA_PLL4			P6	T8	T8			
B5	VREF0B5	CLK10p			P4	T1	T6			
B5	VREF0B5	IO	CLK10n		P3	T2	T5			
B5	VREF0B5	CLK11p			P2	R3	T4			
B5	VREF0B5	CLK11n			N2	R4	T3			
B5	VREF0B5	IO	DIFFIO_TX61n				T11			LOW
B5	VREF0B5	IO	DIFFIO_TX61p				R11			LOW
B5	VREF0B5	IO	DIFFIO_RX61n		M2	R1	T2			HIGH
B5	VREF0B5	IO	DIFFIO_RX61p		N1	P1	T1			HIGH
B5	VREF0B5	IO	DIFFIO_TX60n		N10	R7	R7			HIGH
B5	VREF0B5	IO	DIFFIO_TX60p		N9	T7	R8			HIGH
B5	VREF0B5	IO	DIFFIO_RX60n		M3	P2	R1			HIGH
B5	VREF0B5	IO	DIFFIO_RX60p		M4	R2	R2			HIGH
B5	VREF0B5	VREF0B5			P10	P10	R12			
B5	VREF0B5	IO	DIFFIO_TX59n		N5	P8	P7			HIGH
B5	VREF0B5	IO	DIFFIO_TX59p		N6	N8	P8			HIGH
B5	VREF0B5	IO	DIFFIO_RX59n		L1	K1	R3			HIGH
B5	VREF0B5	IO	DIFFIO_RX59p		L2	L1	R4			HIGH
B5	VREF0B5	IO	DIFFIO_TX58n		N7	R6	R5			HIGH
B5	VREF0B5	IO	DIFFIO_TX58p		N8	P6	R6			HIGH
B5	VREF0B5	IO	DIFFIO_RX58n		L3	N2	P1			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF0B5	IO	DIFFIO_RX58p		L4	M2	P2			HIGH
B5	VREF0B5	IO	DIFFIO_TX57n		N4	P9	R10			HIGH
B5	VREF0B5	IO	DIFFIO_TX57p		N3	N9	R9			HIGH
B5	VREF0B5	IO	DIFFIO_RX57n		K1	L2	P3			HIGH
B5	VREF0B5	IO	DIFFIO_RX57p		K2	K2	P4			HIGH
B5	VREF0B5	IO	DIFFIO_TX56n		M10	P7	P6			HIGH
B5	VREF0B5	IO	DIFFIO_TX56p		M9	N7	P5			HIGH
B5	VREF0B5	IO	DIFFIO_RX56n		K4	P3	N1			HIGH
B5	VREF0B5	IO	DIFFIO_RX56p		K3	N3	N2			HIGH
B5	VREF1B5	IO	DIFFIO_TX55n		M6	N6	N7			HIGH
B5	VREF1B5	IO	DIFFIO_TX55p		M5	M6	N8			HIGH
B5	VREF1B5	IO	DIFFIO_RX55n		J1	L3	N3			HIGH
B5	VREF1B5	IO	DIFFIO_RX55p		J2	M3	N4			HIGH
B5	VREF1B5	IO	DIFFIO_TX54n		M8	R5	P9			HIGH
B5	VREF1B5	IO	DIFFIO_TX54p		M7	P5	P10			HIGH
B5	VREF1B5	IO	DIFFIO_RX54n		J3	P4	M2			HIGH
B5	VREF1B5	IO	DIFFIO_RX54p		J4	N4	M3			HIGH
B5	VREF1B5	IO	DIFFIO_TX53n		L10	M5	N5			HIGH
B5	VREF1B5	IO	DIFFIO_TX53p		L9	N5	N6			HIGH
B5	VREF1B5	IO	DIFFIO_RX53n		H1	M4	L2			HIGH
B5	VREF1B5	IO	DIFFIO_RX53p		H2	L4	L3			HIGH
B5	VREF1B5	IO	DIFFIO_TX52n		L5	M8	N10			HIGH
B5	VREF1B5	IO	DIFFIO_TX52p		L6	L8	N9			HIGH
B5	VREF1B5	IO	DIFFIO_RX52n/RDN5		H3	K3	M4			HIGH
B5	VREF1B5	IO	DIFFIO_RX52p/RUP5		H4	K4	M5			HIGH
B5	VREF1B5	VREF1B5			K9	N10	L8			
B5	VREF1B5	IO	DIFFIO_TX51n		L8	M7	M8			HIGH
B5	VREF1B5	IO	DIFFIO_TX51p		L7	L7	M9			HIGH
B5	VREF1B5	IO	DIFFIO_RX51n		G1	J1	L1			HIGH
B5	VREF1B5	IO	DIFFIO_RX51p		G2	H1	K2			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF1B5	IO	DIFFIO_TX50n		K7	L5	M6			HIGH
B5	VREF1B5	IO	DIFFIO_TX50p		K8	K5	M7			HIGH
B5	VREF1B5	IO	DIFFIO_RX50n		G4	G1	J2			HIGH
B5	VREF1B5	IO	DIFFIO_RX50p		G3	F1	J1			HIGH
B5	VREF1B5	IO	DIFFIO_TX49n		J7	H5	L6			HIGH
B5	VREF1B5	IO	DIFFIO_TX49p		J8	J5	L7			HIGH
B5	VREF1B5	IO	DIFFIO_RX49n		F1	H2	K4			HIGH
B5	VREF1B5	IO	DIFFIO_RX49p		F2	J2	K3			HIGH
B5	VREF1B5	IO	DIFFIO_TX48n		K5	F5	K5			HIGH
B5	VREF1B5	IO	DIFFIO_TX48p		K6	G5	K6			HIGH
B5	VREF1B5	IO	DIFFIO_RX48n		F3	G2	J3			HIGH
B5	VREF1B5	IO	DIFFIO_RX48p		F4	F2	J4			HIGH
B5	VREF2B5	IO	DIFFIO_TX47n		J6	L6	K8			HIGH
B5	VREF2B5	IO	DIFFIO_TX47p		J5	K6	K7			HIGH
B5	VREF2B5	IO	DIFFIO_RX47n		E1	J3	H1			HIGH
B5	VREF2B5	IO	DIFFIO_RX47p		E2	H3	H2			HIGH
B5	VREF2B5	IO	DIFFIO_TX46n		H8	J6	J5			HIGH
B5	VREF2B5	IO	DIFFIO_TX46p		H7	H6	J6			HIGH
B5	VREF2B5	IO	DIFFIO_RX46n		D1	G3	G1			HIGH
B5	VREF2B5	IO	DIFFIO_RX46p		D2	F3	G2			HIGH
B5	VREF2B5	IO	DIFFIO_TX45n		H6	G6	J7			HIGH
B5	VREF2B5	IO	DIFFIO_TX45p		H5	F6	J8			HIGH
B5	VREF2B5	IO	DIFFIO_RX45n		C1	J4	H3			HIGH
B5	VREF2B5	IO	DIFFIO_RX45p		C2	H4	H4			HIGH
B5	VREF2B5	IO	DIFFIO_TX44n		G5	K8	H5			HIGH
B5	VREF2B5	IO	DIFFIO_TX44p		G6	J8	H6			HIGH
B5	VREF2B5	IO	DIFFIO_RX44n			G4	F1			HIGH
B5	VREF2B5	IO	DIFFIO_RX44p			F4	F2			HIGH
B5	VREF2B5	VREF2B5			E5	M10	F6			
B5	VREF2B5	IO	DIFFIO_TX43n		F6	K7	H8			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF2B5	IO	DIFFIO_TX43p		F5	J7	H7			HIGH
B5	VREF2B5	IO	DIFFIO_RX43n			E2	G3			HIGH
B5	VREF2B5	IO	DIFFIO_RX43p			D2	G4			HIGH
B5	VREF2B5	IO	DIFFIO_TX42n			H7	G6			HIGH
B5	VREF2B5	IO	DIFFIO_TX42p			G7	G5			HIGH
B5	VREF2B5	IO	DIFFIO_RX42n			E3	F3			HIGH
B5	VREF2B5	IO	DIFFIO_RX42p			D3	F4			HIGH
B5	VREF2B5	IO	DIFFIO_TX41n			G8	G7			HIGH
B5	VREF2B5	IO	DIFFIO_TX41p			H8	G8			HIGH
B5	VREF2B5	IO	DIFFIO_RX41n				E2			LOW
B5	VREF2B5	IO	DIFFIO_RX41p				E1			LOW
B5	VREF2B5	FPLL10CLKn				D1	L5			
B5	VREF2B5	FPLL10CLKp				E1	L4			
		GNDG_PLL10				K9	E3			
		VCCG_PLL10				J9	D3			
		GNDA_PLL10				M9	D1			
		GND								
		VCCA_PLL10				L9	D2			
B4	VREF0B4	IO				F7	F7			
B4	VREF0B4	IO	DQ0T0		A4	C4	D5	DQ0T0	DQ0T0	
B4	VREF0B4	IO			G7	E4	K9			
B4	VREF0B4	IO	DQ0T1		A3	C5	C3	DQ0T1	DQ0T1	
B4	VREF0B4	IO	DQ0T2		B3	D5	E5	DQ0T2	DQ0T2	
B4	VREF0B4	IO	DQS0T		D5	B4	C5			
B4	VREF0B4	IO			F7	H9	H9			
B4	VREF0B4	IO	DQ0T3		B5	B5	C4	DQ0T3	DQ0T3	
B4	VREF0B4	IO				E5	J9			
B4	VREF0B4	IO	DQ0T4		B4	B3	D4	DQ0T4	DQ0T4	
B4	VREF0B4	IO	DQ0T5		C4	C3	A4	DQ0T5	DQ0T5	
B4	VREF0B4	IO			G8	C2	L9			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF0B4	IO	DQ0T6		A5	A5	B4	DQ0T6	DQ0T6	
B4	VREF0B4	IO			F8	F8	G9			
B4	VREF0B4	IO	DQ0T7		C5	A4	B3	DQ0T7	DQ0T7	
B4	VREF0B4	IO				E7	F8			
B4	VREF0B4	IO			J9	L11	M10			
B4	VREF0B4	IO	DQ1T0		E6	E6	D6	DQ0T8	DQ0T8	
B4	VREF0B4	VREF0B4			E7	K10	E6			
B4	VREF0B4	IO	DQ1T1		A6	C7	C6	DQ0T9	DQ0T9	
B4	VREF0B4	IO	DQ1T2		B7	D7	B5	DQ0T10	DQ0T10	
B4	VREF0B4	IO				J10	J11			
B4	VREF0B4	IO	DQS1T		B6	C6	E7	DQS0T		
B4	VREF0B4	IO			H9	D4	K11			
B4	VREF0B4	IO	DQ1T3		D6	A6	C7	DQ0T11	DQ0T11	
B4	VREF0B4	IO	DQ1T4		A7	B6	A5	DQ0T12	DQ0T12	
B4	VREF0B4	IO				J11	G10			
B4	VREF0B4	IO	DQ1T5		D7	D6	D7	DQ0T13	DQ0T13	
B4	VREF0B4	IO			G9	G9	F9			
B4	VREF0B4	IO	DQ1T6		C6	A7	A6	DQ0T14	DQ0T14	
B4	VREF0B4	IO	DQ1T7		C7	B7	B6	DQ0T15	DQ0T15	
B4	VREF0B4	IO			F9	G10	F10			
B4	VREF0B4	IO				F9	H11			
B4	VREF0B4	IO	DQ2T0		D8	B8	B7	DQ1T0	DQ0T16	
B4	VREF0B4	IO	DQ2T1		C8	D9	D8	DQ1T1	DQ0T17	
B4	VREF0B4	IO			H10	H10	L11			
B4	VREF0B4	IO	DQ2T2		E8	E8	B8	DQ1T2	DQ0T18	
B4	VREF1B4	IO	DQS2T		C9	C8	A7		DQS0T	
B4	VREF1B4	IO				H11	F12			
B4	VREF1B4	IO	DQ2T3		D9	C9	E9	DQ1T3	DQ0T19	
B4	VREF1B4	IO	DQ2T4		B9	D8	A8	DQ1T4	DQ0T20	
B4	VREF1B4	IO	DQ2T5		B8	A9	C9	DQ1T5	DQ0T21	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF1B4	IO	DQ2T6		A8	B9	C8	DQ1T6	DQ0T22	
B4	VREF1B4	IO	FCLK6		G10	F10	G12			
B4	VREF1B4	IO	FCLK7		F10	F11	A14			
B4	VREF1B4	IO	DQ2T7		A9	A8	D9	DQ1T7	DQ0T23	
B4	VREF1B4	IO				J12	J12			
B4	VREF1B4	IO			J10	L12	K12			
B4	VREF1B4	IO	DQ3T0		E10	B10	E11	DQ1T8	DQ0T24	
B4	VREF1B4	VREF1B4			E9	K11	E8			
B4	VREF1B4	IO	DQ3T1		A10	D10	B9	DQ1T9	DQ0T25	
B4	VREF1B4	IO			F11	H12	H13			
B4	VREF1B4	IO	DQ3T2		C10	E10	D10	DQ1T10	DQ0T26	
B4	VREF1B4	IO			K10	E9	H12			
B4	VREF1B4	IO	DQS3T		D10	C10	D11	DQS1T		
B4	VREF1B4	IO	DQ3T3		B10	D11	C10	DQ1T11	DQ0T27	
B4	VREF1B4	IO				G11	F13			
B4	VREF1B4	IO	DQ3T4		A11	E11	A9	DQ1T12	DQ0T28	
B4	VREF1B4	IO	DQ3T5		C11	B11	B11	DQ1T13	DQ0T29	
B4	VREF1B4	IO	DEV_OE		J11	F12	L13			
B4	VREF1B4	IO	DQ3T6		D11	C11	C11	DQ1T14	DQ0T30	
B4	VREF1B4	IO	DQ3T7		B11	A10	B10	DQ1T15	DQ0T31	
B4	VREF1B4	IO	RUP4		H11	F13	G13			
B4	VREF1B4	IO	RDN4		G11	E14	J13			
B4	VREF1B4	IO	DQ4T0		B12	D12	A11			
B4	VREF1B4	IO		nWS	K11	F14	D14			
B4	VREF1B4	IO	DQ4T1		C12	E12	B12			
B4	VREF1B4	IO	DQ4T2		D12	A12	C12			
B4	VREF2B4	IO			G12	G12	H14			
B4	VREF2B4	IO	DQS4T		A13	C12	D12			
B4	VREF2B4	IO		DATA0	H12	E15	E14			
B4	VREF2B4	IO	DQ4T3		B13	B12	C13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF2B4	IO	DQ4T4		E12	C13	D13			
B4	VREF2B4	IO			L11	J13	K13			
B4	VREF2B4	IO	DQ4T5		C13	D13	E13			
B4	VREF2B4	IO		DATA1	F12	C16	F14			
B4	VREF2B4	IO	DQ4T6		D13	E13	A13			
B4	VREF2B4	IO	DQ4T7		E13	B13	B13			
B4	VREF2B4	IO			M11	L14	L12			
B4	VREF2B4	IO		DATA2	J12	F15	F15			
B4	VREF2B4	VREF2B4			E11	K12	E10			
B4	VREF2B4	IO				G13	C14			
B4	VREF2B4	IO					B14			
B4	VREF2B4	IO					K14			
B4	VREF2B4	IO					J14			
B4	VREF2B4	IO					L14			
B4	VREF2B4	IO				H13	K15			
B4	VREF2B4	TMS		TMS	F13	D16	E15			
B4	VREF2B4	TRST		TRST	L12	G15	G15			
B4	VREF2B4	TCK		TCK	K12	F16	G14			
B4	VREF2B4	IO		DATA3	M12	G17	C16			
B4	VREF2B4	IO				G14	J15			
B4	VREF2B4	IO				L16	L15			
B4	VREF2B4	TDI		TDI	G13	E16	D16			
B4	VREF2B4	TDO		TDO	H13	G16	F16			
B4	VREF2B4	IO	CLK12n		J13	B14	A15			
B4	VREF2B4	CLK12p			K13	A14	B15			
B4	VREF2B4	IO	CLK13n		L13	D14	C15			
B4	VREF2B4	CLK13p			M13	C14	D15			
		TEMPDIODEp			B14	E17	E18			
		TEMPDIODEn			C14	F17	F18			
		VCCA_PLL5			F14	J17	G17			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND								
		GNDA_PLL5			G14	H16	F17			
		VCCG_PLL5			D14	K15	J16			
		GNDG_PLL5			E14	K17	L16			
B9		VCC_PLL5_OUTA			F15	L18	H17			
B10		VCC_PLL5_OUTB			G16	J18	L17			
B9	VREF0B3	IO	PLL5_OUT0p		E15	B16	B16			
B9	VREF0B3	IO	PLL5_OUT0n		D15	A16	A16			
B9	VREF0B3	IO	PLL5_OUT1p		K14	B15	B17			
B9	VREF0B3	IO	PLL5_OUT1n		K15	A15	A17			
B9	VREF0B3	IO	PLL5_FBp		H14	D15	D17			
B9	VREF0B3	IO	PLL5_FBn		H15	C15	C17			
B10	VREF0B3	IO	PLL5_OUT2p		C15	D17	B18			
B10	VREF0B3	IO	PLL5_OUT2n		B15	C17	A18			
B10	VREF0B3	IO	PLL5_OUT3p		K16	B17	D18			
B10	VREF0B3	IO	PLL5_OUT3n		J16	A17	C18			
B3	VREF0B3	nSTATUS		nSTATUS	M16	E18	G16			
B3	VREF0B3	nCONFIG		nCONFIG	L16	F19	J18			
B3	VREF0B3	DCLK		DCLK	F16	F18	E19			
B3	VREF0B3	CONF_DONE		CONF_DONE	G17	G18	G18			
B3	VREF0B3	CLK14p			K17	A18	A19			
B3	VREF0B3	IO	CLK14n		J17	B18	B19			
B3	VREF0B3	CLK15p			M17	C18	C19			
B3	VREF0B3	IO	CLK15n		L17	D18	D19			
B3	VREF0B3	VREF0B3			E18	K18	E21			
B3	VREF0B3	IO					K18			
B3	VREF0B3	IO					F19			
B3	VREF0B3	IO		DATA4	H17	G19	G19			
B3	VREF0B3	IO			L18	H20	L18			
B3	VREF0B3	IO			M18	J19	L21			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF0B3	IO					L20			
B3	VREF0B3	IO					F20			
B3	VREF0B3	IO			F17	H19	H19			
B3	VREF0B3	IO	DQ5T0		D16	B19	A20			
B3	VREF0B3	IO	DQ5T1		C16	C19	B20			
B3	VREF0B3	IO		DATA5	K18	F20	J19			
B3	VREF0B3	IO	DQ5T2		E16	D19	C20			
B3	VREF0B3	IO	DQS5T		A16	C20	D20			
B3	VREF0B3	IO				G22	H20			
B3	VREF0B3	IO	DQ5T3		B16	E19	E20			
B3	VREF0B3	IO		DATA6	H18	F21	K19			
B3	VREF0B3	IO	DQ5T4		E17	A20	B21			
B3	VREF0B3	IO	DQ5T5		D17	B20	C21			
B3	VREF1B3	IO			F18	G21	G20			
B3	VREF1B3	IO	DQ5T6		B17	D20	D21			
B3	VREF1B3	IO					G21			
B3	VREF1B3	IO	DQ5T7		C17	E20	A22			
B3	VREF1B3	IO	RUP3		J18	F22	F21			
B3	VREF1B3	IO	RDN3		K19	F24	L19			
B3	VREF1B3	IO	DQ6T0		A18	B21	B22	DQ2T0	DQ1T0	
B3	VREF1B3	IO	DQ6T1		C18	C21	C22	DQ2T1	DQ1T1	
B3	VREF1B3	IO		DATA7	G18	G20	J20			
B3	VREF1B3	IO	DQ6T2		D18	A22	B23	DQ2T2	DQ1T2	
B3	VREF1B3	IO	DQS6T		B18	C22	D22	DQS2T		
B3	VREF1B3	IO				L19	L22			
B3	VREF1B3	IO	DQ6T3		A19	D21	C23	DQ2T3	DQ1T3	
B3	VREF1B3	IO		CLKUSR	J19	F23	H21			
B3	VREF1B3	IO	DQ6T4		B19	E21	A24	DQ2T4	DQ1T4	
B3	VREF1B3	IO				J20	K20			
B3	VREF1B3	IO	DQ6T5		C19	B22	E22	DQ2T5	DQ1T5	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF1B3	IO	DQ6T6		E19	D22	B24	DQ2T6	DQ1T6	
B3	VREF1B3	VREF1B3			E20	K19	E23			
B3	VREF1B3	IO	FCLK0		F19	E23	F22			
B3	VREF1B3	IO	FCLK1		G19	E25	G22			
B3	VREF1B3	IO	DQ6T7		D19	E22	D23	DQ2T7	DQ1T7	
B3	VREF1B3	IO			H19	H21	J21			
B3	VREF1B3	IO					K21			
B3	VREF1B3	IO	DQ7T0		B20	A23	D24	DQ2T8	DQ1T8	
B3	VREF1B3	IO	DQ7T1		A20	B23	A25	DQ2T9	DQ1T9	
B3	VREF1B3	IO	DQ7T2		C20	A24	C24	DQ2T10	DQ1T10	
B3	VREF1B3	IO					F23			
B3	VREF1B3	IO	DQS7T		D20	C24	B26		DQS1T	
B3	VREF1B3	IO	DQ7T3		A21	C23	B25	DQ2T11	DQ1T11	
B3	VREF1B3	IO			J20	H22	L23			
B3	VREF1B3	IO	DQ7T4		B21	D24	C25	DQ2T12	DQ1T12	
B3	VREF1B3	IO	DQ7T5		C21	B24	D25	DQ2T13	DQ1T13	
B3	VREF1B3	IO				J21	H22			
B3	VREF1B3	IO	DQ7T6		D21	D23	A26	DQ2T14	DQ1T14	
B3	VREF1B3	IO	DQ7T7		E21	E24	E24	DQ2T15	DQ1T15	
B3	VREF1B3	IO			H20	G23	K22			
		GND			G20	D28	H24			
B3	VREF2B3	IO					G23			
B3	VREF2B3	IO	DQ8T0		B22	A25	C26	DQ3T0	DQ1T16	
B3	VREF2B3	IO	DQ8T1		A22	C25	A28	DQ3T1	DQ1T17	
B3	VREF2B3	IO				F25	J22			
B3	VREF2B3	IO	DQ8T2		C22	B25	A27	DQ3T2	DQ1T18	
B3	VREF2B3	IO	DQS8T		D23	C26	B27	DQS3T		
B3	VREF2B3	IO					F24			
B3	VREF2B3	IO	DQ8T3		D22	D25	D26	DQ3T3	DQ1T19	
B3	VREF2B3	IO	DQ8T4		A23	A26	C27	DQ3T4	DQ1T20	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF2B3	IO				E27	K23			
B3	VREF2B3	IO	DQ8T5		C23	B26	B28	DQ3T5	DQ1T21	
B3	VREF2B3	IO	DQ8T6		E23	E26	D27	DQ3T6	DQ1T22	
B3	VREF2B3	VREF2B3			E22	K20	E25			
B3	VREF2B3	IO	DQ8T7		B23	D26	E26	DQ3T7	DQ1T23	
B3	VREF2B3	IO			F20	J22	H23			
B3	VREF2B3	IO					J23			
B3	VREF2B3	IO	DQ9T0		A24	B27	A29	DQ3T8	DQ1T24	
B3	VREF2B3	IO					L24			
B3	VREF2B3	IO	DQ9T1		C25	C27	B29	DQ3T9	DQ1T25	
B3	VREF2B3	IO			F21	H23	G24			
B3	VREF2B3	IO	DQ9T2		A25	A27	B30	DQ3T10	DQ1T26	
B3	VREF2B3	IO	DQS9T		C24	B28	C28			
B3	VREF2B3	IO			G21	C30	F25			
B3	VREF2B3	IO	DQ9T3		D24	D27	C29	DQ3T11	DQ1T27	
B3	VREF2B3	IO			G22	L21	J24			
B3	VREF2B3	IO	DQ9T4		B24	A28	D29	DQ3T12	DQ1T28	
B3	VREF2B3	IO	DQ9T5		B25	C28	D28	DQ3T13	DQ1T29	
B3	VREF2B3	IO	DQ9T6		A26	C29	C30	DQ3T14	DQ1T30	
B3	VREF2B3	IO			F22	E28	F26			
B3	VREF2B3	IO	DQ9T7		B26	B29	E28	DQ3T15	DQ1T31	
B3	VREF2B3	IO					K24			
		VCCIO2			B28	C31	C31			
		VCCIO2			M28	N31	C32			
		VCCIO2			P20	T23	M32			
		VCCIO2					T23			
		VCCIO1			R20	U20	AA32			
		VCCIO1			U28	W31	AK31			
		VCCIO1			AG28	AJ31	AK32			
		VCCIO1					U23			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCIO8			Y15	AL29	AC17			
		VCCIO8			AH17	AL19	AM21			
		VCCIO8			AH27	Y17	AM30			
		VCCIO7			Y14	AC16	AC16			
		VCCIO7			AH2	AL13	AM12			
		VCCIO7			AH12	AL3	AM3			
		VCCIO6			R9	AJ1	AA1			
		VCCIO6			U1	W1	AK1			
		VCCIO6			AG1	U12	AK2			
		VCCIO6					U10			
		VCCIO5			B1	T9	C1			
		VCCIO5			M1	N1	C2			
		VCCIO5			P9	C1	M1			
		VCCIO5					T10			
		VCCIO4			A2	A3	A12			
		VCCIO4			A12	A13	A3			
		VCCIO4			J14	J16	K16			
		VCCIO3			A17	M17	A21			
		VCCIO3			A27	A19	A30			
		VCCIO3			J15	A29	K17			
		VCCINT			M14	AA12	M12			
		VCCINT			N11	AA14	M14			
		VCCINT			N13	AA20	M19			
		VCCINT			N15	L13	M21			
		VCCINT			N17	L20	N13			
		VCCINT			P12	M11	N15			
		VCCINT			P14	M13	N18			
		VCCINT			P16	M15	N20			
		VCCINT			R13	M19	P12			
		VCCINT			R15	M21	P14			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT			R17	N12	P16			
		VCCINT			T12	N14	P17			
		VCCINT			T14	N16	P19			
		VCCINT			T16	N18	P21			
		VCCINT			T18	N20	R13			
		VCCINT			U11	P11	R15			
		VCCINT			U13	P13	R18			
		VCCINT			U15	P14	R20			
		VCCINT			U17	P15	T14			
		VCCINT			V12	P17	T16			
		VCCINT			V16	P19	T17			
		VCCINT				P21	T19			
		VCCINT				R12	U14			
		VCCINT				R13	U16			
		VCCINT				R14	U17			
		VCCINT				R18	U19			
		VCCINT				R19	V13			
		VCCINT				R20	V15			
		VCCINT				T11	V18			
		VCCINT				T13	V20			
		VCCINT				T19	W14			
		VCCINT				T21	W16			
		VCCINT				U10	W17			
		VCCINT				U14	W19			
		VCCINT				U18	Y13			
		VCCINT				U22	Y15			
		VCCINT				V11	Y18			
		VCCINT				V13	Y20			
		VCCINT				V15				
		VCCINT				V17				

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT				V19				
		VCCINT				V21				
		VCCINT				W12				
		VCCINT				W14				
		VCCINT				W16				
		VCCINT				W18				
		VCCINT				W20				
		VCCINT				Y11				
		VCCINT				Y13				
		VCCINT				Y15				
		VCCINT				Y19				
		VCCINT				Y21				
		GND			A14	A1	A10			
		GND			A15	A11	A2			
		GND			AA16	A2	A23			
		GND			AC15	A21	A31			
		GND			AF26	A30	AA16			
		GND			AF3	A31	AA17			
		GND			AG2	AA17	AC1			
		GND			AG27	AA18	AC32			
		GND			AH14	AB16	AD17			
		GND			AH15	AD18	AF17			
		GND			B2	AK1	AL1			
		GND			B27	AK2	AL2			
		GND			C26	AK30	AL31			
		GND			C3	AK31	AL32			
		GND			G15	AL1	AM10			
		GND			H16	AL11	AM2			
		GND			L14	AL2	AM23			
		GND			L15	AL21	AM31			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			M15	AL30	B1			
		GND			N12	AL31	B2			
		GND			N14	B1	B31			
		GND			N16	B2	B32			
		GND			N18	B30	H18			
		GND			P1	B31	J17			
		GND			P11	H17	K1			
		GND			P13	H18	K32			
		GND			P15	K16	M13			
		GND			P17	L15	M15			
		GND			P18	L17	M16			
		GND			P28	M1	M17			
		GND			R1	M12	M18			
		GND			R11	M14	M20			
		GND			R12	M16	N12			
		GND			R14	M18	N14			
		GND			R16	M20	N16			
		GND			R18	M31	N17			
		GND			R28	N11	N19			
		GND			T11	N13	N21			
		GND			T13	N15	P13			
		GND			T15	N17	P15			
		GND			T17	N19	P18			
		GND			U12	N21	P20			
		GND			U14	P12	R14			
		GND			U16	P16	R16			
		GND			U18	P18	R17			
		GND			V13	P20	R19			
		GND			V14	R11	T12			
		GND			V15	R15	T13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			V17	R17	T15			
		GND				R21	T18			
		GND				T10	T20			
		GND				T12	T21			
		GND				T14	U12			
		GND				T18	U13			
		GND				T20	U15			
		GND				T22	U18			
		GND				U11	U20			
		GND				U13	U21			
		GND				U15	V14			
		GND				U17	V16			
		GND				U19	V17			
		GND				U21	V19			
		GND				V12	W13			
		GND				V14	W15			
		GND				V16	W18			
		GND				V18	W20			
		GND				V20	Y14			
		GND				W11	Y16			
		GND				W13	Y17			
		GND				W15	Y19			
		GND				W17				
		GND				W19				
		GND				W21				
		GND				Y1				
		GND				Y12				
		GND				Y14				
		GND				Y16				
		GND				Y18				

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND				Y20				
		GND				Y31				
		NC			AC25	AA22	AA11			
		NC			AC26	AB10	AA13			
		NC			AC3	AB11	AB10			
		NC			AC4	AB15	AB12			
		NC			AD25	AB18	AC11			
		NC			AD26	AB19	AD10			
		NC			AD3	AC14	AD11			
		NC			AD4	AC15	AE10			
		NC			D25	AD14	AE16			
		NC			D26	H14	AE22			
		NC			D3	H15	AF11			
		NC			D4	J14	AF16			
		NC			E25	J15	AG16			
		NC			E26	K13	AG25			
		NC			E3	K14	AG26			
		NC			E4	K21	AG27			
		NC				K22	AG28			
		NC				L10	AG5			
		NC				P22	AG7			
		NC				V10	AG8			
		NC					AH1			
		NC					AH16			
		NC					AH2			
		NC					AH21			
		NC					AH29			
		NC					AH31			
		NC					AH32			
		NC					AH4			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC					AH6			
		NC					E12			
		NC					E16			
		NC					E17			
		NC					E27			
		NC					E29			
		NC					E4			
		NC					F11			
		NC					F28			
		NC					F5			
		NC					G11			
		NC					H10			
		NC					H15			
		NC					H16			
		NC					J10			
		NC					K10			
		NC					L10			
		NC					M11			
		NC					N11			
		NC					N22			
		NC					P11			
		NC					P22			
		NC					U22			
		NC					V12			
		NC					V22			
		NC					W11			
		NC					W12			
		NC					W21			
		NC					W22			
		NC					Y11			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC					Y12			
		NC					Y21			
		NC					Y22			
Note to Pin-List:										
1) The wire bond and flip-chip packages will have different data rates for the high speed differential I/O channels. The following table shows the data rates as supported for each package.										

Package	Package Type	High Speed Differential I/O Channel Performance (DIFFIO Speed)		Units
		High	Low	
F780	flip chip	840	N/A	Mbps
B956	flip chip	840	N/A	Mbps
F1020	flip chip	840	462	Mbps

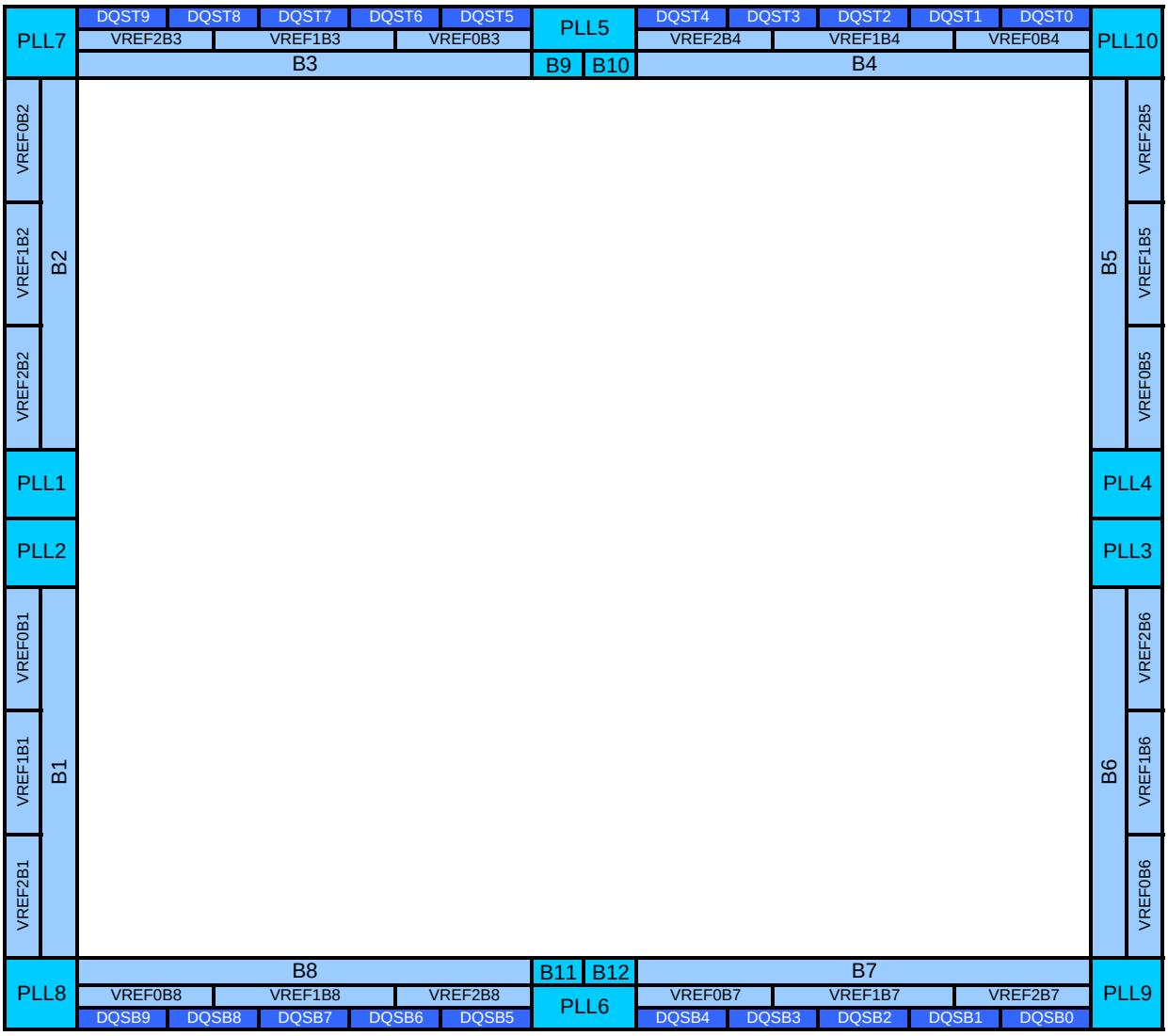
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..8]	Input	Input reference voltage for bank 1. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, designers should connect them to either VCC or Gnd.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1..12]	Power	Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1..12]	Ground	Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA.
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins.
FPLL[10..7]CLKp	Input	Dedicated global clock inputs for fast PLLs (PLLs 7 through 10).
FPLL[10..7]CLKn	Input	Dedicated negative terminal associated with FPLL[10..7]CLKp pins.
CLK[15..0]p	Input	Dedicated global clock inputs 0 to 15.
CLK[15..0]n	I/O, Input	Optional negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6).
PLL6_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL5_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5).
PLL5_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
	Optional/Dual-Purpose Pins	
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete.
DIFFIO_TX[0..81]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_RX[0..81]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

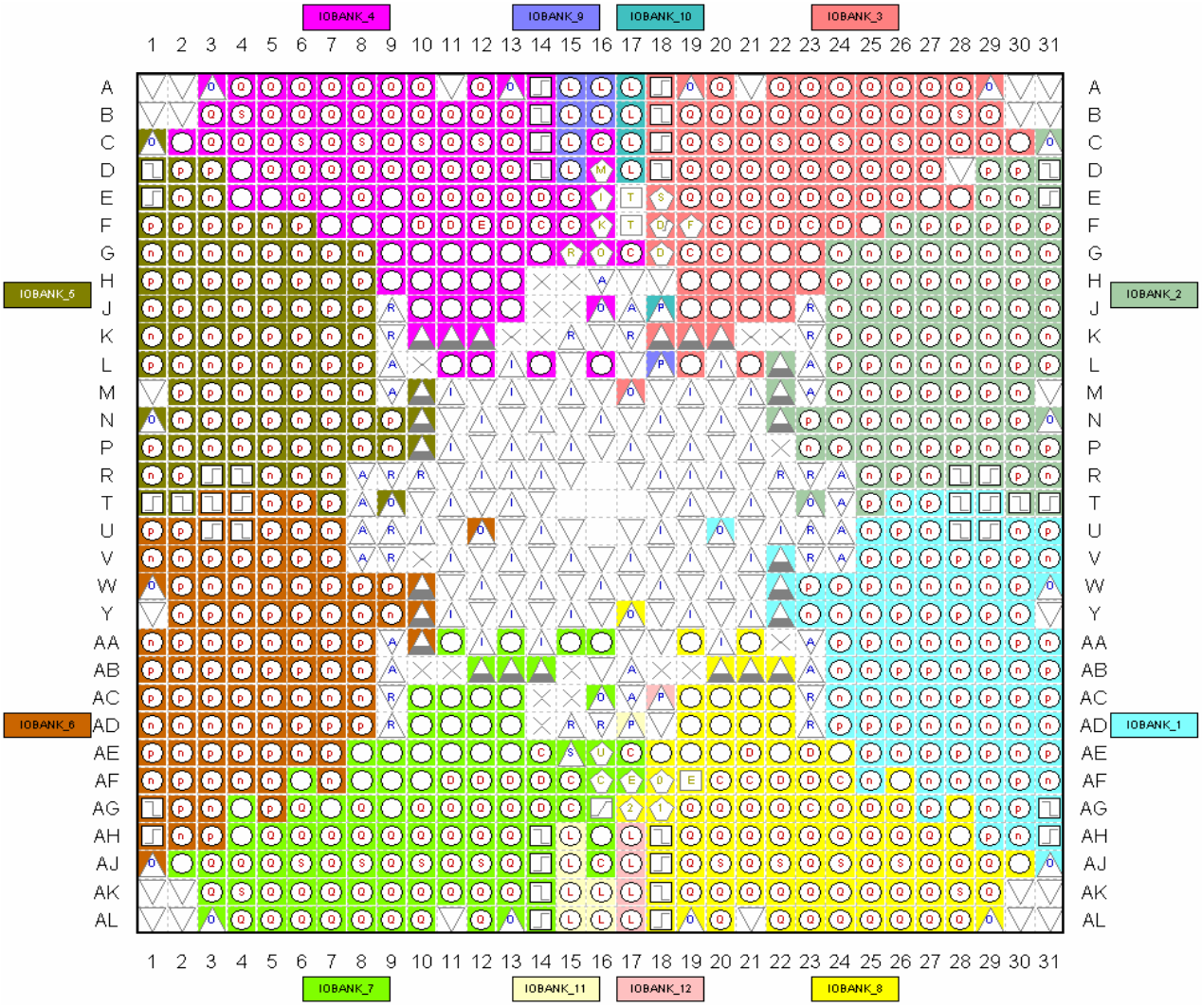
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp.
PLL6_FBp	I/O, Input	External feedback input pin for PLL6.
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp.
INIT_DONE	I/O, Output	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
RUP[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2=0, the RUnLU pin is a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.



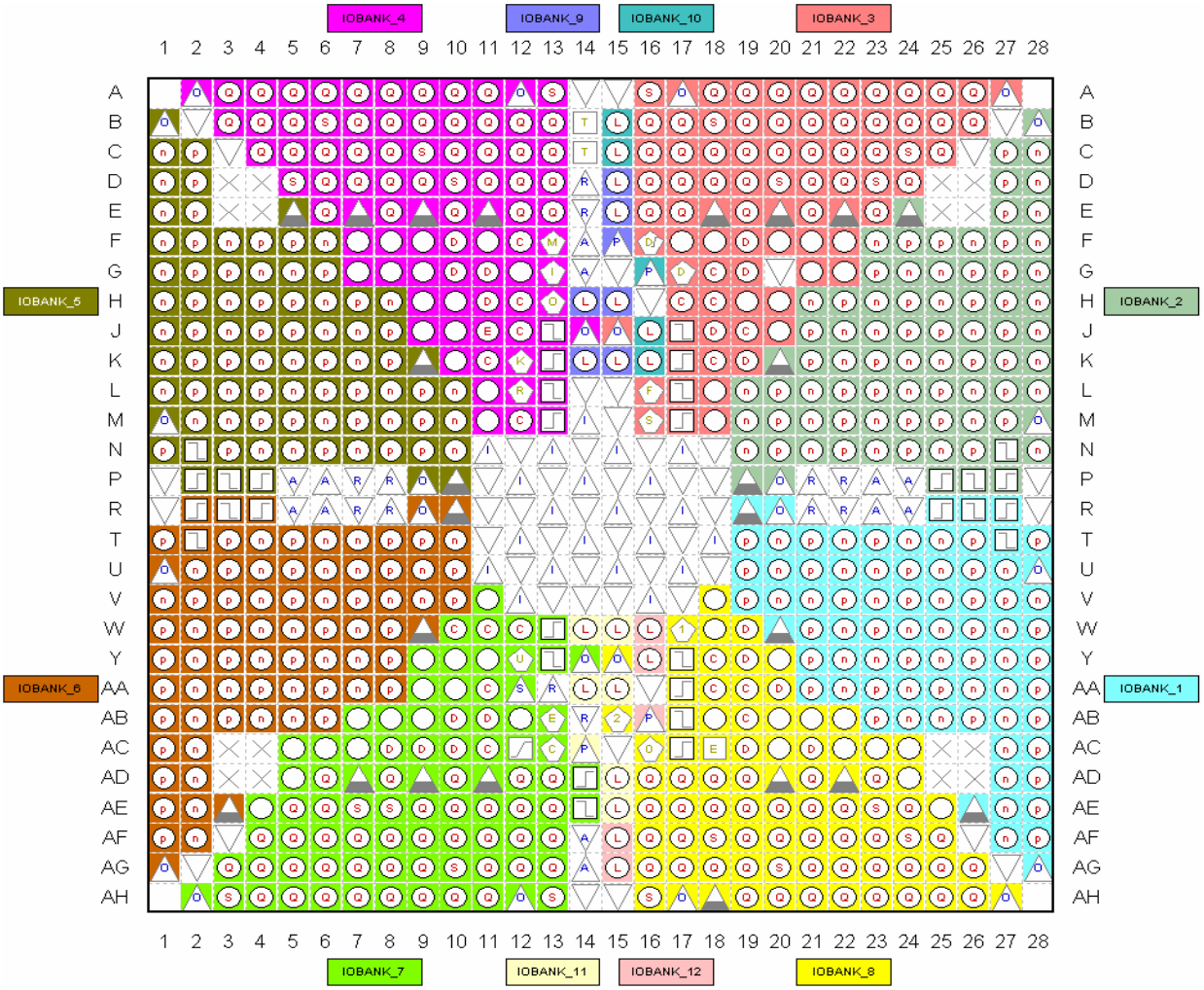
Notes:
1.This is a top view of the silicon die. For flip chip packages the die is mounted up-side down in the package.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

STRATIX EP1S30 B956 Device Package Diagram



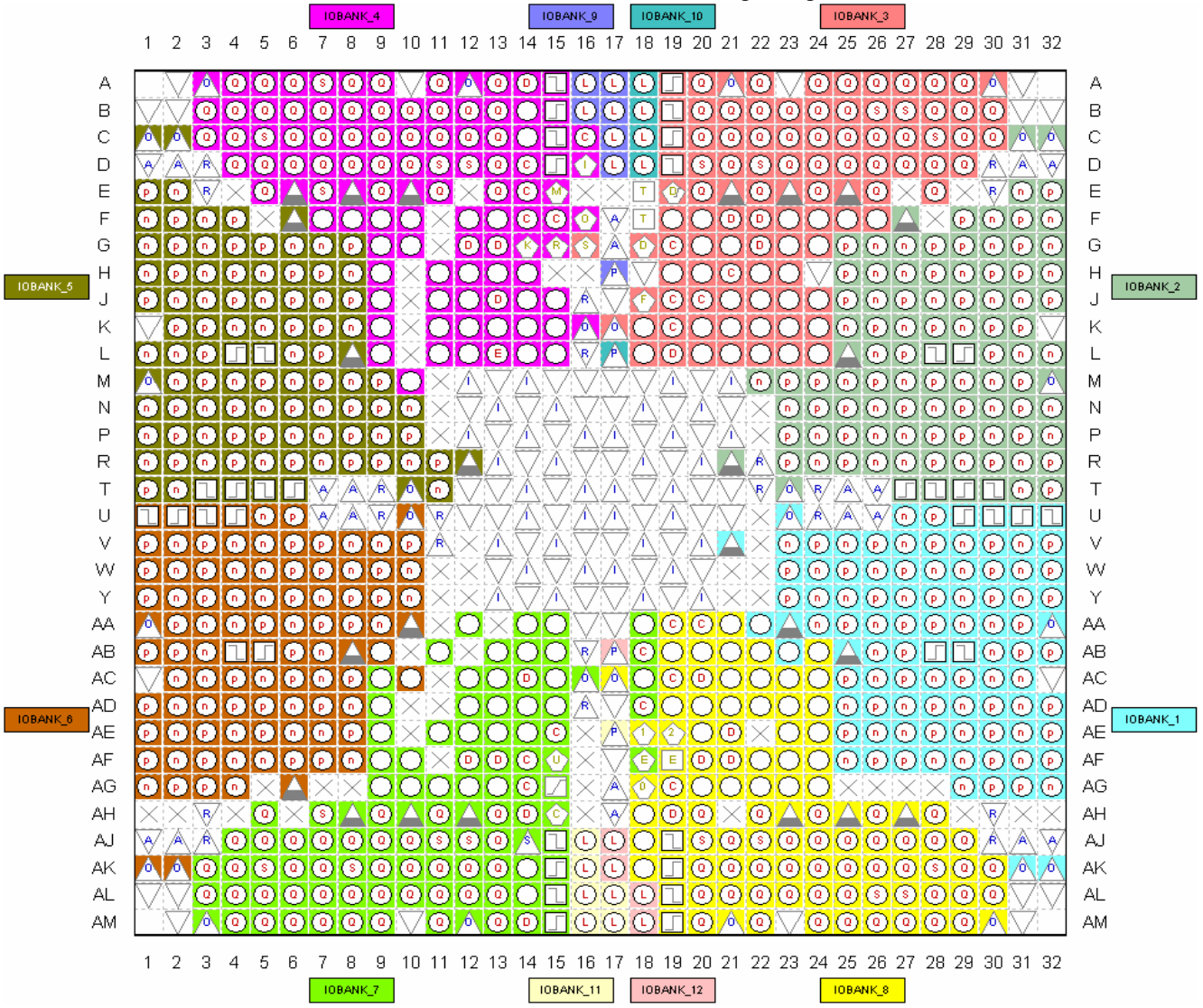
USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

STRATIX EP1S30 F780 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

STRATIX EP1S30 F1020 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

Clock Resources for High Speed Differential I/O (DIFFIO) Receiver and Transmitter channels. *Notes (5), (7)*										
Device	**Pin Count**	**Source FAST PLL**	**Rx Channels** ***Note (1)***		**Tx channels** ***Note (2)***		**Overlapped Rx Channels** ***Note (3)***		**Overlapped Tx Channels** ***Note (4)***	
			High ***(6)***	**Low** ***(6)***	**High** ***(6)***	**Low** ***(6)***	**High** ***(6)***	**Low** ***(6)***	**High** ***(6)***	**Low** ***(6)***
EP1S30	780	PLL1	[20-36]	-	[21-38]	-	-	-	-	-
		PLL2	[4-19]	-	[3-19]	-	-	-	-	-
		PLL3	[62-77]	-	[62-78]	-	-	-	-	-
		PLL4	[45-61]	-	[43-60]	-	-	-	-	-
		PLL7	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
		PLL8	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
		PLL9	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
		PLL10	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
	956	PLL1	[20-39]	-	[21-39]	-	[20-39]	-	[21-39]	-
		PLL2	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL3	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL4	[42-61]	-	[42-60]	-	[42-60]	-	[42-60]	-
		PLL7	[21-39]	-	[21-40]	-	[20-39]	-	[21-39]	-
		PLL8	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL9	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL10	[42-60]	-	[41-60]	-	[42-60]	-	[42-60]	-
	1020	PLL1	[20-39]	-	[21-39]	-	[20-39]	-	[21-39]	-
		PLL2	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL3	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL4	[42-61]	-	[42-60]	-	[42-60]	-	[42-60]	-
		PLL7	[21-39]	[40]	[21-40]	[20]	[20-39]	-	[21-39]	-
		PLL8	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL9	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL10	[42-60]	[41]	[41-60]	[61]	[42-60]	-	[42-60]	-

Notes:
1. These Rx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.

2. These Tx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
3. These Rx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.
4. These Tx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.
5. Each range of channel numbers are shown in [ ] brackets.
6. Data channels designated as "high" speed support a maximum data rate of 840 Mbps for -5 and -6 speed grade devices and 624 Mbps for -7 speed grade devices. Data channels designated as "low" speed support a maximum data rate of 462 Mbps for all speed grades.
7. The high speed differential I/O (DIFFIO) channels span across two banks on both sides of the device. Each Fast PLL can normally only feed channels in one bank. However, the center PLLs can also clock the channels associated with the adjacent center PLL on the same side of the device through a mux that is shown in figures 5-16 and 5-17 in volume 2 of the Stratix Device Handbook. These channels are called "cross-bank" channels. When cross-bank channels are used only one center PLL on each side can be used.
8. PLLs 7, 8, 9, and 10 are not available for the EP1S30 and EP1S40 devices in the F780 package.

Version Number	Date	Changes Made
3.4	2/4/2005	Revised package diagrams.
3.5	11/14/2005	Update all package diagram for EP1S30.
3.6	3/2/2006	Added CRC_ERROR pin in Pin List and Pin Definition