Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L5		GXB_TX_L32n					E38				
GXB_L5		GXB_TX_L32p					E37				
GXB_L5		GXB_RX_L32n,GXB_REFCLK_L32n					E42				
GXB_L5		GXB_RX_L32p,GXB_REFCLK_L32p					E41				
GXB_L5		GXB_TX_L31n					F36				
GXB_L5		GXB_TX_L31p					F35				
GXB_L5		GXB_RX_L31n,GXB_REFCLK_L31n					F40				
GXB_L5		GXB_RX_L31p,GXB_REFCLK_L31p					F39				
GXB_L5		GXB_TX_L30n					G38				
GXB_L5		GXB_TX_L30p					G37				
GXB_L5		GXB_RX_L30n,GXB_REFCLK_L30n					G42				
GXB_L5		GXB_RX_L30p,GXB_REFCLK_L30p					G41				
GXB_L5		REFCLK10Lp					N33				
GXB_L5		REFCLK10Ln					N32				
GXB_L4		REFCLK9Lp					R32				
GXB_L4		REFCLK9Ln					R33				
GXB_L4		GXB_TX_L29n					H36				
GXB_L4		GXB_TX_L29p					H35				
GXB_L4		GXB_RX_L29n,GXB_REFCLK_L29n					H40				
GXB_L4		GXB_RX_L29p,GXB_REFCLK_L29p					H39				
GXB_L4		GXB_TX_L28n					J38				
GXB_L4		GXB_TX_L28p					J37				
GXB_L4		GXB_RX_L28n,GXB_REFCLK_L28n					J42				
GXB_L4		GXB_RX_L28p,GXB_REFCLK_L28p					J41				
GXB_L4		GXB_TX_L27n					K36				
GXB_L4		GXB_TX_L27p					K35				
GXB_L4		GXB_RX_L27n,GXB_REFCLK_L27n					K40				
GXB_L4		GXB_RX_L27p,GXB_REFCLK_L27p					K39				
GXB_L4		GXB_TX_L26n					L38				
GXB_L4		GXB_TX_L26p					L37				
GXB_L4		GXB_RX_L26n,GXB_REFCLK_L26n					L42				
GXB_L4		GXB_RX_L26p,GXB_REFCLK_L26p					L41				
GXB_L4		GXB_TX_L25n					M36				
GXB_L4		GXB_TX_L25p					M35				
GXB_L4		GXB_RX_L25n,GXB_REFCLK_L25n					M40				
GXB_L4		GXB_RX_L25p,GXB_REFCLK_L25p					M39				
GXB_L4		GXB_TX_L24n					N38				
GXB_L4		GXB_TX_L24p					N37				
GXB_L4		GXB_RX_L24n,GXB_REFCLK_L24n					N42				
GXB_L4		GXB_RX_L24p,GXB_REFCLK_L24p					N41				
GXB_L4		REFCLK8Lp					U33				
GXB_L4		REFCLK8Ln					U34				
GXB_L3		REFCLK7Lp					W32				
GXB_L3		REFCLK7Ln					W33				
GXB_L3		GXB_TX_L23n					P36				
GXB_L3		GXB_TX_L23p					P35				
GXB_L3		GXB_RX_L23n,GXB_REFCLK_L23n					P40				
GXB_L3		GXB_RX_L23p,GXB_REFCLK_L23p					P39				
GXB_L3		GXB_TX_L22n					R38				
GXB_L3		GXB_TX_L22p					R37				
GXB_L3		GXB_RX_L22n,GXB_REFCLK_L22n					R42				
GXB_L3		GXB_RX_L22p,GXB_REFCLK_L22p					R41				
GXB_L3		GXB_TX_L21n					T36				
GXB_L3		GXB_TX_L21p					T35				
GXB_L3		GXB_RX_L21n,GXB_REFCLK_L21n					T40				
GXB_L3		GXB_RX_L21p,GXB_REFCLK_L21p					T39				
GXB_L3		GXB_TX_L20n					U38				
GXB_L3		GXB_TX_L20p					U37				
GXB_L3		GXB_RX_L20n,GXB_REFCLK_L20n					U42				
GXB_L3		GXB_RX_L20p,GXB_REFCLK_L20p					U41				
GXB_L3		GXB_TX_L19n					V36				
GXB_L3		GXB_TX_L19p					V35				
GXB_L3		GXB_RX_L19n,GXB_REFCLK_L19n					V40				
GXB_L3		GXB_RX_L19p,GXB_REFCLK_L19p					V39				
GXB_L3		GXB_TX_L18n					W38				
GXB_L3		GXB_TX_L18p					W37				
GXB_L3		GXB_RX_L18n,GXB_REFCLK_L18n					W42				
GXB_L3		GXB_RX_L18p,GXB_REFCLK_L18p					W41				
GXB_L3		REFCLK6Lp					AA33				
GXB_L3		REFCLK6Ln					AA34				
GXB_L2		REFCLK5Lp					AC32				
GXB_L2		REFCLK5Ln					AC33				
GXB_L2		GXB_TX_L17n					Y36				
GXB_L2		GXB_TX_L17p					Y35				
GXB_L2		GXB_RX_L17n,GXB_REFCLK_L17n					Y40				
GXB_L2		GXB_RX_L17p,GXB_REFCLK_L17p					Y39				
GXB_L2		GXB_TX_L16n					AA38				
GXB_L2		GXB_TX_L16p					AA37				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L2		GXB_RX_L16n,GXB_REFCLK_L16n					AA42				
GXB_L2		GXB_RX_L16p,GXB_REFCLK_L16p					AA41				
GXB_L2		GXB_TX_L15n					AB36				
GXB_L2		GXB_TX_L15p					AB35				
GXB_L2		GXB_RX_L15n,GXB_REFCLK_L15n					AB40				
GXB_L2		GXB_RX_L15p,GXB_REFCLK_L15p					AB39				
GXB_L2		GXB_TX_L14n					AC38				
GXB_L2		GXB_TX_L14p					AC37				
GXB_L2		GXB_RX_L14n,GXB_REFCLK_L14n					AC42				
GXB_L2		GXB_RX_L14p,GXB_REFCLK_L14p					AC41				
GXB_L2		GXB_TX_L13n					AD36				
GXB_L2		GXB_TX_L13p					AD35				
GXB_L2		GXB_RX_L13n,GXB_REFCLK_L13n					AD40				
GXB_L2		GXB_RX_L13p,GXB_REFCLK_L13p					AD39				
GXB_L2		GXB_TX_L12n					AE38				
GXB_L2		GXB_TX_L12p					AE37				
GXB_L2		GXB_RX_L12n,GXB_REFCLK_L12n					AE42				
GXB_L2		GXB_RX_L12p,GXB_REFCLK_L12p					AE41				
GXB_L2		REFCLK4Lp					AE33				
GXB_L2		REFCLK4Ln					AE34				
GXB_L1		REFCLK3Lp					AG32				
GXB_L1		REFCLK3Ln					AG33				
GXB_L1		GXB_TX_L11n					AF36				
GXB_L1		GXB_TX_L11p					AF35				
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					AF40				
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					AF39				
GXB_L1		GXB_TX_L10n					AG38				
GXB_L1		GXB_TX_L10p					AG37				
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					AG42				
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					AG41				
GXB_L1		GXB_TX_L9n					AH36				
GXB_L1		GXB_TX_L9p					AH35				
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					AH40				
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					AH39				
GXB_L1		GXB_TX_L8n					AJ38				
GXB_L1		GXB_TX_L8p					AJ37				
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					AJ42				
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					AJ41				
GXB_L1		GXB_TX_L7n					AK36				
GXB_L1		GXB_TX_L7p					AK35				
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					AK40				
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					AK39				
GXB_L1		GXB_TX_L6n					AL38				
GXB_L1		GXB_TX_L6p					AL37				
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					AL42				
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					AL41				
GXB_L1		REFCLK2Lp					AJ33				
GXB_L1		REFCLK2Ln					AJ34				
GXB_L0		REFCLK1Lp					AL32				
GXB_L0		REFCLK1Ln					AL33				
GXB_L0		GXB_TX_L5n					AM36				
GXB_L0		GXB_TX_L5p					AM35				
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					AM40				
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					AM39				
GXB_L0		GXB_TX_L4n					AN38				
GXB_L0		GXB_TX_L4p					AN37				
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AN42				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AN41				
GXB_L0		GXB_TX_L3n					AP36				
GXB_L0		GXB_TX_L3p					AP35				
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AP40				
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AP39				
GXB_L0		GXB_TX_L2n					AR38				
GXB_L0		GXB_TX_L2p					AR37				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AR42				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AR41				
GXB_L0		GXB_TX_L1n					AT36				
GXB_L0		GXB_TX_L1p					AT35				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AT40				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AT39				
GXB_L0		GXB_TX_L0n					AU38				
GXB_L0		GXB_TX_L0p					AU37				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AU42				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AU41				
GXB_L0		REFCLK0Lp					AN33				
GXB_L0		REFCLK0Ln					AN34				
3A		nCONFIG		nCONFIG			AU34				
3A		TRST		TRST			AV36				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3A		TMS		TMS			AV33				
3A		TCK		TCK			AW37				
3A		TDI		TDI			AU32				
3A		TDO		TDO			AP30				
3A		nCSO		nCSO			AH30				
3A		AS_DATA3		AS_DATA3			AW36				
3A		AS_DATA2		AS_DATA2			AG30				
3A		AS_DATA1		AS_DATA1			AT32				
3A		AS_DATA0,ASDO		AS_DATA0,ASDO			AK30				
3A		DCLK		DCLK			AL30				
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_TX_B1n	DIFFOUT_B1n	AY38	DQ1B	DQ1B		
3A	VREFB3AN0	IO		CRC_ERROR	DIFFIO_TX_B1p	DIFFOUT_B1p	AW38	DQ1B	DQ1B		
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_RX_B2n	DIFFOUT_B2n	AW35	DQSn1B	DQ1B		
3A	VREFB3AN0	IO		DEV_OE	DIFFIO_RX_B2p	DIFFOUT_B2p	AV35	DQS1B	DQ1B/CQn1B		
3A	VREFB3AN0	IO		DEV_CLRn	DIFFIO_TX_B3n	DIFFOUT_B3n	AY37	DQ1B	DQ1B		
3A	VREFB3AN0	IO		INIT_DONE	DIFFIO_TX_B3p	DIFFOUT_B3p	AY36	DQ1B	DQ1B		
3A	VREFB3AN0	IO		nCEO	DIFFIO_RX_B4n	DIFFOUT_B4n	AY39	DQSn2B	DQSn1B/DQ1B		
3A	VREFB3AN0	IO		DATA0	DIFFIO_RX_B4p	DIFFOUT_B4p	AW39	DQS2B	DQS1B/CQ1B		
3A	VREFB3AN0	IO		DATA1	DIFFIO_TX_B5n	DIFFOUT_B5n	AY40	DQ2B	DQ1B		
3A	VREFB3AN0	IO		DATA2	DIFFIO_TX_B5p	DIFFOUT_B5p	AW40	DQ2B	DQ1B		
3A	VREFB3AN0	IO		DATA3	DIFFIO_RX_B6n	DIFFOUT_B6n	BB41	DQ2B	DQ1B		
3A	VREFB3AN0	IO		DATA4	DIFFIO_RX_B6p	DIFFOUT_B6p	BB40	DQ2B	DQ1B		
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B7n	DIFFOUT_B7n	BB39	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA6	DIFFIO_TX_B7p	DIFFOUT_B7p	BB38	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_RX_B8n	DIFFOUT_B8n	AY34	DQSn3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B8p	DIFFOUT_B8p	AW34	DQS3B	DQ2B/CQn2B	DQ1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B9n	DIFFOUT_B9n	BB37	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_TX_B9p	DIFFOUT_B9p	BB36	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_RX_B10n	DIFFOUT_B10n	AW33	DQSn4B	DQSn2B/DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B10p	DIFFOUT_B10p	AV32	DQS4B	DQS2B/CQ2B	DQ1B/CQn1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B11n	DIFFOUT_B11n	AV30	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA14	DIFFIO_TX_B11p	DIFFOUT_B11p	AU30	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_RX_B12n	DIFFOUT_B12n	AW31	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA16	DIFFIO_RX_B12p	DIFFOUT_B12p	AV31	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA17	DIFFIO_TX_B13n	DIFFOUT_B13n	AM29	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA18	DIFFIO_TX_B13p	DIFFOUT_B13p	AL29	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA19	DIFFIO_RX_B14n	DIFFOUT_B14n	AT30	DQSn5B	DQ3B	DQSn1B/DQ1B	
3A	VREFB3AN0	IO		DATA20	DIFFIO_RX_B14p	DIFFOUT_B14p	AR31	DQS5B	DQ3B/CQn3B	DQS1B/CQ1B	
3A	VREFB3AN0	IO		DATA21	DIFFIO_TX_B15n	DIFFOUT_B15n	AR29	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA22	DIFFIO_TX_B15p	DIFFOUT_B15p	AP29	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA23	DIFFIO_RX_B16n	DIFFOUT_B16n	AH28	DQSn6B	DQSn3B/DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA24	DIFFIO_RX_B16p	DIFFOUT_B16p	AH29	DQS6B	DQS3B/CQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA25	DIFFIO_TX_B17n	DIFFOUT_B17n	AK29	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA26	DIFFIO_TX_B17p	DIFFOUT_B17p	AJ29	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA27	DIFFIO_RX_B18n	DIFFOUT_B18n	AK28	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA28	DIFFIO_RX_B18p	DIFFOUT_B18p	AJ28	DQ6B	DQ3B	DQ1B	
3B	VREFB3BN0	IO		DATA29	DIFFIO_TX_B19n	DIFFOUT_B19n	AY33	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA30	DIFFIO_TX_B19p	DIFFOUT_B19p	BA34	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA31	DIFFIO_RX_B20n	DIFFOUT_B20n	BB35	DQSn7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		PR_DONE	DIFFIO_RX_B20p	DIFFOUT_B20p	BB34	DQS7B	DQ4B/CQn4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		PR_REQUEST	DIFFIO_TX_B21n	DIFFOUT_B21n	BB32	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		PR_READY	DIFFIO_TX_B21p	DIFFOUT_B21p	BB31	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK0n		DIFFIO_RX_B22n	DIFFOUT_B22n	BA32	DQSn8B	DQSn4B/DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK0p		DIFFIO_RX_B22p	DIFFOUT_B22p	BA31	DQS8B	DQS4B/CQ4B	DQ2B/CQn2B	DQ1B
3B	VREFB3BN0	IO		PR_ERROR	DIFFIO_TX_B23n	DIFFOUT_B23n	AV27	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		CvP_CONFDONE	DIFFIO_TX_B23p	DIFFOUT_B23p	AW28	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B24n	DIFFOUT_B24n	AY31	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B24p	DIFFOUT_B24p	AY30	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B25n	DIFFOUT_B25n	AN28	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B25p	DIFFOUT_B25p	AM28	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B26n	DIFFOUT_B26n	AT28	DQSn9B	DQ5B	DQSn2B/DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B26p	DIFFOUT_B26p	AR28	DQS9B	DQ5B/CQn5B	DQS2B/CQ2B	DQ1B
3B	VREFB3BN0	IO		nPERSTL0	DIFFIO_TX_B27n	DIFFOUT_B27n	AP28	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		nPERSTL1	DIFFIO_TX_B27p	DIFFOUT_B27p	AP27	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK2n		DIFFIO_RX_B28n	DIFFOUT_B28n	AV29	DQSn10B	DQSn5B/DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK2p		DIFFIO_RX_B28p	DIFFOUT_B28p	AW30	DQS10B	DQS5B/CQ5B	DQ2B	DQ1B/CQn1B
3B	VREFB3BN0	IO		nPERSTR1	DIFFIO_TX_B29n	DIFFOUT_B29n	AV28	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		nPERSTR0	DIFFIO_TX_B29p	DIFFOUT_B29p	AU29	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK3n		DIFFIO_RX_B30n	DIFFOUT_B30n	AU27	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK3p		DIFFIO_RX_B30p	DIFFOUT_B30p	AT27	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AN27	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AM27	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AL26	DQSn11B	DQ6B	DQ3B	DQSn1B/DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AK26	DQS11B	DQ6B/CQn6B	DQ3B	DQS1B/CQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AL27	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AK27	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AG28	DQSn12B	DQSn6B/DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AF27	DQS12B	DQS6B/CQ6B	DQ3B/CQn3B	DQ1B

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3B	VREFB3BN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AJ26	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AH26	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AH27	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AG27	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AE28	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AD28	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AF29	DQSn13B	DQ7B	DQSn3B/DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AF28	DQS13B	DQ7B/CQn7B	DQS3B/CQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AD29	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AC29	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AD27	DQSn14B	DQSn7B/DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AD26	DQS14B	DQS7B/CQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AD25	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AC25	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AF26	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AE26	DQ14B	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B43n	DIFFOUT_B43n	BA29	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	BA28	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	BB29	DQSn15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	BB28	DQS15B	DQ8B/CQn8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AY28	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AW27	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AY27	DQSn16B	DQSn8B/DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	BA26	DQS16B	DQS8B/CQ8B	DQ4B/CQn4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	BA25	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AY25	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	BB26	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	BB25	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AJ25	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AH25	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AF24	DQSn17B	DQ9B	DQSn4B/DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AF23	DQS17B	DQ9B/CQn9B	DQS4B/CQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AG25	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AF25	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AH24	DQSn18B	DQSn9B/DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AG24	DQS18B	DQS9B/CQ9B	DQ4B	DQ2B/CQn2B
3C	VREFB3CN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AK25	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AK24	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AJ23	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AH23	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B55n	DIFFOUT_B55n	AY24	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B55p	DIFFOUT_B55p	AW25	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B56n	DIFFOUT_B56n	AW24	DQSn19B	DQ10B	DQ5B	DQSn2B/DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B56p	DIFFOUT_B56p	AV24	DQS19B	DQ10B/CQn10B	DQ5B	DQS2B/CQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AV26	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AV25	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AU26	DQSn20B	DQSn10B/DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AT26	DQS20B	DQS10B/CQ10B	DQ5B/CQn5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B59n	DIFFOUT_B59n	AT25	DQ20B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B59p	DIFFOUT_B59p	AR25	DQ20B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B60n	DIFFOUT_B60n	AU24	DQ20B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B60p	DIFFOUT_B60p	AT24	DQ20B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AN25	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AM26	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AP26	DQSn21B	DQ11B	DQSn5B/DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AP25	DQS21B	DQ11B/CQn11B	DQS5B/CQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B63n	DIFFOUT_B63n	AM25	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B63p	DIFFOUT_B63p	AL24	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B64n	DIFFOUT_B64n	AP24	DQSn22B	DQSn11B/DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B64p	DIFFOUT_B64p	AN24	DQS22B	DQS11B/CQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AL23	DQ22B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AK23	DQ22B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AM24	DQ22B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AM23	DQ22B	DQ11B	DQ5B	DQ2B
3D	VREFB3DN0	IO			DIFFIO_TX_B67n	DIFFOUT_B67n	AK22	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B67p	DIFFOUT_B67p	AJ22	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B68n	DIFFOUT_B68n	AG22	DQSn23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B68p	DIFFOUT_B68p	AF22	DQS23B	DQ12B/CQn12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AH22	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AG21	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AH20	DQSn24B	DQSn12B/DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AH21	DQS24B	DQS12B/CQ12B	DQ6B/CQn6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B71n	DIFFOUT_B71n	AF19	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B71p	DIFFOUT_B71p	AF20	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B72n	DIFFOUT_B72n	AJ20	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B72p	DIFFOUT_B72p	AK20	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	BB22	DQ25B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	BB23	DQ25B	DQ13B	DQ6B	

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3D	VREFB3DN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AY21	DQSn25B	DQ13B	DQSn6B/DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AY22	DQS25B	DQ13B/CQn13B	DQS6B/CQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B75n	DIFFOUT_B75n	BA23	DQ25B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B75p	DIFFOUT_B75p	BA22	DQ25B	DQ13B	DQ6B	
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AW22	DQSn26B	DQSn13B/DQ13B	DQ6B	
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AV22	DQS26B	DQS13B/CQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AV23	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AU23	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AW21	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AV21	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B79n	DIFFOUT_B79n	AM22	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B79p	DIFFOUT_B79p	AM21	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B80n	DIFFOUT_B80n	AL21	DQSn27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B80p	DIFFOUT_B80p	AK21	DQS27B	DQ14B/CQn14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AM20	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AL20	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B82n	DIFFOUT_B82n	AR23	DQSn28B	DQSn14B/DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B82p	DIFFOUT_B82p	AR22	DQS28B	DQS14B/CQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B83n	DIFFOUT_B83n	AP21	DQ28B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B83p	DIFFOUT_B83p	AN21	DQ28B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B84n	DIFFOUT_B84n	AT23	DQ28B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B84p	DIFFOUT_B84p	AT22	DQ28B	DQ14B		
4D	VREFB4DN0	IO			DIFFIO_TX_B133n	DIFFOUT_B133n	AV20	DQ45B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_TX_B133p	DIFFOUT_B133p	AU20	DQ45B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_RX_B134n	DIFFOUT_B134n	AW19	DQSn45B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_RX_B134p	DIFFOUT_B134p	AV19	DQS45B	DQ15B/CQn15B		
4D	VREFB4DN0	IO			DIFFIO_TX_B135n	DIFFOUT_B135n	AT20	DQ45B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_TX_B135p	DIFFOUT_B135p	AR20	DQ45B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_RX_B136n	DIFFOUT_B136n	AV18	DQSn46B	DQSn15B/DQ15B		
4D	VREFB4DN0	IO			DIFFIO_RX_B136p	DIFFOUT_B136p	AU18	DQS46B	DQS15B/CQ15B		
4D	VREFB4DN0	IO			DIFFIO_TX_B137n	DIFFOUT_B137n	AN19	DQ46B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_TX_B137p	DIFFOUT_B137p	AP20	DQ46B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_RX_B138n	DIFFOUT_B138n	AT19	DQ46B	DQ15B		
4D	VREFB4DN0	IO			DIFFIO_RX_B138p	DIFFOUT_B138p	AR19	DQ46B	DQ15B		
4D	VREFB4DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B139n	DIFFOUT_B139n	AY20	DQ47B	DQ16B	DQ7B	
4D	VREFB4DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B139p	DIFFOUT_B139p	AY19	DQ47B	DQ16B	DQ7B	
4D	VREFB4DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B140n	DIFFOUT_B140n	AY18	DQSn47B	DQ16B	DQ7B	
4D	VREFB4DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B140p	DIFFOUT_B140p	AW18	DQS47B	DQ16B/CQn16B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B141n	DIFFOUT_B141n	BB17	DQ47B	DQ16B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B141p	DIFFOUT_B141p	BA17	DQ47B	DQ16B	DQ7B	
4D	VREFB4DN0	IO	CLK6n		DIFFIO_RX_B142n	DIFFOUT_B142n	BB20	DQSn48B	DQSn16B/DQ16B	DQ7B	
4D	VREFB4DN0	IO	CLK6p		DIFFIO_RX_B142p	DIFFOUT_B142p	BA20	DQS48B	DQS16B/CQ16B	DQ7B/CQn7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B143n	DIFFOUT_B143n	BB16	DQ48B	DQ16B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B143p	DIFFOUT_B143p	BA16	DQ48B	DQ16B	DQ7B	
4D	VREFB4DN0	IO	CLK7n		DIFFIO_RX_B144n	DIFFOUT_B144n	BB19	DQ48B	DQ16B	DQ7B	
4D	VREFB4DN0	IO	CLK7p		DIFFIO_RX_B144p	DIFFOUT_B144p	BA19	DQ48B	DQ16B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B145n	DIFFOUT_B145n	AH19	DQ49B	DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B145p	DIFFOUT_B145p	AG19	DQ49B	DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_RX_B146n	DIFFOUT_B146n	AK19	DQSn49B	DQ17B	DQSn7B/DQ7B	
4D	VREFB4DN0	IO			DIFFIO_RX_B146p	DIFFOUT_B146p	AJ19	DQS49B	DQ17B/CQn17B	DQS7B/CQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B147n	DIFFOUT_B147n	AG18	DQ49B	DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B147p	DIFFOUT_B147p	AF18	DQ49B	DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_RX_B148n	DIFFOUT_B148n	AM18	DQSn50B	DQSn17B/DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_RX_B148p	DIFFOUT_B148p	AM19	DQS50B	DQS17B/CQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B149n	DIFFOUT_B149n	AL18	DQ50B	DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_TX_B149p	DIFFOUT_B149p	AK18	DQ50B	DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_RX_B150n	DIFFOUT_B150n	AH18	DQ50B	DQ17B	DQ7B	
4D	VREFB4DN0	IO			DIFFIO_RX_B150p	DIFFOUT_B150p	AH17	DQ50B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B151n	DIFFOUT_B151n	AD17	DQ51B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B151p	DIFFOUT_B151p	AC17	DQ51B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B152n	DIFFOUT_B152n	AF17	DQSn51B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B152p	DIFFOUT_B152p	AE17	DQS51B	DQ18B/CQn18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B153n	DIFFOUT_B153n	AG15	DQ51B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B153p	DIFFOUT_B153p	AF15	DQ51B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B154n	DIFFOUT_B154n	AG16	DQSn52B	DQSn18B/DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B154p	DIFFOUT_B154p	AF16	DQS52B	DQS18B/CQ18B	DQ8B/CQn8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B155n	DIFFOUT_B155n	AH15	DQ52B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B155p	DIFFOUT_B155p	AH16	DQ52B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B156n	DIFFOUT_B156n	AJ16	DQ52B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B156p	DIFFOUT_B156p	AJ17	DQ52B	DQ18B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B157n	DIFFOUT_B157n	AR17	DQ53B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B157p	DIFFOUT_B157p	AP17	DQ53B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B158n	DIFFOUT_B158n	AT17	DQSn53B	DQ19B	DQSn8B/DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B158p	DIFFOUT_B158p	AT18	DQS53B	DQ19B/CQn19B	DQS8B/CQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B159n	DIFFOUT_B159n	AV17	DQ53B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B159p	DIFFOUT_B159p	AU17	DQ53B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B160n	DIFFOUT_B160n	AR16	DQSn54B	DQSn19B/DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B160p	DIFFOUT_B160p	AT15	DQS54B	DQS19B/CQ19B	DQ8B	DQ3B/CQn3B

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4C	VREFB4CN0	IO			DIFFIO_TX_B161n	DIFFOUT_B161n	AU14	DQ54B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B161p	DIFFOUT_B161p	AU15	DQ54B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B162n	DIFFOUT_B162n	AV16	DQ54B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B162p	DIFFOUT_B162p	AV15	DQ54B	DQ19B	DQ8B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B163n	DIFFOUT_B163n	AY16	DQ55B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B163p	DIFFOUT_B163p	AW16	DQ55B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B164n	DIFFOUT_B164n	AY15	DQSn55B	DQ20B	DQ9B	DQSn3B/DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B164p	DIFFOUT_B164p	AW15	DQS55B	DQ20B/CQn20B	DQ9B	DQS3B/CQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B165n	DIFFOUT_B165n	AY13	DQ55B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B165p	DIFFOUT_B165p	AW13	DQ55B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B166n	DIFFOUT_B166n	BB14	DQSn56B	DQSn20B/DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B166p	DIFFOUT_B166p	BA14	DQS56B	DQS20B/CQ20B	DQ9B/CQn9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	BB11	DQ56B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B167p	DIFFOUT_B167p	BA11	DQ56B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B168n	DIFFOUT_B168n	BB13	DQ56B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B168p	DIFFOUT_B168p	BA13	DQ56B	DQ20B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B169n	DIFFOUT_B169n	AP18	DQ57B	DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B169p	DIFFOUT_B169p	AN18	DQ57B	DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B170n	DIFFOUT_B170n	AP15	DQSn57B	DQ21B	DQSn9B/DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B170p	DIFFOUT_B170p	AP16	DQS57B	DQ21B/CQn21B	DQS9B/CQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B171n	DIFFOUT_B171n	AM17	DQ57B	DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B171p	DIFFOUT_B171p	AL17	DQ57B	DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B172n	DIFFOUT_B172n	AN16	DQSn58B	DQSn21B/DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B172p	DIFFOUT_B172p	AM16	DQS58B	DQS21B/CQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B173n	DIFFOUT_B173n	AL15	DQ58B	DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_TX_B173p	DIFFOUT_B173p	AK15	DQ58B	DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B174n	DIFFOUT_B174n	AK16	DQ58B	DQ21B	DQ9B	DQ3B
4C	VREFB4CN0	IO			DIFFIO_RX_B174p	DIFFOUT_B174p	AK17	DQ58B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B175n	DIFFOUT_B175n	AR14	DQ59B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B175p	DIFFOUT_B175p	AP14	DQ59B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B176n	DIFFOUT_B176n	AN15	DQSn59B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B176p	DIFFOUT_B176p	AM15	DQS59B	DQ22B/CQn22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B177n	DIFFOUT_B177n	AK14	DQ59B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B177p	DIFFOUT_B177p	AJ14	DQ59B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B178n	DIFFOUT_B178n	AE15	DQSn60B	DQSn22B/DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B178p	DIFFOUT_B178p	AD15	DQS60B	DQS22B/CQ22B	DQ10B/CQn10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B179n	DIFFOUT_B179n	AF13	DQ60B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B179p	DIFFOUT_B179p	AF14	DQ60B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B180n	DIFFOUT_B180n	AH13	DQ60B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B180p	DIFFOUT_B180p	AG13	DQ60B	DQ22B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B181n	DIFFOUT_B181n	AV13	DQ61B	DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B181p	DIFFOUT_B181p	AV14	DQ61B	DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B182n	DIFFOUT_B182n	AY12	DQSn61B	DQ23B	DQSn10B/DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B182p	DIFFOUT_B182p	AW12	DQS61B	DQ23B/CQn23B	DQS10B/CQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B183n	DIFFOUT_B183n	AY10	DQ61B	DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B183p	DIFFOUT_B183p	AW10	DQ61B	DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B184n	DIFFOUT_B184n	BB10	DQSn62B	DQSn23B/DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B184p	DIFFOUT_B184p	BA10	DQS62B	DQS23B/CQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B185n	DIFFOUT_B185n	AY9	DQ62B	DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_TX_B185p	DIFFOUT_B185p	AW9	DQ62B	DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B186n	DIFFOUT_B186n	BB8	DQ62B	DQ23B	DQ10B	
4B	VREFB4BN0	IO			DIFFIO_RX_B186p	DIFFOUT_B186p	BA8	DQ62B	DQ23B	DQ10B	
4A	VREFB4AN0	IO			DIFFIO_TX_B199n	DIFFOUT_B199n	BA4	DQ67B	DQ24B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B199p	DIFFOUT_B199p	BA5	DQ67B	DQ24B	DQ11B	
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B200n	DIFFOUT_B200n	BB7	DQSn67B	DQ24B	DQ11B	
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B200p	DIFFOUT_B200p	BA7	DQS67B	DQ24B/CQn24B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B201n	DIFFOUT_B201n	AY6	DQ67B	DQ24B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B201p	DIFFOUT_B201p	AY7	DQ67B	DQ24B	DQ11B	
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B202n	DIFFOUT_B202n	BB4	DQSn68B	DQSn24B/DQ24B	DQ11B	
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B202p	DIFFOUT_B202p	BB5	DQS68B	DQS24B/CQ24B	DQ11B/CQn11B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B203n	DIFFOUT_B203n	BB2	DQ68B	DQ24B	DQ11B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B203p	DIFFOUT_B203p	BB3	DQ68B	DQ24B	DQ11B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B204n	DIFFOUT_B204n	AY3	DQ68B	DQ24B	DQ11B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B204p	DIFFOUT_B204p	AY4	DQ68B	DQ24B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B205n	DIFFOUT_B205n	AV11	DQ69B	DQ25B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B205p	DIFFOUT_B205p	AU11	DQ69B	DQ25B	DQ11B	
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B206n	DIFFOUT_B206n	AR12	DQSn69B	DQ25B	DQSn11B/DQ11B	
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B206p	DIFFOUT_B206p	AT13	DQS69B	DQ25B/CQn25B	DQS11B/CQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B207n	DIFFOUT_B207n	AV12	DQ69B	DQ25B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B207p	DIFFOUT_B207p	AU12	DQ69B	DQ25B	DQ11B	
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B208n	DIFFOUT_B208n	AV9	DQSn70B	DQSn25B/DQ25B	DQ11B	
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B208p	DIFFOUT_B208p	AU9	DQS70B	DQS25B/CQ25B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B209n	DIFFOUT_B209n	AW5	DQ70B	DQ25B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_TX_B209p	DIFFOUT_B209p	AW6	DQ70B	DQ25B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_RX_B210n	DIFFOUT_B210n	AW7	DQ70B	DQ25B	DQ11B	
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_RX_B210p	DIFFOUT_B210p	AW8	DQ70B	DQ25B	DQ11B	
4A		GND					AR13				
4A		nCE		nCE			AL14				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4A		nSTATUS		nSTATUS			AM14				
4A		CONF_DONE		CONF_DONE			AM13				
4A		nIO_PULLUP		nIO_PULLUP			AV8				
4A		MSEL0		MSEL0			AK13				
4A		MSEL1		MSEL1			AJ13				
4A		MSEL2		MSEL2			AW4				
4A		MSEL3		MSEL3			AW3				
4A		MSEL4		MSEL4			AV7				
GXB_R0		REFCLK0Rn					AN9				
GXB_R0		REFCLK0Rp					AN10				
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AU2				
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AU1				
GXB_R0		GXB_TX_R0p					AU6				
GXB_R0		GXB_TX_R0n					AU5				
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AT4				
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AT3				
GXB_R0		GXB_TX_R1p					AT8				
GXB_R0		GXB_TX_R1n					AT7				
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AR2				
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AR1				
GXB_R0		GXB_TX_R2p					AR6				
GXB_R0		GXB_TX_R2n					AR5				
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AP4				
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AP3				
GXB_R0		GXB_TX_R3p					AP8				
GXB_R0		GXB_TX_R3n					AP7				
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					AN2				
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					AN1				
GXB_R0		GXB_TX_R4p					AN6				
GXB_R0		GXB_TX_R4n					AN5				
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					AM4				
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					AM3				
GXB_R0		GXB_TX_R5p					AM8				
GXB_R0		GXB_TX_R5n					AM7				
GXB_R0		REFCLK1Rn					AL10				
GXB_R0		REFCLK1Rp					AL11				
GXB_R1		REFCLK2Rn					AJ9				
GXB_R1		REFCLK2Rp					AJ10				
GXB_R1		GXB_RX_R6p,GXB_REFCLK_R6p					AL2				
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					AL1				
GXB_R1		GXB_TX_R6p					AL6				
GXB_R1		GXB_TX_R6n					AL5				
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					AK4				
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					AK3				
GXB_R1		GXB_TX_R7p					AK8				
GXB_R1		GXB_TX_R7n					AK7				
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					AJ2				
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					AJ1				
GXB_R1		GXB_TX_R8p					AJ6				
GXB_R1		GXB_TX_R8n					AJ5				
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					AH4				
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					AH3				
GXB_R1		GXB_TX_R9p					AH8				
GXB_R1		GXB_TX_R9n					AH7				
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					AG2				
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					AG1				
GXB_R1		GXB_TX_R10p					AG6				
GXB_R1		GXB_TX_R10n					AG5				
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					AF4				
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					AF3				
GXB_R1		GXB_TX_R11p					AF8				
GXB_R1		GXB_TX_R11n					AF7				
GXB_R1		REFCLK3Rn					AG10				
GXB_R1		REFCLK3Rp					AG11				
GXB_R2		REFCLK4Rn					AE9				
GXB_R2		REFCLK4Rp					AE10				
GXB_R2		GXB_RX_R12p,GXB_REFCLK_R12p					AE2				
GXB_R2		GXB_RX_R12n,GXB_REFCLK_R12n					AE1				
GXB_R2		GXB_TX_R12p					AE6				
GXB_R2		GXB_TX_R12n					AE5				
GXB_R2		GXB_RX_R13p,GXB_REFCLK_R13p					AD4				
GXB_R2		GXB_RX_R13n,GXB_REFCLK_R13n					AD3				
GXB_R2		GXB_TX_R13p					AD8				
GXB_R2		GXB_TX_R13n					AD7				
GXB_R2		GXB_RX_R14p,GXB_REFCLK_R14p					AC2				
GXB_R2		GXB_RX_R14n,GXB_REFCLK_R14n					AC1				
GXB_R2		GXB_TX_R14p					AC6				
GXB_R2		GXB_TX_R14n					AC5				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_R2		GXB_RX_R15p,GXB_REFCLK_R15p					AB4				
GXB_R2		GXB_RX_R15n,GXB_REFCLK_R15n					AB3				
GXB_R2		GXB_TX_R15p					AB8				
GXB_R2		GXB_TX_R15n					AB7				
GXB_R2		GXB_RX_R16p,GXB_REFCLK_R16p					AA2				
GXB_R2		GXB_RX_R16n,GXB_REFCLK_R16n					AA1				
GXB_R2		GXB_TX_R16p					AA6				
GXB_R2		GXB_TX_R16n					AA5				
GXB_R2		GXB_RX_R17p,GXB_REFCLK_R17p					Y4				
GXB_R2		GXB_RX_R17n,GXB_REFCLK_R17n					Y3				
GXB_R2		GXB_TX_R17p					Y8				
GXB_R2		GXB_TX_R17n					Y7				
GXB_R2		REFCLK5Rn					AC10				
GXB_R2		REFCLK5Rp					AC11				
GXB_R3		REFCLK6Rn					AA9				
GXB_R3		REFCLK6Rp					AA10				
GXB_R3		GXB_RX_R18p,GXB_REFCLK_R18p					W2				
GXB_R3		GXB_RX_R18n,GXB_REFCLK_R18n					W1				
GXB_R3		GXB_TX_R18p					W6				
GXB_R3		GXB_TX_R18n					W5				
GXB_R3		GXB_RX_R19p,GXB_REFCLK_R19p					V4				
GXB_R3		GXB_RX_R19n,GXB_REFCLK_R19n					V3				
GXB_R3		GXB_TX_R19p					V8				
GXB_R3		GXB_TX_R19n					V7				
GXB_R3		GXB_RX_R20p,GXB_REFCLK_R20p					U2				
GXB_R3		GXB_RX_R20n,GXB_REFCLK_R20n					U1				
GXB_R3		GXB_TX_R20p					U6				
GXB_R3		GXB_TX_R20n					U5				
GXB_R3		GXB_RX_R21p,GXB_REFCLK_R21p					T4				
GXB_R3		GXB_RX_R21n,GXB_REFCLK_R21n					T3				
GXB_R3		GXB_TX_R21p					T8				
GXB_R3		GXB_TX_R21n					T7				
GXB_R3		GXB_RX_R22p,GXB_REFCLK_R22p					R2				
GXB_R3		GXB_RX_R22n,GXB_REFCLK_R22n					R1				
GXB_R3		GXB_TX_R22p					R6				
GXB_R3		GXB_TX_R22n					R5				
GXB_R3		GXB_RX_R23p,GXB_REFCLK_R23p					P4				
GXB_R3		GXB_RX_R23n,GXB_REFCLK_R23n					P3				
GXB_R3		GXB_TX_R23p					P8				
GXB_R3		GXB_TX_R23n					P7				
GXB_R3		REFCLK7Rn					W10				
GXB_R3		REFCLK7Rp					W11				
GXB_R4		REFCLK8Rn					U9				
GXB_R4		REFCLK8Rp					U10				
GXB_R4		GXB_RX_R24p,GXB_REFCLK_R24p					N2				
GXB_R4		GXB_RX_R24n,GXB_REFCLK_R24n					N1				
GXB_R4		GXB_TX_R24p					N6				
GXB_R4		GXB_TX_R24n					N5				
GXB_R4		GXB_RX_R25p,GXB_REFCLK_R25p					M4				
GXB_R4		GXB_RX_R25n,GXB_REFCLK_R25n					M3				
GXB_R4		GXB_TX_R25p					M8				
GXB_R4		GXB_TX_R25n					M7				
GXB_R4		GXB_RX_R26p,GXB_REFCLK_R26p					L2				
GXB_R4		GXB_RX_R26n,GXB_REFCLK_R26n					L1				
GXB_R4		GXB_TX_R26p					L6				
GXB_R4		GXB_TX_R26n					L5				
GXB_R4		GXB_RX_R27p,GXB_REFCLK_R27p					K4				
GXB_R4		GXB_RX_R27n,GXB_REFCLK_R27n					K3				
GXB_R4		GXB_TX_R27p					K8				
GXB_R4		GXB_TX_R27n					K7				
GXB_R4		GXB_RX_R28p,GXB_REFCLK_R28p					J2				
GXB_R4		GXB_RX_R28n,GXB_REFCLK_R28n					J1				
GXB_R4		GXB_TX_R28p					J6				
GXB_R4		GXB_TX_R28n					J5				
GXB_R4		GXB_RX_R29p,GXB_REFCLK_R29p					H4				
GXB_R4		GXB_RX_R29n,GXB_REFCLK_R29n					H3				
GXB_R4		GXB_TX_R29p					H8				
GXB_R4		GXB_TX_R29n					H7				
GXB_R4		REFCLK9Rn					R10				
GXB_R4		REFCLK9Rp					R11				
GXB_R5		REFCLK10Rn					N11				
GXB_R5		REFCLK10Rp					N10				
GXB_R5		GXB_RX_R30p,GXB_REFCLK_R30p					G2				
GXB_R5		GXB_RX_R30n,GXB_REFCLK_R30n					G1				
GXB_R5		GXB_TX_R30p					G6				
GXB_R5		GXB_TX_R30n					G5				
GXB_R5		GXB_RX_R31p,GXB_REFCLK_R31p					F4				
GXB_R5		GXB_RX_R31n,GXB_REFCLK_R31n					F3				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_R5		GXB_TX_R31p					F8				
GXB_R5		GXB_TX_R31n					F7				
GXB_R5		GXB_RX_R32p,GXB_REFCLK_R32p					E2				
GXB_R5		GXB_RX_R32n,GXB_REFCLK_R32n					E1				
GXB_R5		GXB_TX_R32p					E6				
GXB_R5		GXB_TX_R32n					E5				
7A		GND					M12				
7A	VREFB7AN0	IO	RZQ_4		DIFFIO_RX_T1p	DIFFOUT_T1p	E10	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	E9	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	C5	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	C4	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T3p	DIFFOUT_T3p	C7	DQS1T	DQS1T/CQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T3n	DIFFOUT_T3n	C6	DQSn1T	DQSn1T/DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	A3	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	A2	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T5p	DIFFOUT_T5p	C3	DQS2T	DQ1T/CQn1T	DQS1T/CQ1T	
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T5n	DIFFOUT_T5n	B3	DQSn2T	DQ1T	DQSn1T/DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B6	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	B5	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	C9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	C8	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	F11	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	E11	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T9p	DIFFOUT_T9p	D10	DQS3T	DQS2T/CQ2T	DQ1T/CQn1T	
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T9n	DIFFOUT_T9n	C10	DQSn3T	DQSn2T/DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	H12	DQ4T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	G12	DQ4T	DQ2T	DQ1T	
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T11p	DIFFOUT_T11p	G10	DQS4T	DQ2T/CQn2T	DQ1T	
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T11n	DIFFOUT_T11n	F10	DQSn4T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	J12	DQ4T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	J11	DQ4T	DQ2T	DQ1T	
7B	VREFB7BN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	L14	DQ7T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	L13	DQ7T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	L12	DQ7T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	K12	DQ7T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	M13	DQS7T	DQS3T/CQ3T		
7B	VREFB7BN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	N14	DQSn7T	DQSn3T/DQ3T		
7B	VREFB7BN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J13	DQ8T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	K14	DQ8T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	G13	DQS8T	DQ3T/CQn3T		
7B	VREFB7BN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	F13	DQSn8T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	M15	DQ8T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	L15	DQ8T	DQ3T		
7B	VREFB7BN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	R15	DQ9T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	P15	DQ9T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	R13	DQ9T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	P13	DQ9T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	T14	DQS9T	DQS4T/CQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	T13	DQSn9T	DQSn4T/DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	N16	DQ10T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	N15	DQ10T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	R14	DQS10T	DQ4T/CQn4T	DQS2T/CQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	T15	DQSn10T	DQ4T	DQSn2T/DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	R16	DQ10T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	P16	DQ10T	DQ4T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	B9	DQ11T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	B8	DQ11T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	E12	DQ11T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	D12	DQ11T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	E13	DQS11T	DQS5T/CQ5T	DQ2T/CQn2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	D13	DQSn11T	DQSn5T/DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	A6	DQ12T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A5	DQ12T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	B11	DQS12T	DQ5T/CQn5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	A11	DQSn12T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	A9	DQ12T	DQ5T	DQ2T	
7B	VREFB7BN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	A8	DQ12T	DQ5T	DQ2T	
7C	VREFB7CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	C13	DQ13T	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	C12	DQ13T	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	B12	DQ13T	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	A12	DQ13T	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	B14	DQS13T	DQS6T/CQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	A14	DQSn13T	DQSn6T/DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	D15	DQ14T	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	C15	DQ14T	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T41p	DIFFOUT_T41p	B15	DQS14T	DQ6T/CQn6T	DQS3T/CQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T41n	DIFFOUT_T41n	A15	DQSn14T	DQ6T	DQSn3T/DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	D16	DQ14T	DQ6T	DQ3T	DQ1T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7C	VREFB7CN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	C16	DQ14T	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	T17	DQ15T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	R17	DQ15T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	U16	DQ15T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	V17	DQ15T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	T18	DQS15T	DQS7T/CQ7T	DQ3T/CQn3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	R18	DQSn15T	DQSn7T/DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	P18	DQ16T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	N18	DQ16T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	M18	DQS16T	DQ7T/CQn7T	DQ3T	DQS1T/CQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	L18	DQSn16T	DQ7T	DQ3T	DQSn1T/DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	N17	DQ16T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	M17	DQ16T	DQ7T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T49p	DIFFOUT_T49p	J17	DQ17T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T49n	DIFFOUT_T49n	J16	DQ17T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	J15	DQ17T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	J14	DQ17T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	H16	DQS17T	DQS8T/CQ8T	DQ4T	DQ1T/CQn1T
7C	VREFB7CN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	H15	DQSn17T	DQSn8T/DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	L17	DQ18T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	L16	DQ18T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	J18	DQS18T	DQ8T/CQn8T	DQS4T/CQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	K17	DQSn18T	DQ8T	DQSn4T/DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	H18	DQ18T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	G18	DQ18T	DQ8T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	G15	DQ19T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	G14	DQ19T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	F14	DQ19T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E14	DQ19T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T57p	DIFFOUT_T57p	G16	DQS19T	DQS9T/CQ9T	DQ4T/CQn4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T57n	DIFFOUT_T57n	F16	DQSn19T	DQSn9T/DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	E16	DQ20T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	E15	DQ20T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	G17	DQS20T	DQ9T/CQn9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	F17	DQSn20T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	E18	DQ20T	DQ9T	DQ4T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	E17	DQ20T	DQ9T	DQ4T	DQ1T
7D	VREFB7DN0	IO			DIFFIO_RX_T61p	DIFFOUT_T61p	R19	DQ21T	DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_RX_T61n	DIFFOUT_T61n	P19	DQ21T	DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	N20	DQ21T	DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	N19	DQ21T	DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	T20	DQS21T	DQS10T/CQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	R20	DQSn21T	DQSn10T/DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	L19	DQ22T	DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	K19	DQ22T	DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	L20	DQS22T	DQ10T/CQn10T	DQS5T/CQ5T	
7D	VREFB7DN0	IO			DIFFIO_RX_T65n	DIFFOUT_T65n	K20	DQSn22T	DQ10T	DQSn5T/DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	M21	DQ22T	DQ10T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T66n	DIFFOUT_T66n	M20	DQ22T	DQ10T	DQ5T	
7D	VREFB7DN0	IO	CLK19p		DIFFIO_RX_T67p	DIFFOUT_T67p	B18	DQ23T	DQ11T	DQ5T	
7D	VREFB7DN0	IO	CLK19n		DIFFIO_RX_T67n	DIFFOUT_T67n	A18	DQ23T	DQ11T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	B17	DQ23T	DQ11T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	A17	DQ23T	DQ11T	DQ5T	
7D	VREFB7DN0	IO	CLK18p		DIFFIO_RX_T69p	DIFFOUT_T69p	C19	DQS23T	DQS11T/CQ11T	DQ5T/CQn5T	
7D	VREFB7DN0	IO	CLK18n		DIFFIO_RX_T69n	DIFFOUT_T69n	C18	DQSn23T	DQSn11T/DQ11T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	B20	DQ24T	DQ11T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_TX_T70n	DIFFOUT_T70n	A20	DQ24T	DQ11T	DQ5T	
7D	VREFB7DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T71p	DIFFOUT_T71p	C21	DQS24T	DQ11T/CQn11T	DQ5T	
7D	VREFB7DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T71n	DIFFOUT_T71n	C20	DQSn24T	DQ11T	DQ5T	
7D	VREFB7DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T72p	DIFFOUT_T72p	B21	DQ24T	DQ11T	DQ5T	
7D	VREFB7DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T72n	DIFFOUT_T72n	A21	DQ24T	DQ11T	DQ5T	
7D	VREFB7DN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	E21	DQ25T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	D21	DQ25T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	D18	DQ25T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	D19	DQ25T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	F19	DQS25T	DQS12T/CQ12T		
7D	VREFB7DN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	E19	DQSn25T	DQSn12T/DQ12T		
7D	VREFB7DN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	J19	DQ26T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	H19	DQ26T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	F20	DQS26T	DQ12T/CQn12T		
7D	VREFB7DN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	E20	DQSn26T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	G20	DQ26T	DQ12T		
7D	VREFB7DN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	G19	DQ26T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_RX_T127p	DIFFOUT_T127p	J21	DQ43T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_RX_T127n	DIFFOUT_T127n	H21	DQ43T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	G23	DQ43T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_TX_T128n	DIFFOUT_T128n	H22	DQ43T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_RX_T129p	DIFFOUT_T129p	F23	DQS43T	DQS13T/CQ13T		

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8D	VREFB8DN0	IO			DIFFIO_RX_T129n	DIFFOUT_T129n	F22	DQSn43T	DQSn13T/DQ13T		
8D	VREFB8DN0	IO			DIFFIO_TX_T130p	DIFFOUT_T130p	H24	DQ44T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_TX_T130n	DIFFOUT_T130n	G24	DQ44T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_RX_T131p	DIFFOUT_T131p	K23	DQS44T	DQ13T/CQn13T		
8D	VREFB8DN0	IO			DIFFIO_RX_T131n	DIFFOUT_T131n	J23	DQSn44T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_TX_T132p	DIFFOUT_T132p	H25	DQ44T	DQ13T		
8D	VREFB8DN0	IO			DIFFIO_TX_T132n	DIFFOUT_T132n	G25	DQ44T	DQ13T		
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T133p	DIFFOUT_T133p	E22	DQ45T	DQ14T	DQ6T	
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T133n	DIFFOUT_T133n	D22	DQ45T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T134p	DIFFOUT_T134p	E23	DQ45T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T134n	DIFFOUT_T134n	E24	DQ45T	DQ14T	DQ6T	
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T135p	DIFFOUT_T135p	C23	DQS45T	DQS14T/CQ14T	DQ6T	
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T135n	DIFFOUT_T135n	C22	DQSn45T	DQSn14T/DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T136p	DIFFOUT_T136p	D24	DQ46T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T136n	DIFFOUT_T136n	C24	DQ46T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T137p	DIFFOUT_T137p	B23	DQS46T	DQ14T/CQn14T	DQS6T/CQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T137n	DIFFOUT_T137n	A23	DQSn46T	DQ14T	DQSn6T/DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T138p	DIFFOUT_T138p	B24	DQ46T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T138n	DIFFOUT_T138n	A24	DQ46T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T139p	DIFFOUT_T139p	N22	DQ47T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T139n	DIFFOUT_T139n	N21	DQ47T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T140p	DIFFOUT_T140p	L21	DQ47T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T140n	DIFFOUT_T140n	L22	DQ47T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T141p	DIFFOUT_T141p	M23	DQS47T	DQS15T/CQ15T	DQ6T/CQn6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T141n	DIFFOUT_T141n	L23	DQSn47T	DQSn15T/DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T142p	DIFFOUT_T142p	P21	DQ48T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T142n	DIFFOUT_T142n	R21	DQ48T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T143p	DIFFOUT_T143p	N23	DQS48T	DQ15T/CQn15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T143n	DIFFOUT_T143n	P22	DQSn48T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T144p	DIFFOUT_T144p	R22	DQ48T	DQ15T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T144n	DIFFOUT_T144n	R23	DQ48T	DQ15T	DQ6T	
8C	VREFB8CN0	IO			DIFFIO_RX_T145p	DIFFOUT_T145p	R24	DQ49T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T145n	DIFFOUT_T145n	P24	DQ49T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T146p	DIFFOUT_T146p	T23	DQ49T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T146n	DIFFOUT_T146n	T24	DQ49T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T147p	DIFFOUT_T147p	V25	DQS49T	DQS16T/CQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T147n	DIFFOUT_T147n	U25	DQSn49T	DQSn16T/DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T148p	DIFFOUT_T148p	N24	DQ50T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T148n	DIFFOUT_T148n	M24	DQ50T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T149p	DIFFOUT_T149p	N25	DQS50T	DQ16T/CQn16T	DQS7T/CQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T149n	DIFFOUT_T149n	N26	DQSn50T	DQ16T	DQSn7T/DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T150p	DIFFOUT_T150p	R25	DQ50T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T150n	DIFFOUT_T150n	P25	DQ50T	DQ16T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T151p	DIFFOUT_T151p	F25	DQ51T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T151n	DIFFOUT_T151n	E25	DQ51T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T152p	DIFFOUT_T152p	G26	DQ51T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T152n	DIFFOUT_T152n	F26	DQ51T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T153p	DIFFOUT_T153p	D25	DQS51T	DQS17T/CQ17T	DQ7T/CQn7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T153n	DIFFOUT_T153n	C25	DQSn51T	DQSn17T/DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T154p	DIFFOUT_T154p	E27	DQ52T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T154n	DIFFOUT_T154n	E26	DQ52T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T155p	DIFFOUT_T155p	F28	DQS52T	DQ17T/CQn17T	DQ7T	DQS2T/CQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T155n	DIFFOUT_T155n	E28	DQSn52T	DQ17T	DQ7T	DQSn2T/DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T156p	DIFFOUT_T156p	D27	DQ52T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T156n	DIFFOUT_T156n	C27	DQ52T	DQ17T	DQ7T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T157p	DIFFOUT_T157p	K25	DQ53T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T157n	DIFFOUT_T157n	J25	DQ53T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T158p	DIFFOUT_T158p	L24	DQ53T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T158n	DIFFOUT_T158n	L25	DQ53T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T159p	DIFFOUT_T159p	M26	DQS53T	DQS18T/CQ18T	DQ8T	DQ2T/CQn2T
8C	VREFB8CN0	IO			DIFFIO_RX_T159n	DIFFOUT_T159n	L26	DQSn53T	DQSn18T/DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T160p	DIFFOUT_T160p	J27	DQ54T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T160n	DIFFOUT_T160n	H27	DQ54T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T161p	DIFFOUT_T161p	K26	DQS54T	DQ18T/CQn18T	DQS8T/CQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T161n	DIFFOUT_T161n	J26	DQSn54T	DQ18T	DQSn8T/DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T162p	DIFFOUT_T162p	H28	DQ54T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T162n	DIFFOUT_T162n	G28	DQ54T	DQ18T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T163p	DIFFOUT_T163p	B26	DQ55T	DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T163n	DIFFOUT_T163n	A26	DQ55T	DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T164p	DIFFOUT_T164p	D28	DQ55T	DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T164n	DIFFOUT_T164n	C28	DQ55T	DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T165p	DIFFOUT_T165p	B27	DQS55T	DQS19T/CQ19T	DQ8T/CQn8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T165n	DIFFOUT_T165n	A27	DQSn55T	DQSn19T/DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T166p	DIFFOUT_T166p	B29	DQ56T	DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T166n	DIFFOUT_T166n	A29	DQ56T	DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T167p	DIFFOUT_T167p	D30	DQS56T	DQ19T/CQn19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T167n	DIFFOUT_T167n	C30	DQSn56T	DQ19T	DQ8T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T168p	DIFFOUT_T168p	B30	DQ56T	DQ19T	DQ8T	DQ2T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8C	VREFB8CN0	IO			DIFFIO_TX_T168n	DIFFOUT_T168n	A30	DQ56T	DQ19T	DQ8T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T169p	DIFFOUT_T169p	L27	DQ57T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T169n	DIFFOUT_T169n	L28	DQ57T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T170p	DIFFOUT_T170p	K28	DQ57T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T170n	DIFFOUT_T170n	J28	DQ57T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T171p	DIFFOUT_T171p	H30	DQS57T	DQS20T/CQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T171n	DIFFOUT_T171n	J29	DQSn57T	DQSn20T/DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T172p	DIFFOUT_T172p	G29	DQ58T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T172n	DIFFOUT_T172n	F29	DQ58T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T173p	DIFFOUT_T173p	E31	DQS58T	DQ20T/CQn20T	DQS9T/CQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T173n	DIFFOUT_T173n	D31	DQSn58T	DQ20T	DQSn9T/DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T174p	DIFFOUT_T174p	E29	DQ58T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T174n	DIFFOUT_T174n	E30	DQ58T	DQ20T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T175p	DIFFOUT_T175p	T27	DQ59T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T175n	DIFFOUT_T175n	R27	DQ59T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T176p	DIFFOUT_T176p	T26	DQ59T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T176n	DIFFOUT_T176n	R26	DQ59T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T177p	DIFFOUT_T177p	U27	DQS59T	DQS21T/CQ21T	DQ9T/CQn9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T177n	DIFFOUT_T177n	U28	DQSn59T	DQSn21T/DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T178p	DIFFOUT_T178p	T29	DQ60T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T178n	DIFFOUT_T178n	T30	DQ60T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T179p	DIFFOUT_T179p	P27	DQS60T	DQ21T/CQn21T	DQ9T	DQS3T/CQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T179n	DIFFOUT_T179n	P28	DQSn60T	DQ21T	DQ9T	DQSn3T/DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T180p	DIFFOUT_T180p	R28	DQ60T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T180n	DIFFOUT_T180n	R29	DQ60T	DQ21T	DQ9T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T181p	DIFFOUT_T181p	B32	DQ61T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T181n	DIFFOUT_T181n	C31	DQ61T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T182p	DIFFOUT_T182p	A32	DQ61T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T182n	DIFFOUT_T182n	A33	DQ61T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T183p	DIFFOUT_T183p	C33	DQS61T	DQS22T/CQ22T	DQ10T	DQ3T/CQn3T
8B	VREFB8BN0	IO			DIFFIO_RX_T183n	DIFFOUT_T183n	B33	DQSn61T	DQSn22T/DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T184p	DIFFOUT_T184p	B36	DQ62T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T184n	DIFFOUT_T184n	A36	DQ62T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T185p	DIFFOUT_T185p	B35	DQS62T	DQ22T/CQn22T	DQS10T/CQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T185n	DIFFOUT_T185n	A35	DQSn62T	DQ22T	DQSn10T/DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T186p	DIFFOUT_T186p	C34	DQ62T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T186n	DIFFOUT_T186n	C35	DQ62T	DQ22T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T187p	DIFFOUT_T187p	N27	DQ63T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T187n	DIFFOUT_T187n	M27	DQ63T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T188p	DIFFOUT_T188p	N28	DQ63T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T188n	DIFFOUT_T188n	N29	DQ63T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T189p	DIFFOUT_T189p	P30	DQS63T	DQS23T/CQ23T	DQ10T/CQn10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T189n	DIFFOUT_T189n	N30	DQSn63T	DQSn23T/DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T190p	DIFFOUT_T190p	M29	DQ64T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T190n	DIFFOUT_T190n	M30	DQ64T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T191p	DIFFOUT_T191p	L29	DQS64T	DQ23T/CQn23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T191n	DIFFOUT_T191n	K29	DQSn64T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T192p	DIFFOUT_T192p	L30	DQ64T	DQ23T	DQ10T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T192n	DIFFOUT_T192n	L31	DQ64T	DQ23T	DQ10T	DQ3T
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T193p	DIFFOUT_T193p	B38	DQ65T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T193n	DIFFOUT_T193n	A38	DQ65T	DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T194p	DIFFOUT_T194p	A40	DQ65T	DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T194n	DIFFOUT_T194n	A41	DQ65T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T195p	DIFFOUT_T195p	C40	DQS65T	DQS24T/CQ24T	DQ11T	
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T195n	DIFFOUT_T195n	B40	DQSn65T	DQSn24T/DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T196p	DIFFOUT_T196p	C36	DQ66T	DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T196n	DIFFOUT_T196n	C37	DQ66T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T197p	DIFFOUT_T197p	D34	DQS66T	DQ24T/CQn24T	DQS11T/CQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T197n	DIFFOUT_T197n	D35	DQSn66T	DQ24T	DQSn11T/DQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T198p	DIFFOUT_T198p	C38	DQ66T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T198n	DIFFOUT_T198n	C39	DQ66T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T199p	DIFFOUT_T199p	J32	DQ67T	DQ25T	DQ11T	
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T199n	DIFFOUT_T199n	K31	DQ67T	DQ25T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T200p	DIFFOUT_T200p	J31	DQ67T	DQ25T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T200n	DIFFOUT_T200n	H31	DQ67T	DQ25T	DQ11T	
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T201p	DIFFOUT_T201p	G31	DQS67T	DQS25T/CQ25T	DQ11T/CQn11T	
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T201n	DIFFOUT_T201n	F31	DQSn67T	DQSn25T/DQ25T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T202p	DIFFOUT_T202p	E33	DQ68T	DQ25T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T202n	DIFFOUT_T202n	D33	DQ68T	DQ25T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_RX_T203p	DIFFOUT_T203p	F32	DQS68T	DQ25T/CQn25T	DQ11T	
8A	VREFB8AN0	IO	RZQ_5		DIFFIO_RX_T203n	DIFFOUT_T203n	E32	DQSn68T	DQ25T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T204p	DIFFOUT_T204p	G32	DQ68T	DQ25T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T204n	DIFFOUT_T204n	G33	DQ68T	DQ25T	DQ11T	
		GND					AA35				
		GND					AA36				
		GND					AA39				
		GND					AA40				
		GND					AB32				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AB34				
		GND					AB37				
		GND					AB38				
		GND					AB41				
		GND					AB42				
		GND					AC31				
		GND					AC35				
		GND					AC36				
		GND					AC39				
		GND					AC40				
		GND					AD33				
		GND					AD37				
		GND					AD38				
		GND					AD41				
		GND					AD42				
		GND					AE35				
		GND					AE36				
		GND					AE39				
		GND					AE40				
		GND					AF31				
		GND					AF32				
		GND					AF34				
		GND					AF37				
		GND					AF38				
		GND					AF41				
		GND					AF42				
		GND					AG35				
		GND					AG36				
		GND					AG39				
		GND					AG40				
		GND					AH33				
		GND					AH37				
		GND					AH38				
		GND					AH41				
		GND					AH42				
		GND					AJ31				
		GND					AJ35				
		GND					AJ36				
		GND					AJ39				
		GND					AJ40				
		GND					AK32				
		GND					AK34				
		GND					AK37				
		GND					AK38				
		GND					AK41				
		GND					AK42				
		GND					AL31				
		GND					AL35				
		GND					AL36				
		GND					AL39				
		GND					AL40				
		GND					AM31				
		GND					AM33				
		GND					AM37				
		GND					AM38				
		GND					AM41				
		GND					AM42				
		GND					AN31				
		GND					AN35				
		GND					AN36				
		GND					AN39				
		GND					AN40				
		GND					AP32				
		GND					AP34				
		GND					AP37				
		GND					AP38				
		GND					AP41				
		GND					AP42				
		GND					AR33				
		GND					AR34				
		GND					AR35				
		GND					AR36				
		GND					AR39				
		GND					AR40				
		GND					AT34				
		GND					AT37				
		GND					AT38				
		GND					AT41				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AT42				
		GND					AU35				
		GND					AU36				
		GND					AU39				
		GND					AU40				
		GND					AV37				
		GND					AV38				
		GND					AV41				
		GND					AV42				
		GND					AW41				
		GND					AY41				
		GND					AY42				
		GND					B41				
		GND					B42				
		GND					C41				
		GND					D37				
		GND					D38				
		GND					D41				
		GND					D42				
		GND					E35				
		GND					E36				
		GND					E39				
		GND					E40				
		GND					F34				
		GND					F37				
		GND					F38				
		GND					F41				
		GND					F42				
		GND					G35				
		GND					G36				
		GND					G39				
		GND					G40				
		GND					H34				
		GND					H37				
		GND					H38				
		GND					H41				
		GND					H42				
		GND					J35				
		GND					J36				
		GND					J39				
		GND					J40				
		GND					K33				
		GND					K34				
		GND					K37				
		GND					K38				
		GND					K41				
		GND					K42				
		GND					L32				
		GND					L35				
		GND					L36				
		GND					L39				
		GND					L40				
		GND					M32				
		GND					M37				
		GND					M38				
		GND					M41				
		GND					M42				
		GND					N34				
		GND					N35				
		GND					N36				
		GND					N39				
		GND					N40				
		GND					P32				
		GND					P34				
		GND					P37				
		GND					P38				
		GND					P41				
		GND					P42				
		GND					R31				
		GND					R35				
		GND					R36				
		GND					R39				
		GND					R40				
		GND					T31				
		GND					T33				
		GND					T37				
		GND					T38				
		GND					T41				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					T42				
		GND					U31				
		GND					U35				
		GND					U36				
		GND					U39				
		GND					U40				
		GND					V32				
		GND					V34				
		GND					V37				
		GND					V38				
		GND					V41				
		GND					V42				
		GND					W31				
		GND					W35				
		GND					W36				
		GND					W39				
		GND					W40				
		GND					Y31				
		GND					Y33				
		GND					Y37				
		GND					Y38				
		GND					Y41				
		GND					Y42				
		GND					AA3				
		GND					AA4				
		GND					AA7				
		GND					AA8				
		GND					AB1				
		GND					AB11				
		GND					AB2				
		GND					AB5				
		GND					AB6				
		GND					AB9				
		GND					AC12				
		GND					AC3				
		GND					AC4				
		GND					AC7				
		GND					AC8				
		GND					AD1				
		GND					AD10				
		GND					AD2				
		GND					AD5				
		GND					AD6				
		GND					AE3				
		GND					AE4				
		GND					AE7				
		GND					AE8				
		GND					AF1				
		GND					AF11				
		GND					AF12				
		GND					AF2				
		GND					AF5				
		GND					AF6				
		GND					AF9				
		GND					AG3				
		GND					AG4				
		GND					AG7				
		GND					AG8				
		GND					AH1				
		GND					AH10				
		GND					AH2				
		GND					AH5				
		GND					AH6				
		GND					AJ12				
		GND					AJ3				
		GND					AJ4				
		GND					AJ7				
		GND					AJ8				
		GND					AK1				
		GND					AK11				
		GND					AK2				
		GND					AK5				
		GND					AK6				
		GND					AK9				
		GND					AL12				
		GND					AL3				
		GND					AL4				
		GND					AL7				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AL8				
		GND					AM1				
		GND					AM10				
		GND					AM12				
		GND					AM2				
		GND					AM5				
		GND					AM6				
		GND					AN12				
		GND					AN3				
		GND					AN4				
		GND					AN7				
		GND					AN8				
		GND					AP1				
		GND					AP11				
		GND					AP2				
		GND					AP5				
		GND					AP6				
		GND					AP9				
		GND					AR10				
		GND					AR3				
		GND					AR4				
		GND					AR7				
		GND					AR8				
		GND					AR9				
		GND					AT1				
		GND					AT2				
		GND					AT5				
		GND					AT6				
		GND					AT9				
		GND					AU3				
		GND					AU4				
		GND					AU7				
		GND					AU8				
		GND					AV1				
		GND					AV2				
		GND					AV5				
		GND					AV6				
		GND					AW2				
		GND					AY1				
		GND					AY2				
		GND					B1				
		GND					B2				
		GND					C2				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					D6				
		GND					E3				
		GND					E4				
		GND					E7				
		GND					E8				
		GND					F1				
		GND					F2				
		GND					F5				
		GND					F6				
		GND					F9				
		GND					G3				
		GND					G4				
		GND					G7				
		GND					G8				
		GND					H1				
		GND					H2				
		GND					H5				
		GND					H6				
		GND					H9				
		GND					J3				
		GND					J4				
		GND					J7				
		GND					J8				
		GND					K1				
		GND					K10				
		GND					K2				
		GND					K5				
		GND					K6				
		GND					K9				
		GND					L11				
		GND					L3				
		GND					L4				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					L7				
		GND					L8				
		GND					M1				
		GND					M11				
		GND					M2				
		GND					M5				
		GND					M6				
		GND					N3				
		GND					N4				
		GND					N7				
		GND					N8				
		GND					N9				
		GND					P1				
		GND					P11				
		GND					P2				
		GND					P5				
		GND					P6				
		GND					P9				
		GND					R12				
		GND					R3				
		GND					R4				
		GND					R7				
		GND					R8				
		GND					T1				
		GND					T10				
		GND					T12				
		GND					T2				
		GND					T5				
		GND					T6				
		GND					U12				
		GND					U3				
		GND					U4				
		GND					U7				
		GND					U8				
		GND					V1				
		GND					V11				
		GND					V2				
		GND					V5				
		GND					V6				
		GND					V9				
		GND					W12				
		GND					W3				
		GND					W4				
		GND					W7				
		GND					W8				
		GND					Y1				
		GND					Y10				
		GND					Y12				
		GND					Y2				
		GND					Y5				
		GND					Y6				
		GND					AA14				
		GND					AA16				
		GND					AA18				
		GND					AA20				
		GND					AA23				
		GND					AA25				
		GND					AA26				
		GND					AA28				
		GND					AA29				
		GND					AB13				
		GND					AB15				
		GND					AB19				
		GND					AB24				
		GND					AB27				
		GND					AB30				
		GND					AC14				
		GND					AC16				
		GND					AC18				
		GND					AC20				
		GND					AC23				
		GND					AC26				
		GND					AC28				
		GND					AD13				
		GND					AD30				
		GND					AE14				
		GND					AE16				
		GND					AE19				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AE21				
		GND					AE23				
		GND					AE25				
		GND					AE27				
		GND					AE29				
		GND					AG14				
		GND					AG17				
		GND					AG20				
		GND					AG23				
		GND					AG26				
		GND					AG29				
		GND					AJ15				
		GND					AJ18				
		GND					AJ21				
		GND					AJ24				
		GND					AJ27				
		GND					AJ30				
		GND					AK12				
		GND					AK31				
		GND					AL13				
		GND					AL16				
		GND					AL19				
		GND					AL22				
		GND					AL25				
		GND					AL28				
		GND					AN14				
		GND					AN17				
		GND					AN20				
		GND					AN23				
		GND					AN26				
		GND					AN29				
		GND					AR11				
		GND					AR15				
		GND					AR18				
		GND					AR21				
		GND					AR24				
		GND					AR27				
		GND					AR30				
		GND					AR32				
		GND					AT12				
		GND					AU13				
		GND					AU16				
		GND					AU19				
		GND					AU22				
		GND					AU25				
		GND					AU28				
		GND					AU31				
		GND					AV10				
		GND					AV3				
		GND					AV34				
		GND					AV39				
		GND					AV4				
		GND					AV40				
		GND					AW11				
		GND					AW14				
		GND					AW17				
		GND					AW20				
		GND					AW23				
		GND					AW26				
		GND					AW29				
		GND					AW32				
		GND					AY35				
		GND					AY5				
		GND					AY8				
		GND					B10				
		GND					B13				
		GND					B16				
		GND					B19				
		GND					B22				
		GND					B25				
		GND					B28				
		GND					B31				
		GND					B34				
		GND					B37				
		GND					B39				
		GND					B4				
		GND					B7				
		GND					BA12				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					BA15				
		GND					BA18				
		GND					BA21				
		GND					BA24				
		GND					BA27				
		GND					BA3				
		GND					BA30				
		GND					BA33				
		GND					BA36				
		GND					BA38				
		GND					BA40				
		GND					BA6				
		GND					BA9				
		GND					D11				
		GND					D14				
		GND					D17				
		GND					D20				
		GND					D23				
		GND					D26				
		GND					D29				
		GND					D3				
		GND					D32				
		GND					D36				
		GND					D39				
		GND					D4				
		GND					D40				
		GND					D9				
		GND					E34				
		GND					F12				
		GND					F15				
		GND					F18				
		GND					F21				
		GND					F24				
		GND					F27				
		GND					F30				
		GND					F33				
		GND					G34				
		GND					G9				
		GND					H11				
		GND					H14				
		GND					H17				
		GND					H20				
		GND					H23				
		GND					H26				
		GND					H29				
		GND					H32				
		GND					J34				
		GND					J9				
		GND					K13				
		GND					K15				
		GND					K18				
		GND					K21				
		GND					K24				
		GND					K27				
		GND					K30				
		GND					M14				
		GND					M16				
		GND					M19				
		GND					M22				
		GND					M25				
		GND					M28				
		GND					M31				
		GND					N12				
		GND					N31				
		GND					P14				
		GND					P17				
		GND					P20				
		GND					P23				
		GND					P26				
		GND					P29				
		GND					P31				
		GND					T16				
		GND					T19				
		GND					T22				
		GND					T25				
		GND					T28				
		GND					U14				
		GND					U17				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					U19				
		GND					U21				
		GND					U23				
		GND					U26				
		GND					U29				
		GND					V12				
		GND					V13				
		GND					V15				
		GND					V20				
		GND					V22				
		GND					V24				
		GND					V27				
		GND					V30				
		GND					V31				
		GND					W14				
		GND					W16				
		GND					W18				
		GND					W23				
		GND					W26				
		GND					W28				
		GND					W29				
		GND					Y13				
		GND					Y15				
		GND					Y17				
		GND					Y19				
		GND					Y21				
		GND					Y24				
		GND					Y27				
		GND					Y30				
		GND					AC22				
		VCC					AE18				
		VCC					AE20				
		VCC					AE22				
		VCC					AE24				
		VCC					U18				
		VCC					U20				
		VCC					U22				
		VCC					U24				
		VCC					AA17				
		VCC					AA19				
		VCC					AA21				
		VCC					AA22				
		VCC					AA24				
		VCC					AB17				
		VCC					AB18				
		VCC					AB20				
		VCC					AB23				
		VCC					AB25				
		VCC					AC19				
		VCC					AC21				
		VCC					AC24				
		VCC					AD18				
		VCC					AD19				
		VCC					AD20				
		VCC					AD21				
		VCC					AD22				
		VCC					AD23				
		VCC					AD24				
		VCC					V18				
		VCC					V19				
		VCC					V21				
		VCC					V23				
		VCC					W17				
		VCC					W19				
		VCC					W20				
		VCC					W21				
		VCC					W22				
		VCC					W24				
		VCC					W25				
		VCC					Y18				
		VCC					Y20				
		VCC					Y22				
		VCC					Y23				
		VCC					Y25				
		VCC					AB21				
		VCCPT					AF21				
		VCCPT					AF30				
		VCCPT					AH14				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCPT					N13				
		VCCPT					R30				
		VCCPT					T21				
		DNU					BA41				
		DNU					BA42				
		DNU					AN30				
		DNU					AU21				
		DNU					BA1				
		DNU					BA2				
		DNU					P12				
		DNU					G22				
		DNU					AB22				
		VCCPGM					AP31				
		VCCPGM					AP12				
		TEMPDIODEn					D7				
		TEMPDIODEp					D8				
		VCCBAT					AN13				
		VCCIO3A					BA37				
		VCCIO3A					BA39				
		VCCIO3B					BA35				
		VCCIO3B					BB33				
		VCCIO3C					BB27				
		VCCIO3C					BB30				
		VCCIO3D					BB21				
		VCCIO3D					BB24				
		VCCIO4A					BB6				
		VCCIO4B					BB9				
		VCCIO4C					AY14				
		VCCIO4C					BB12				
		VCCIO4D					BB15				
		VCCIO4D					BB18				
		VCCIO7A					A4				
		VCCIO7B					A10				
		VCCIO7B					A7				
		VCCIO7C					A13				
		VCCIO7C					C14				
		VCCIO7D					A16				
		VCCIO7D					A19				
		VCCIO8A					A39				
		VCCIO8B					A34				
		VCCIO8B					A37				
		VCCIO8C					A28				
		VCCIO8C					A31				
		VCCIO8D					A22				
		VCCIO8D					A25				
		VCCPD3AB					AY29				
		VCCPD3AB					AY32				
		VCCPD3CD					AY23				
		VCCPD3CD					AY26				
		VCCPD4					AY11				
		VCCPD4					AY17				
		VCCPD7					C11				
		VCCPD7					C17				
		VCCPD8					C26				
		VCCPD8					C29				
		VCCPD8					C32				
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AT31				
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AT29				
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AR26				
3D	VREFB3DN0	VREFB3DN0	VREFB3DN0				AP23				
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AT11				
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AT14				
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AT16				
4D	VREFB4DN0	VREFB4DN0	VREFB4DN0				AP19				
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G11				
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H13				
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				K16				
7D	VREFB7DN0	VREFB7DN0	VREFB7DN0				J20				
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				J30				
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				G30				
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G27				
8D	VREFB8DN0	VREFB8DN0	VREFB8DN0				J24				
		VCCH_GXBL0					AM34				
		VCCH_GXBL1					AH34				
		VCCH_GXBL2					AD34				
		VCCH_GXBL3					Y34				
		VCCH_GXBL4					T34				
		VCCH_GXBL5					M34				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCH_GXBR0					AM9				
		VCCH_GXBR1					AH9				
		VCCH_GXBR2					AD9				
		VCCH_GXBR3					Y9				
		VCCH_GXBR4					T9				
		VCCH_GXBR5					M9				
		VCCR_GXBL0					AP33				
		VCCR_GXBL1					AK33				
		VCCR_GXBL2					AF33				
		VCCR_GXBL3					AB33				
		VCCR_GXBL4					V33				
		VCCR_GXBL5					P33				
		VCCR_GXBR0					AP10				
		VCCR_GXBR1					AK10				
		VCCR_GXBR2					AF10				
		VCCR_GXBR3					AB10				
		VCCR_GXBR4					V10				
		VCCR_GXBR5					P10				
		VCCT_GXBL0					AM32				
		VCCT_GXBL0					AN32				
		VCCT_GXBL1					AH32				
		VCCT_GXBL1					AJ32				
		VCCT_GXBL2					AD32				
		VCCT_GXBL2					AE32				
		VCCT_GXBL3					AA32				
		VCCT_GXBL3					Y32				
		VCCT_GXBL4					T32				
		VCCT_GXBL4					U32				
		VCCT_GXBL5					L33				
		VCCT_GXBL5					M33				
		VCCT_GXBR0					AM11				
		VCCT_GXBR0					AN11				
		VCCT_GXBR1					AH11				
		VCCT_GXBR1					AJ11				
		VCCT_GXBR2					AD11				
		VCCT_GXBR2					AE11				
		VCCT_GXBR3					AA11				
		VCCT_GXBR3					Y11				
		VCCT_GXBR4					T11				
		VCCT_GXBR4					U11				
		VCCT_GXBR5					L10				
		VCCT_GXBR5					M10				
		VCCHIP_L					AA27				
		VCCHIP_L					AB26				
		VCCHIP_L					AB28				
		VCCHIP_L					AC27				
		VCCHIP_L					V26				
		VCCHIP_L					V28				
		VCCHIP_L					W27				
		VCCHIP_L					Y26				
		VCCHIP_L					Y28				
		VCCHIP_R					AA15				
		VCCHIP_R					AB16				
		VCCHIP_R					AC15				
		VCCHIP_R					AD14				
		VCCHIP_R					AD16				
		VCCHIP_R					U15				
		VCCHIP_R					V16				
		VCCHIP_R					W15				
		VCCHIP_R					Y16				
		RREF_BL					AW42				
		RREF_BR					AW1				
		RREF_TL					C42				
		RREF_TR					C1				
		VCCA_FPLL					AT33				
		VCCA_FPLL					AN22				
		VCCA_FPLL					AT10				
		VCCA_FPLL					J10				
		VCCA_FPLL					K22				
		VCCA_FPLL					J33				
		VCCA_FPLL					AA31				
		VCCA_FPLL					AD31				
		VCCA_FPLL					AG31				
		VCCA_FPLL					AA12				
		VCCA_FPLL					AD12				
		VCCA_FPLL					AG12				
		VCCA_GXBL0					AL34				
		VCCA_GXBL1					AG34				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCA_GXBL2					AC34				
		VCCA_GXBL3					W34				
		VCCA_GXBL4					R34				
		VCCA_GXBL5					L34				
		VCCA_GXBR0					AL9				
		VCCA_GXBR1					AG9				
		VCCA_GXBR2					AC9				
		VCCA_GXBR3					W9				
		VCCA_GXBR4					R9				
		VCCA_GXBR5					L9				
		VCCHSSI_L					AA30				
		VCCHSSI_L					AB29				
		VCCHSSI_L					AC30				
		VCCHSSI_L					AE30				
		VCCHSSI_L					U30				
		VCCHSSI_L					V29				
		VCCHSSI_L					W30				
		VCCHSSI_L					Y29				
		VCCHSSI_R					AA13				
		VCCHSSI_R					AB14				
		VCCHSSI_R					AC13				
		VCCHSSI_R					AE13				
		VCCHSSI_R					U13				
		VCCHSSI_R					V14				
		VCCHSSI_R					W13				
		VCCHSSI_R					Y14				
		VCCD_FPLL					AU33				
		VCCD_FPLL					AP22				
		VCCD_FPLL					AU10				
		VCCD_FPLL					H10				
		VCCD_FPLL					J22				
		VCCD_FPLL					H33				
		VCCD_FPLL					AB31				
		VCCD_FPLL					AE31				
		VCCD_FPLL					AH31				
		VCCD_FPLL					AB12				
		VCCD_FPLL					AE12				
		VCCD_FPLL					AH12				
		VCC_AUX					AM30				
		VCC_AUX					AP13				
		VCC_AUX					AT21				
		VCC_AUX					G21				
		VCC_AUX					K11				
		VCC_AUX					K32				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the
Stratix V Device Family Pin Connection Guidelines.
(2) The GXB_REFCLK pin is not supported in the current Quartus II software version, but will be supported in the future Quartus II software release version.

Pin Information for the Stratix® V 5SGXB9 Device
Version 1.0

Version Number	Date	Changes Made
1.0	4/3/2012	Initial release.