Sub-Bank	Package Name	Index within I/O Bank	Index within I/O Sub-Bank	DDR3 Scheme 1: Component/UDIMM/SODIMM	DDR3 Scheme 2: Component/UDIMM/SODIMM. Used for HPS-EMIF	DDR3 Scheme 3: RDIMM	DDR3 AC_LANE_0_1_2 RDIMM	DDR3 Scheme 5: LRDIMM	DDR4 Scheme 1: Component and DIMM (Supports Ping pong; Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	DDR4 Scheme 2: Component and DIMM (Supports up to 2 ranks for UDIMM/RDIMM/SO-DIMM/Component). Used for HPS EMIF	DDR4 Scheme 3: Component and DIMM, with 3DS (Support 3DS; Supports Ping pong; Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	LPDDR3 Scheme 1	LPDDR3 Scheme 2	RLDRAM3 Scheme 1	QDR-IV Scheme 1	QDR-IV Scheme 2	RLDRAMII Scheme 1	QDRII/II+/II+ Xtreme Scheme 1
Lane 3	LVDSXX_1N	47	11		Not used by Address/Command pins in this scheme; usable as Data pins. In HPS mode, ECC pins must be placed here.	CK_N_1	Not used by Address/Command pins in this scheme; usable as Data pins	CK_N_1	CK_N_1	Not used by Address/Command pins in this scheme; usable as Data pins. In HPS mode, ECC pins must be placed here.	CK_N_1	Not used by Address/Command pins in this scheme; usable as Data pins	Not used by Address/Command or Data Pins			Not used by Address/Command or Data Pins	Not used by Address/Command or Data Pins	Not used by Address/Command or Data Pins
	LVDSXX_1P	46	10			CK_1		CK_1	CK_1		CK_1							
	LVDSXX_2N	45	9	CK_N_3					CK_N_3									
	LVDSXX_2P	44	8	CK_3					CK_3									
	LVDSXX_3N	43	7	CK_N_2					CK_N_2		CS_3							
	LVDSXX_3P	42	6	CK_2					CK_2		CS_2							
	LVDSXX_4N	41	5	CKE_3		CKE_3			CKE_3		CKE_3							
	LVDSXX_4P	40	4	CKE_2		CKE_2			CKE_2		CKE_2				PE_N_0			
	LVDSXX_5N	39	3	ODT_3		ODT_3		RM_1	ODT_3		ODT_3				AP_0			
	LVDSXX_5P	38	2	ODT_2		ODT_2		RM_0	ODT_2		ODT_2				A_24			
	LVDSXX_6N	37	1	CS_N_3		CS_N_3		CS_N_3	CS_N_3		C_1				A_23			
	LVDSXX_6P	36	0	CS_N_2		CS_N_2		CS_N_2	CS_N_2		C_0				A_22			
Lane 2	LVDSXX_7N	35	11	BA_2	BA_2	BA_2	BA_2	BA_2	BG_0	BG_0	BG_0		CK_N_3	BA_2	A_21	A_21	A_22	A_22
	LVDSXX_7P	34	10	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1		CK_3	BA_1	A_20	A_20	A_21	A_21
	LVDSXX_8N	33	9	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0		CK_N_2	BA_0	A_19	A_19	A_20	A_20
	LVDSXX_8P	32	8	CAS_N_0	CAS_N_0	CAS_N_0	CAS_N_0	CAS_N_0	A_17	A_17	A_17		CK_2	A_17	A_18	A_18	A_19	A_19
	LVDSXX_9N	31	7	RAS_N_0	RAS_N_0	RAS_N_0	RAS_N_0	RAS_N_0	A_16	A_16	A_16			A_16	A_17	A_17	A_18	A_18
	LVDSXX_9P	30	6	A_15	A_15	A_15	A_15	A_15	A_15	A_15	A_15		CKE_3	A_15	A_16	A_16	A_17	A_17
	LVDSXX_10N	29	5	A_14	A_14	A_14	A_14	A_14	A_14	A_14	A_14		CKE_2	A_14	A_15	A_15	A_16	A_16
	LVDSXX_10P	28	4	A_13	A_13	A_13	A_13	A_13	A_13	A_13	A_13		ODT_3	A_13	A_14	A_14	A_15	A_15
	LVDSXX_11N	27	3	A_12	A_12	A_12	A_12	A_12	A_12	A_12	A_12		ODT_2	A_12	A_13	A_13	A_14	A_14
	LVDSXX_11P	26	2	Recommended RZQ Site														
	LVDSXX_12N	25	1	Recommended Differential "N-Side" Reference Clock Input Site (LVDS Reference Clock Only)														
	LVDSXX_12P	24	0	Recommended Single-Ended or Differential "P-Side" PLL Reference Clock Input Site														
Lane 1	LVDSXX_13N	23	11	A_11	A_11	A_11	A_11	A_11	A_11	A_11	A_11			A_11	A_12	A_12	A_13	A_13
	LVDSXX_13P	22	10	A_10	A_10	A_10	A_10	A_10	A_10	A_10	A_10			A_10	A_11	A_11	A_12	A_12
	LVDSXX_14N	21	9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_10	A_10	A_11	A_11
	LVDSXX_14P	20	8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_9	A_9	A_10	A_10
	LVDSXX_15N	19	7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_8	A_8	A_9	A_9
	LVDSXX_15P	18	6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_7	A_7	A_8	A_8
	LVDSXX_16N	17	5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_6	A_6	A_7	A_7
	LVDSXX_16P	16	4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_5	A_5	A_6	A_6
	LVDSXX_17N	15	3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_4	A_4	A_5	A_5
	LVDSXX_17P	14	2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_3	A_3	A_4	A_4
	LVDSXX_18N	13	1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_2	A_2	A_3	A_3
	LVDSXX_18P	12	0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_1	A_1	A_2	A_2
Lane 0	LVDSXX_19N	11	11	CK_N_1	CK_N_1	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	CK_N_1	CK_N_1	REF_N_0	A_0	A_0	A_1	A_1
	LVDSXX_19P	10	10	CK_1	CK_1	ALERT_N_0	ALERT_N_0	ALERT_N_0	CS_N_1	CS_N_1	CS_N_1	CK_1	CK_1		AINV_0	AINV_0	A_0	A_0
	LVDSXX_20N	9	9	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	
	LVDSXX_20P	8	8	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	
	LVDSXX_21N	7	7	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	WE_N_0	RWB_N_0	RWB_N_0	REF_N_0	RPS_N_0
	LVDSXX_21P	6	6	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	A_20	RWA_N_0	RWA_N_0	WE_N_0	WPS_N_0
	LVDSXX_22N	5	5	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	A_19	LDB_N_0	LDB_N_0	CS_N_0	DOFF_N_0
	LVDSXX_22P	4	4	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	A_18	LDA_N_0	LDA_N_0	BA_2	
	LVDSXX_23N	3	3	CS_N_1	CS_N_1	CS_N_1	CS_N_1	CS_N_1	ACT_N_0	ACT_N_0	ACT_N_0	CS_N_1	CS_N_1	CS_N_1	LBK1_N_0	LBK1_N_0	BA_1		
	LVDSXX_23P	2	2	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	LBK0_N_0	LBK0_N_0	BA_0		
	LVDSXX_24N	1	1	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0		CS_N_3	RESET_N_0	RESET_N_0	RESET_N_0			
	LVDSXX_24P	0	0	WE_N_0	WE_N_0	WE_N_0	WE_N_0	WE_N_0	BG_1	BG_1	BG_1		CS_N_2	BA_3	CFG_N_0	CFG_N_0			

Date	Version	Changes
July 2017	2017.07.26	Initial release.
January 2018	2018.01.15	The external memory interface pin information is applicable for both Intel Stratix 10 ES and production devices.
October 2018	2018.10.23	Added the Sub-Bank, Package Name, and Index within I/O Sub-Bank columns.