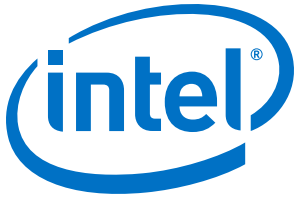

Intel® Stratix® 10 Device Family Pin Connection Guidelines

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Contents

Intel® Stratix® 10 Device Family Pin Connection Guidelines....4
Intel® Stratix® 10 GX Pin Connection Guidelines....5
Clock and PLL Pins....5
Dedicated Configuration/JTAG Pins....6
Optional/Dual-Purpose Configuration Pins....8
3V Compatible I/Os....9
Differential I/O Pins....10
External Memory Interface Pins....10
Voltage Sensor Pins....11
Temperature Sensor Pins....12
Reference Pins....13
No Connect and DNU Pins....14
Power Supply Pins....14
Transceiver Pins....19
Secure Device Manager (SDM) Pins....23
Notes to Intel Stratix 10 GX Pin Connection Guidelines....38
Intel Stratix 10 MX Pin Connection Guidelines....39
UIB and eSRAM Pins....39
Intel Stratix 10 MX Power Supply Pins....41
Notes to Intel Stratix 10 MX Pin Connection Guidelines....42
Intel Stratix 10 TX Pin Connection Guidelines....43
Intel Stratix 10 TX Transceiver Pins....43
Notes to Intel Stratix 10 TX Pin Connection Guidelines....45
Intel Stratix 10 SX Pin Connection Guidelines....46
Hard Processor System (HPS) Supply Pins....46
HPS Oscillator Clock Input Pin....48
HPS JTAG Pins....48
HPS GPIO Pins....49
HPS SDMMC Pins....50
HPS NAND Pins....51
HPS USB Pins....53
HPS EMAC Pins....54

HPS I2C_EMAC and MDIO Pins....56
HPS I2C Pins....57
HPS SPI Pins....58
HPS UART Pins....60
HPS Trace Pins....61
Notes to Intel Stratix 10 SX Pin Connection Guidelines....63
Power Supply Sharing Guidelines for Intel Stratix 10 Devices....64
Example 1—Intel Stratix 10 GX....65
Example 2—Intel Stratix 10 GX....68
Example 3—Intel Stratix 10 SX (–1V, –2V, and –3V parts)....71
Example 4—Intel Stratix 10 SX (–2L and –3X parts)....75
Example 5—Intel Stratix 10 SX (–1V, –2V, and –3V parts)....78
Example 6—Intel Stratix 10 SX (–2L and –3X parts)....82
Example 7—Intel Stratix 10 MX (–1V, –2V, and –3V parts)....86
Example 8—Intel Stratix 10 MX (–1V, –2V, and –3V parts)....90
Example 9—Intel Stratix 10 TX (–1V, –2V, and –3V parts)....94
Example 10—Intel Stratix 10 TX (–2L and –3X parts)....98
Document Revision History for the Intel Stratix 10 Device Family Pin Connection Guidelines....102

PCG-01020 | 2019.01.31

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Intel® Stratix® 10 Device Family Pin Connection Guidelines

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Intel® Stratix® 10 GX Pin Connection Guidelines

This section contains connection guidelines that apply to the Intel® Stratix® 10 GX, Intel Stratix 10 MX, Intel Stratix 10 TX, and Intel Stratix 10 SX devices.

Clock and PLL Pins

Note: Intel recommends that you create an Intel Quartus® Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 1. Clock and PLL Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK_[2][A,B,C,F,G,H,I,J,K,L,M,N]_[0,1]p CLK_[3][A,B,C,D,E,F,G,H,I,J,K,L]_[0,1]p	I/O, Clock Input	Dedicated high speed clock input pins that can be used for data inputs or outputs. Differential input OCT Rd, single-ended input OCT Rt, and single-ended output OCT Rs are supported on these pins. When you do not use these pins as dedicated clock pins, you can use them as regular I/O pins.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.
CLK_[2][A,B,C,F,G,H,I,J,K,L,M,N]_[0,1]n CLK_[3][A,B,C,D,E,F,G,H,I,J,K,L]_[0,1]n	I/O, Clock Input		
PLL_[2][A,B,C,F,G,H,I,J,K,L,M,N]_FB[0] PLL_[3][A,B,C,F,G,H,I,J,K,L]_FB[0]	I/O, Clock	Dual-purpose I/O pins that can be used as single-ended inputs, single-ended outputs, or external feedback input pins. For more information about the supported pins, refer to the device pin-out file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.
PLL_[2][A,B,C,F,G,H,I,J,K,L,M,N]_FBp	I/O, Clock	Dual-purpose I/O pins that can be used as differential I/Os, or external feedback input pins. For more information about the supported pins, refer to the device pin-out file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
PLL_[3] [A,B,C,F,G,H,I,J,K,L]_ FBp			
PLL_[2] [A,B,C,F,G,H,I,J,K,L,M ,N]_FBn PLL_[3] [A,B,C,F,G,H,I,J,K,L]_ FBn	I/O, Clock		
PLL_[2] [A,B,C,F,G,H,I,J,K,L,M ,N]_CLKOUT[0:1] PLL_[3] [A,B,C,F,G,H,I,J,K,L]_ CLKOUT[0:1] PLL_[2] [A,B,C,F,G,H,I,J,K,L,M ,N]_CLKOUT[0:1]p PLL_[3] [A,B,C,F,G,H,I,J,K,L]_ CLKOUT[0:1]p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair. For more information about the supported pins, refer to the device pin-out file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.
PLL_[2] [A,B,C,F,G,H,I,J,K,L,M ,N]_CLKOUT[0:1]n PLL_[3] [A,B,C,F,G,H,I,J,K,L]_ CLKOUT[0:1]n	I/O, Clock		

Dedicated Configuration/JTAG Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 2. Dedicated Configuration/JTAG Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
TCK	Input	Dedicated JTAG test clock input pin. This pin can also be used to access the SDM and HPS JTAG chains. For more information, refer to the HPS JTAG Pins on page 48.	If the JTAG interface is not used, connect this pin through a 1-kΩ pull-down resistor to GND. This pin has an internal 25-kΩ pull-down. Do not drive voltage higher than the VCCIO_SDM supply for the TCK pin. The TCK input pin is powered by the VCCIO_SDM supply.
TMS	Input	Dedicated JTAG test mode select input pin. This pin can also be used to access the SDM and HPS JTAG chains. For more information, refer to the HPS JTAG Pins on page 48.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to the VCCIO_SDM supply. If the JTAG interface is not used, connect the TMS pin to the VCCIO_SDM supply using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than the VCCIO_SDM supply for the TMS pin. The TMS input pin is powered by the VCCIO_SDM supply.
TDO	Output	Dedicated JTAG test data output pin. This pin can also be used to access the SDM and HPS JTAG chains. For more information, refer to the HPS JTAG Pins on page 48.	If the JTAG interface is not used, leave the TDO pin unconnected.
TDI	Input	Dedicated JTAG test data input pin. This pin can also be used to access the SDM and HPS JTAG chains. For more information, refer to the HPS JTAG Pins on page 48.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to the VCCIO_SDM supply. If the JTAG interface is not used, connect the TDI pin to the VCCIO_SDM supply using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than the VCCIO_SDM supply for the TDI pin. The TDI input pin is powered by the VCCIO_SDM supply.
nSTATUS	Output	This pin is used for synchronization with the device driving nCONFIG and to report errors.	When you are using the Avalon-ST configuration scheme, connect this pin to the configuration host. For other configuration schemes, you can use this pin to monitor the configuration status. This pin must be pulled up through a 10-kΩ resistor to VCCIO_SDM for all configuration schemes. This pin has an internal 25-kΩ pull-up.
nCONFIG	Input	The nCONFIG pin is used to clear the device and prepare for reconfiguration.	When you use the Avalon-ST configuration scheme, connect this pin directly to the configuration host.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			When you use other configuration schemes, pull this pin to VCCIO_SDM through an external 10-KΩ pull-up resistor. When you use other configuration schemes, this pin can be used to restart configuration by driving it low and then high again.
OSC_CLK_1	Input	This pin is used as the clock for device configuration and transceiver calibration.	You must provide an external clock source to this pin if you are using transceivers. If you choose to use the external clock source for configuration and/or instantiate any transceivers in your design, you must provide a 25-MHz, 100-MHz, or 125-MHz free-running clock source to this pin and enable it in the Intel Quartus Prime software when you compile your design. If you are using the internal oscillator for configuration and do not instantiate any transceivers in your design, leave this pin unconnected.

Optional/Dual-Purpose Configuration Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 3. Optional/Dual-Purpose Configuration Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
AVST_DATA[31:0]	I/O, Input	Dual-purpose configuration data input pins. Use DATA [15:0] pins for Avalon Streaming Interface (Avalon-ST) x16 mode, DATA [31:0] pins for Avalon-ST x32 mode, or as regular I/O pins. Avalon-ST x8 mode uses the SDM_IO pins. These pins can also be used as user I/O pins after configuration.	If these pins are not used as the dual-purpose pins and they are not used as I/O pins, leave these pins unconnected.
AVST_CLK	I/O, Input	Dual-purpose Avalon-ST interface clock input pin. This pin is used for Avalon-ST x16 and x32 configuration schemes.	Connect this pin to the clock signal of an external configuration controller when configuring using the Avalon-ST x16 or x32 interface.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
		This pin can also be used as a user I/O pin after configuration.	
AVST_VALID	I/O, Input	Dual-purpose Avalon-ST interface data valid input pin. This pin is used for Avalon-ST x16 and x32 configuration schemes. This pin can also be used as a user I/O pin after configuration.	Connect this pin to the data valid signal of an external configuration controller when configuring using the Avalon-ST x16 or x32 interface.
nPERST[L,R][0:2]	I/O, Input	Dual-purpose fundamental reset pin that is only available when you use together with PCI Express® (PCIe®) hard IP (HIP). When the PCIe HIP on a side (left or right) is enabled, the nPERST pins on that side cannot be used as general-purpose I/Os (GPIOs). In this case, connect the nPERST pin to the system PCIe nPERST signal to ensure that both ends of the link start link-training at the same time. The nPERST pins on a side are available as GPIOs only when the PCIe HIP on that side is not enabled. When the pin is low, the transceivers are in reset. When the pin is high, the transceivers are out of reset. When you do not use this pin as the fundamental reset, you can use this pin as a user I/O pin.	Connect this pin as defined in the Intel Quartus Prime software. This pin is powered by the VCCIO3V supply. When VCCIO3V is connected to a 3.0-V supply, you must use a diode to clamp the 3.3V LVTTL PCIe input signal to the VCCIO3V power of the device. When VCCIO3V is connected to any voltage other than 3.0V, you must use a level translator to shift down the voltage from 3.3V LVTTL to the corresponding voltage level powering the VCCIO3V pin. Only one nPERST pin is used per PCIe HIP. The Intel Stratix 10 components may have all six pins listed even when the specific component might only have 1 or 2 PCIe HIPs. • nPERSTL0 = Bottom Left PCIe HIP & CvP • nPERSTL1 = Middle Left PCIe HIP (When available) • nPERSTL2 = Top Left PCIe HIP (When available) • nPERSTR0 = Bottom Right PCIe HIP (When available) • nPERSTR1 = Middle Right PCIe HIP (When available) • nPERSTR2 = Top Right PCIe HIP (When available) For maximum compatibility, always use the bottom left PCIe HIP first, as this is the only location that supports Configuration via Protocol (CvP) using the PCIe link. See Note 13 in *Notes to Intel Stratix 10 GX Pin Connection Guidelines.*

3V Compatible I/Os

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 4. 3V Compatible I/Os Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
IO3V[0,1,2,3,4,5,6,7]_[10,12,20,22]	I/O	These are the 3.0V I/O pins. Each transceiver tile supports eight 3.0V I/O pins. These pins support 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.0V I/O standards. For details about the supported I/O standards, refer to the *Intel Stratix 10 Device Datasheet*.	Connect these pins according to the I/O interface standard you are using. You must provide power to the VCCR_GXB and VCCT_GXB pins of a transceiver tile to enable the 3.0V I/O pins within that tile. For any transceiver tiles that have their VCCR_GXB and/or VCCT_GXB unpowered, the corresponding 3.0V I/O pins within that tile is disabled. Connect unused pins as defined in the Intel Quartus Prime software.

Differential I/O Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 5. Differential I/O Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
LVDS[2][A,B,C,D,E,F,G,H,I,J,K,L,M,N]_[1:24][p,n] LVDS[3][A,B,C,D,E,F,G,H,I,J,K,L,M,N]_[1:24][p,n]	I/O, RX/TX channel	These are true LVDS receiver and transmitter channels on column I/O banks. Each I/O pair can be configured as a LVDS receiver or a LVDS transmitter. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If these pins are not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Intel Quartus Prime software.

External Memory Interface Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 6. External Memory Interface Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQS[0:47] DQS[48:95]	I/O, bi-directional	Optional data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.
DQSn[0:47] DQSn[48:95]	I/O, bi-directional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.
DQ[0:47] DQ[48:95]	I/O, bi-directional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan on migrating to a different memory interface that has a different DQ bus width, you need to reevaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the device pin-out file.	Connect unused pins as defined in the Intel Quartus Prime software.

Related Information

External Memory Interface Pin Information for Intel Stratix 10 Devices

Voltage Sensor Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 7. Voltage Sensor Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VREFP_ADC	Input	Dedicated precision analog voltage reference.	Tie the VREFP_ADC pin to an external 1.25V accurate reference source (+/- 0.2%) for better ADC performance. Treat the VREFP_ADC as an analog signal together with the VREFN_ADC signal that provides a differential 1.25V voltage. If no external reference is supplied, always connect the VREFP_ADC pin to GND. An on-chip reference source (+/-10%) is activated by connecting this pin to GND.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			VREFP_ADC must be equal to or lower than VCCA_PLL to prevent damage. When connecting an external voltage reference source to the VREFP_ADC and VREFN_ADC, Intel recommends keeping the VREF source as close as possible to minimize coupling noise to the power rail. Reference traces must be routed as a tightly coupled differential pair to the package ball with ground shielding. Intel recommends you to place a 10 µF and 1 µF board capacitor to decouple VREFP_ADC and VREFN_ADC. Place the 1 µF board capacitor as close as possible to the package balls.
VREFN_ADC	Input		Tie the VREFN_ADC pin to the GND for better ADC performance. Treat VREFN_ADC as an analog signal together with the VREFP_ADC signal that provides a differential 1.25V voltage. If no external reference is supplied, always connect the VREFN_ADC pin to GND. When connecting an external voltage reference source to the VREFP_ADC and VREFN_ADC, Intel recommends keeping the VREF source as close as possible to minimize coupling noise to the power rail. Reference traces must be routed as a tightly coupled differential pair to the package ball with ground shielding. Intel recommends you to place a 10 µF and 1 µF board capacitor to decouple VREFP_ADC and VREFN_ADC. Place the 1 µF board capacitor as close as possible to the package balls.
VSIGP_[0,1]	Input	2 pairs of analog differential inputs pins used with the voltage sensor inside the FPGA to monitor external analog voltages.	Tie these pins to GND if you do not use the voltage sensor feature. For details on the usage of these pins, refer to the *Intel Stratix 10 Analog to Digital Converter User Guide*. Do not drive VSIGP and VSIGN pins until the VCCA_PLL power rail has reached 1.62V to prevent damage.
VSIGN_[0,1]	Input		

Temperature Sensor Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 8. Temperature Sensor Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
TEMPDIODEp[0..6]	Input	These pins connect to the internal temperature sensing diodes in the FPGA core and in the transceiver tiles (bias-high input).	Connect this pin to an external temperature sensing device to allow sensing of the FPGA's temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave this pin unconnected. For more information about the locations and channel numbers of the temperature sensors, refer to the *Intel Stratix 10 Analog to Digital Converter User Guide*.
TEMPDIODEn[0..6]	Input	These pins connect to the internal temperature sensing diodes in the FPGA core and in the transceiver tiles (bias-low input).	Connect this pin to an external temperature sensing device to allow sensing of the FPGA's temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave this pin unconnected. For more information about the locations and channel numbers of the temperature sensors, refer to the *Intel Stratix 10 Analog to Digital Converter User Guide*.

Related Information

Temperature Sensor Channels

Reference Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 9. Reference Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RZQ_[2][A,B,C,F,G,H,I,J,K,L,M,N] RZQ_[3][A,B,C,D,E,F,G,H,I,J,K,L]	I/O, bi-directional	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. Connect the external precision resistor to the designated pin within the bank. If not required, this pin is a regular I/O pin.	When using OCT, tie these pins to GND through either a 240-Ω or 100-Ω resistor, depending on the desired OCT impedance. For more information on the OCT schemes, refer to the *Intel Stratix 10 General Purpose I/O User Guide*. When you do not use these pins as dedicated input for the external precision resistor or as I/O pins, leave these pins unconnected.

No Connect and DNU Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 10. No Connect and DNU Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, GND, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration, you have the option to connect these pins to either power, GND, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.

Power Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 11. Power Supply Pins (See Notes 4 through 10)—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCP	Power	VCCP supplies power to the periphery.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the Electrical Characteristics in the *Intel Stratix 10 Device Datasheet*.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			Use the Intel Stratix 10 Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board. See Notes 2, 3, 4, 6, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCC	Power	VCC supplies power to the core.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the Electrical Characteristics in the *Intel Stratix 10 Device Datasheet*. Use the Intel Stratix 10 Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board. See Notes 2, 3, 4, 6, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCPT	Power	Power supply for the programmable power technology and I/O pre-drivers.	Connect VCCPT to a 1.8V low noise switching regulator. You have the option to source the following from the same regulator as VCCPT: • VCCIO_SDM and VCCIO_HPS • VCCIO and VCCIO3V if these rails are using the same voltage level • VCCBAT if this rail is using the same voltage level and the design security key feature is not required • VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC with proper isolation filtering Provide a minimum decoupling of 1uF for the VCCPT power rail near the VCCPT pin. A floating voltage may be observed on VCCPT during device power-up and power-down sequencing due to VCCERAM, with the magnitude of the floating voltage being lower than VCCPT. This is the expected behavior and will neither cause any functional failure nor reliability concerns to the device as long as the power-up or power-down sequence is followed. For the power rail sharing, refer to the Power Supply Sharing Guidelines for Intel Stratix 10 Devices.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			See Notes 2, 3, 4, 7, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCA_PLL	Power	PLL Analog power.	Connect VCCA_PLL to a 1.8V low noise switching regulator. With proper isolation filtering, you have the option to source VCCA_PLL from the same regulator as VCCPT. See Notes 2, 3, 4, 7, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCIO([2] [A,B,C,F,L,M,N], [3] [A,B,C,I,J,K,L])	Power	These are the supply voltage pins for the I/O banks. Each bank can support a different voltage level. Supported VCCIO standards include the following: • Diff HSTL/HSTL(12,15,18) • Diff SSTL/SSTL(12,125, 135, 15, 18) • Diff HSUL/HSUL(12) • Diff POD 12 • LVDS/Mini_LVDS/RSDS • 1.2V, 1.5V, and 1.8V	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, or 1.8V supplies, depending on the I/O standard required by the specific bank. You have the option to power down unused I/O banks by connecting their VCCIO pin to GND. During the power-up sequence only, a transient current whose magnitude is less than the VCCIO operating static current may be observed as the VCCIO transistors become operational. This is the expected behavior and will neither cause any functional failure nor reliability concerns to the device as long as the power-up or power-down sequence is followed. When I/O bank 3A is used for AVST x16 or AVST x32 configuration mode, you must connect the VCCIO3A power supply to the VCCIO_SDM power supply for proper device functionality. For more details, refer to the *Intel Stratix 10 General Purpose I/O User Guide*. For the power rail sharing, refer to the Power Supply Sharing Guidelines for Intel Stratix 10 Devices. See Notes 2, 3, 4, 8, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCIO3V	Power	Power supply of the 3V I/O bank.	Connect these pins to 1.2V, 1.5V, 1.8V, 2.5V, or 3.0V supplies, depending on the I/O standard required by the specified bank. VCCIO3V must be powered on for proper device operation even if the VCCIO3V banks are unused. VCCR_GXB and VCCH_GXB must be powered up to operate the VCCIO3V bank. For more details, refer to the *Intel Stratix 10 General Purpose I/O User Guide*. For the power rail sharing, refer to the Power Supply Sharing Guidelines for Intel Stratix 10 Devices.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			See Notes 2, 3, 4, 8, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCIO_SDM	Power	Configuration pins power supply.	Connect these pins to a 1.8V power supply. When dual-purpose configuration pins are used for configuration, tie VCCIO of the bank where the dual-purpose configuration pins reside to the same regulator as VCCIO_SDM. When these pins require the same voltage level as VCCIO, you have the option to tie them to the same regulator as VCCIO. Provide a minimum decoupling of 47nF for the VCCIO_SDM power rail near the VCCIO_SDM pin. For the power rail sharing, refer to the Power Supply Sharing Guidelines for Intel Stratix 10 Devices. See Notes 2, 3, 4, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCERAM	Power	Embedded memory and digital transceiver power supply.	Connect all VCCERAM pins to a 0.9V low noise switching power supply. VCCPLLDIG_SDM must be sourced from the same regulator as VCCERAM with proper isolation filtering. For more details, refer to the *Intel Stratix 10 Device Datasheet*. See Notes 2, 3, 7, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCPLLDIG_SDM	Power	SDM block PLL power pins.	VCCPLLDIG_SDM must be sourced from the same regulator as VCCERAM with proper isolation filtering.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	When using the design security volatile key, connect this pin to a non-volatile battery power source in the range of 1.2V - 1.8V. When not using the volatile key, tie this pin to the 1.8-V VCCPT. This pin must be properly powered as per the recommended voltage range as the power-on reset (POR) circuitry of the Intel Stratix 10 devices monitors VCCBAT. Provide a minimum decoupling of 47nF for the VCCBAT power rail near the VCCBAT pin. For the power rail sharing, refer to the Power Supply Sharing Guidelines for Intel Stratix 10 Devices.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCPLL_SDM	Power	VCCPLL_SDM supplies analog power to the SDM block PLLs.	Connect these pins to a 1.8V low noise power supply through a proper isolation filter. With proper isolation filtering, you have the option to source VCCPLL_SDM from the same regulator as VCCPT when all power rails require 1.8V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
GND	Ground	Device ground pins.	Connect all GND pins to the board ground plane.
VREFB[[2][A,B,C,F,G,H,I,J,K,L,M,N], [3][A,B,C,D,E,F,G,H,I,J,K,L]]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then use these pins as voltage-reference pins for the bank.	If VREF pins are not used, connect them to either the VCCIO in the bank in which the pins reside or GND. See Notes 2, 8, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCLSENSE	Power	Differential sense line to external regulator.	VCCLSENSE and GNDSENSE are differential remote sense pins for the VCC power. Connect your regulators' differential remote sense lines to the respective VCCLSENSE and GNDSENSE pins. This compensates for the DC IR drop associated with the PCB and device package from the VCC power. Route these connections as differential pair traces and keep them isolated from any other noise source. You must connect the VCCLSENSE and GNDSENSE lines to the regulator's remote sense inputs.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
GNDSENSE	Power		
VCCADC	Power	ADC power pin for the voltage sensors.	You must supply a low noise 1.8V power supply to this pin if you are using the internal voltage sensors of the Intel Stratix 10 device. When you are using the voltage sensors, tie this pin to VCCA_PLL with proper isolation filtering. If you are not using the voltage sensors, tie this pin to VCCA_PLL.
VCCFUSEWR_SDM	Power	The required power supply to program (write) the optional, one-time programmable eFuses. These eFuses are an integral part of the Intel Stratix 10 security architecture. For more information, refer to the *Intel Stratix 10 Device Security User Guide*.	2.4V power supply is required on this pin if field-programming of the eFuses is required. If field-programming of the eFuses is not required, tie this pin to VCCPT or leave it unconnected (floating). Do not tie this pin to GND. If field-programming of the eFuses is required, Intel recommends you to use an adjustable regulator that is set to 2.4V output when programming the eFuses and 1.8V output at all other times. A floating voltage may be observed on the VCCFUSEWR_SDM power during power-up and power-down sequencing due to VCCPT and/or VCCERAM, with the total magnitude of the floating voltage being lower than VCCFUSEWR_SDM. During the power-up sequence only, a transient current whose magnitude is less than the VCCFUSEWR_SDM operating transient current may be observed. The floating voltage and transient current are expected behavior and will neither cause any functional failure nor reliability concerns to the device as long as the power-up or power-down sequence is followed.

Transceiver Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 12. Transceiver Pins (See Notes 4 through 10)—Preliminary

For more information on the pin description and connection guidelines of the nPERST[L,R][0:2] pins, refer to the *Optional/Dual-Purpose Configuration Pins* section. For more information on the pin description and connection guidelines of the OSC_CLK_1 pin, refer to the *Dedicated Configuration/JTAG Pins* section.

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCR_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]	Power	Analog power, receiver, specific to each transceiver bank of the left (L) side or right (R) side of the device.	Connect VCCR_GXB pins to a 1.03V or 1.12V low noise switching regulator depending on the transceiver data rate. VCCR_GXB and VCCT_GXB pins of each bank within a transceiver tile (L-tile or H-tile) must have the same voltage (either 1.03V or 1.12V). However, VCCR_GXB and VCCT_GXB of different banks within the same transceiver tile can have different voltages based on the configured transceiver data rates to further reduce power consumption of the transceiver tile. When the banks within a transceiver tile are powered at different voltages (for example, some banks operating at 1.03V while other banks operating at 1.12V), the xN clock lines are only allowed to transverse between contiguous banks operating at the same VCCR_GXB or VCCT_GXB voltages. The xN clock lines crossing boundaries of banks operating at different voltages is not allowed. For any input reference clock coming into a transceiver tile, that clock can be distributed to any bank within the tile even if the VCCR_GXB and VCCT_GXB operating voltages of the banks are different. When all of the transceivers on the same tile are not used, you may power down the transceivers in that tile by connecting its VCCR_GXB, VCCT_GXB, and VCCH_GXB to GND. Place a 22-nF decoupling capacitor between each VCCR_GXB power pin and GND pin on the back side of the BGA pin field. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*. See Notes 2, 3, 4, 7, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCT_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]	Power	Analog power, transmitter, specific to each transceiver bank of the left (L) side or right (R) side of the device.	Connect VCCT_GXB pins to a 1.03V or 1.12V low noise switching regulator depending on the transceiver data rate. VCCR_GXB and VCCT_GXB pins of each bank within a transceiver tile (L-tile or H-tile) must have the same voltage (either 1.03V or 1.12V). However, VCCR_GXB and VCCT_GXB

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			of different banks within the same transceiver tile can have different voltages based on the configured transceiver data rates to further reduce power consumption of the transceiver tile. When the banks within a transceiver tile are powered at different voltages (for example, some banks operating at 1.03V while other banks operating at 1.12V), the xN clock lines are only allowed to transverse between contiguous banks operating at the same VCCR_GXB or VCCT_GXB voltages. The xN clock lines crossing boundaries of banks operating at different voltages is not allowed. For any input reference clock coming into a transceiver tile, that clock can be distributed to any bank within the tile even if the VCCR_GXB and VCCT_GXB operating voltages of the banks are different. When all of the transceivers on the same tile are not used, you may power down the transceivers in that tile by connecting its VCCR_GXB, VCCT_GXB, and VCCH_GXB to GND. Place a 22-nF decoupling capacitor between each VCCT_GXB power pin and GND pin on the back side of the BGA pin field. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*. See Notes 2, 3, 4, 7, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
VCCH_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]	Power	Analog power, block level transmitter buffers, specific to the left (L) side or right (R) side of the device.	Connect VCCH_GXB to 1.8V low noise switching regulator. With a proper isolation filtering, you have the option to source VCCH_GXB from the same regulator as VCCPT. To minimize the regulator switching noise impact on channel jitter performance, keep the switching frequency for VCCH_GXB regulator below 2 MHz. For OTN applications, the switching frequency for VCCH_GXB is recommended to be below 500 KHz. Place a 22-nF decoupling capacitor between each VCCH_GXB power pin and GND pin on the back side of the BGA pin field.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			A leakage voltage may be observed on the VCCH_GXB power rail before the VCCH_GXB is powered on due to leakage inside the device during the power-up and power-down sequencing. The total magnitude of this leakage voltage is lower than VCCH_GXB and this is an expected behavior. During the power-up sequence only, a transient current whose magnitude is less than the VCCH_GXB static operating current may be observed. The floating voltage and transient current are expected behavior and will neither cause any functional failure nor reliability concerns to the device as long as the power-up or power-down sequence is followed. When all of the transceivers on the same tile are not used, you may power down the transceivers in that tile by connecting its VCCR_GXB, VCCT_GXB, and VCCH_GXB to GND. See Notes 2, 3, 4, 7, and 10 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
`GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_RX_CH[0:5]p` `GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_REFCLK[0:5]p`	Input	High speed positive differential receiver channels or REFCLK inputs. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	These pins can be AC-coupled or DC-coupled when used. For more information, refer to the *Intel Stratix 10 Device Datasheet*. Connect all unused GXB_RXp pins directly to GND.
`GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_RX_CH[0:5]n` `GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_REFCLK[0:5]n`	Input	High speed negative differential receiver channels or REFCLK inputs. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	These pins can be AC-coupled or DC-coupled when used. For more information, refer to the *Intel Stratix 10 Device Datasheet*. Connect all unused GXB_RXn pins directly to GND.
`GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_TX_CH[0:5]p`	Output	High speed positive differential transmitter channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating.
`GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_TX_CH[0:5]n`	Output	High speed negative differential transmitter channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	Leave all unused GXB_TXn pins floating.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_CH[B,T]p	Input	High speed differential reference clock positive receiver channels, specific to each transceiver bank of the left (L) side or right (R) side of the device. REFCLK_GXB can be used as dedicated clock input pins with fPLL for core clock generation even when the transceiver channel is not used.	These pins should be AC-coupled when connected to any I/O standard other than the HCSL I/O standard. For the HCSL I/O standard, these pins must be DC-coupled. For example, PCIe reference clocks should be DC-coupled if it uses the HCSL I/O standard. Connect all unused pins individually to GND. See Note 9 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_CH[B,T]n	Input	High speed differential reference clock complement, complementary receiver channel, specific to each transceiver bank of the left (L) side or right (R) side of the device. REFCLK_GXB can be used as dedicated clock input pins with fPLL for core clock generation even when the transceiver channel is not used.	These pins should be AC-coupled when connected to any I/O standard other than the HCSL I/O standard. For the HCSL I/O standard, these pins must be DC-coupled. For example, PCIe reference clocks should be DC-coupled if it uses the HCSL I/O standard. Connect all unused pins individually to GND. See Note 9 in Notes to Intel Stratix 10 GX Pin Connection Guidelines.
RREF_[T,M,B][L,R]	Input	Reference resistor for fPLL, IOPLL, and transceiver, specific to the top (T), middle (M), and bottom (B) of the left (L) side or right (R) side of the device.	If any REFCLK pin or transceiver channel on one side (left or right) of the device, IOPLL, or fPLL is used, you must connect each RREF pin on that side of the device to its own individual 2kΩ +/-1% resistor to GND. Otherwise, you can connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Secure Device Manager (SDM) Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 13. SDM Pins (See Note 11)—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RREF_SDM	Input	Reference resistor input for the PLLs of the SDM interface.	Connect a 2kΩ +/-1% resistor to GND.
SDM_IO0	PWRMGT_SCL	PMBus Power Management Clock. By default, the PWRMGT_SCL function is enabled in SDM_IO14. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM_IO0 pin. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up. When this pin is used as the PWRMGT_SCL function, this pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V.	This pin is used as the clock pin for the PMBus interface. When a –V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the VCC voltage regulator for the PMBus slave mode. Connect this pin to the PMBus clock pin of your regulator.
	INIT_DONE	The INIT_DONE pin indicates the device has enter user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime software. Intel recommends you to use SDM_IO0 or SDM_IO16 to implement the INIT_DONE function when available as it has an internal weak pull-down for the correct function of INIT_DONE during power up. If SDM_IO0 and SDM_IO16 are unavailable, SDM_IO5 can also be used for the INIT_DONE function when the configuration mode is set to Avalon®–ST x8 or Avalon–ST x32 (AVST x8 or AVST x32) as these modes require an external 4.7–kΩ pull-down resistor. If SDM_IO0, SDM_IO5, and SDM_IO16 are unavailable, the INIT_DONE function can also be implemented using any unused SDM I/O pins provided that an external 4.7–kΩ pull-down resistor is provided for the INIT_DONE signal. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	When the INIT_DONE function is enabled, this pin will drive high when configuration is completed and the device goes into user mode.
	PWRMGT_ALERT	PMBus Power Management Alert. When this pin is used as the PWRMGT_ALERT function, this pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V.	This pin is used as the ALERT function for the PMBus interface when the Intel Stratix 10 –V is the PMBus slave. When using the SmartVID feature with the Intel Stratix 10 –V device as a PMBus slave, you must connect either the SDM_IO0 or SDM_IO12 pin as the PWRMGT_ALERT signal along with the PWRMGT_SCL and PWRMGT_SDA signals to the PMBus master device to complete the SmartVID power

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	management interface. The PMBus master device reads the VID codes from the Intel Stratix 10 slave and programs the voltage regulator to output the correct VID voltage. Connect this pin to the PMBus ALERT pin of your regulator.
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad serial peripheral interface (quad SPI) devices.
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.
SDM_IO1	AVSTx8_DATA2	Avalon-ST Interface Data 2. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data2 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
	AS_DATA1	Active Serial Data 1. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data1 pin of the EPCQ-L device when configuring from the EPCQ-L device.
	SDMMC_CFG_DATA1	SD/MMC Card Data 1. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data1 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
SDM_IO2	AVSTx8_DATA0	Avalon Stream Interface Data 0. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data0 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
	AS_CLK	Active Serial Clock. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the clock input of the EPCQ-L device when configuring from the EPCQ-L device.
	SDMMC_CFG_DATA0	SD/MMC Card Data 0. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data0 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
SDM_IO3	AVSTx8_DATA3	Avalon Stream Interface Data 3. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data3 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
	AS_DATA2	Active Serial Data 2. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data2 pin of the EPCQ-L device when configuring from the EPCQ-L device.
	SDMMC_CFG_DATA2	SD/MMC Card Data 2. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data2 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
SDM_IO4	AVSTx8_DATA1	Avalon Stream Interface Data 1. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data1 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
	AS_DATA0	Active Serial Data 0. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data0 pin of the EPCQ-L device when configuring from the EPCQ-L device.
	SDMMC_CFG_CMD	SD/MMC Card Command. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the command input of the SD/MMC card flash device when configuring from the SD/MMC flash.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
SDM_IO5	MSEL[0]	Configuration input pins that set the configuration scheme for the FPGA device. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	This pin will function as MSEL[0] during power up and reset to determine the configuration scheme. This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected. For more information, refer to the *Intel Stratix 10 Configuration User Guide*.
	CONF_DONE	The CONF_DONE pin indicates all configuration data has been received. By default, SDM_IO16 is the recommended pin to implement the CONF_DONE function. If you are using the Avalon-ST x8 configuration scheme and PMBus power management feature, the PWRMGT_SDA function can be assigned to either SDM_IO12 or SDM_IO16. Use SDM_IO5 to implement the CONF_DONE function if SDM_IO16 is used for the PWRMGT_SDA function. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect the CONF_DONE pin to the external configuration controller when configuring using the Avalon-ST interface.
	AS_nCSO0	Active Serial Chip Select 0. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the nCS input of the first EPCQ-L device when configuring from EPCQ-L devices.
	SDMMC_CFG_CCLK	SD/MMC Card Clock. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the clock input of the SD/MMC card flash device when configuring from the SD/MMC flash.
	INIT_DONE	The INIT_DONE pin indicates the device has enter user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime software. Intel recommends you to use SDM_IO0 or SDM_IO16 to implement the INIT_DONE function when available as it has an internal weak pull-down for the correct function of INIT_DONE during power up. If SDM_IO0 and SDM_IO16 are unavailable, SDM_IO5 can also be used for the INIT_DONE function when the configuration mode is set to Avalon–ST x8 or Avalon–ST x32 (AVST x8 or AVST x32) as these modes require an external 4.7–kΩ pull-down resistor.	When the INIT_DONE function is enabled, this pin will drive high when configuration is completed and the device goes into user mode.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		If SDM_IO0, SDM_IO5, and SDM_IO16 are unavailable, the INIT_DONE function can also be implemented using any unused SDM I/O pins provided that an external 4.7–kΩ pull-down resistor is provided for the INIT_DONE signal. This pin is pulled high internally by a 25–kΩ resistor when the device is powered up.	
SDM_IO6	AVSTx8_DATA4	Avalon Stream Interface Data 4. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data4 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
	AS_DATA3	Active Serial Data 3. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data3 pin of the EPCQ-L device when configuring from the EPCQ-L device.
	SDMMC_CFG_DATA3	SD/MMC Card Data 3. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data3 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
SDM_IO7	MSEL[1]	Configuration input pins that set the configuration scheme for the FPGA device. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	This pin will function as MSEL[1] during power up and reset to determine the configuration scheme. This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected. For more information, refer to the *Intel Stratix 10 Configuration User Guide*.
	AS_nCSO2	Active Serial Chip Select 2. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the nCS input of the third EPCQ-L device when configuring from EPCQ-L devices.
SDM_IO8	AVST_READY	Avalon Stream Interface Data Ready. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the ready signal output of the external configuration controller when configuring using the Avalon-ST x8 , x16, or x32 interface.
	AS_nCSO3	Active Serial Chip Select 3. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the nCS input of the fourth EPCQ-L device when configuring from EPCQ-L devices.
	SDMMC_CFG_DATA4	SD/MMC Card Data 4. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data4 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
SDM_IO9	MSEL[2]	Configuration input pins that set the configuration scheme for the FPGA device. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	This pin will function as MSEL[2] during power up and reset to determine the configuration scheme. This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected. For more information, refer to the *Intel Stratix 10 Configuration User Guide*.
	AS_nCSO1	Active Serial Chip Select 1. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the nCS input of the second EPCQ-L device when configuring from EPCQ-L devices.
SDM_IO10	AVSTx8_DATA7	Avalon Stream Interface Data 7. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data7 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
	SDMMC_CFG_DATA7	SD/MMC Card Data 7. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data7 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.
SDM_IO11	AVSTx8_VALID	Avalon Stream Interface Data Valid. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data valid pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
	PWRMGT_SDA	PMBus Power Management Serial Data. By default, use the SDM_IO11 pin for the PWRMGT_SDA function. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM_IO12 pin. When this pin is used as the PWRMGT_SDA function, this pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	This pin is used as the data pin for the PMBus interface. When a –V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the VCC voltage regulator for the PMBus slave mode. Connect this pin to the PMBus data pin of your regulator.
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices.
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.
SDM_IO12	PWRMGT_SDA	PMBus Power Management Serial Data. By default, use the SDM_IO11 pin for the PWRMGT_SDA function. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM_IO12 or SDM_IO16 pin. When this pin is used as the PWRMGT_SDA function, this pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	This pin is used as the data pin for the PMBus. When a –V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the VCC voltage regulator for the PMBus slave mode. Connect this pin to the PMBus data pin of your regulator.
	PWRMGT_ALERT	PMBus Power Management Alert. When this pin is used as the PWRMGT_ALERT function, this pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ	This pin is used as the ALERT function for the PMBus interface when the Intel Stratix 10 –V is the PMBus slave.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	When using the SmartVID feature with the Intel Stratix 10 –V device as a PMBus slave, you must connect either the SDM_IO0 or SDM_IO12 pin as the PWRMGT_ALERT signal along with the PWRMGT_SCL and PWRMGT_SDA signals to the PMBus master device to complete the SmartVID power management interface. The PMBus master device reads the VID codes from the Intel Stratix 10 slave and programs the voltage regulator to output the correct VID voltage. Connect this pin to the PMBus ALERT pin of your regulator.
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices.
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
SDM_IO13	AVSTx8_DATA5	Avalon Stream Interface Data 5. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	This pin has multiple functions depending on the configuration mode used: • Connect this pin to the data5 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. • Connect this pin to the data5 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
	SDMMC_CFG_DATA5	SD/MMC Card Data 5. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices.
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
SDM_IO14	AVSTx8_CLK	Avalon Stream Interface Clock Input. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the clock output of an external configuration controller when configuring using the Avalon-ST x8 interface.
	PWRMGT_SCL	PMBus Power Management Clock. By default, the PWRMGT_SCL function is enabled in SDM_IO14. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM_IO0 pin. When this pin is used as the PWRMGT_SCL function, this pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	This pin is used as the clock pin for the PMBus interface. When a –V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the VCC voltage regulator for the PMBus slave mode. Connect this pin to the PMBus clock pin of your regulator.
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.
SDM_IO15	AVSTx8_DATA6	Avalon Stream Interface Data 6. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data6 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
	SDMMC_CFG_DATA6	SD/MMC Card Data 6. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this pin to the data6 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.
SDM_IO16	CONF_DONE	The CONF_DONE pin indicates device configuration has completed. SDM_IO16 is the recommended pin to implement the CONF_DONE function, if this pin is enabled in the Intel Quartus Prime software. Intel recommends you to use this pin as it has a weak pull-down for the correct function during power up. If you are using the Avalon-ST x8 configuration scheme and PMBus power management feature, the PWRMGT_SDA function can be assigned to either SDM_IO12 or SDM_IO16. Use SDM_IO5 to implement the CONF_DONE function if SDM_IO16 is used for the PWRMGT_SDA function. The CONF_DONE function can also be implemented using other unused SDM I/O pins. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect the CONF_DONE pin to the external configuration controller when configuring using the Avalon-ST interface.
	PWRMGT_SDA	PMBus Power Management Serial Data. By default, use the SDM_IO11 pin for the PWRMGT_SDA function. When this pin is used as the PWRMGT_SDA function, this pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	This pin is used as the data pin for the PMBus interface. When a –V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the VCC voltage regulator for the PMBus slave mode. Connect this pin to the PMBus data pin of your regulator.
	INIT_DONE	The INIT_DONE pin indicates the device has enter user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime software.	When the INIT_DONE function is enabled, this pin will drive high when configuration is completed and the device goes into user mode.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		Intel recommends you to use SDM_IO0 or SDM_IO16 to implement the INIT_DONE function when available as it has an internal weak pull-down for the correct function of INIT_DONE during power up. If SDM_IO0 and SDM_IO16 are unavailable, SDM_IO5 can also be used for the INIT_DONE function when the configuration mode is set to Avalon–ST x8 or Avalon–ST x32 (AVST x8 or AVST x32) as these modes require an external 4.7–kΩ pull-down resistor. If SDM_IO0, SDM_IO5, and SDM_IO16 are unavailable, the INIT_DONE function can also be implemented using any unused SDM I/O pins provided that an external 4.7–kΩ pull-down resistor is provided for the INIT_DONE signal. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	
	SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the SEU event.
	CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software. This pin is pulled low internally by a 25-kΩ resistor when the device is powered up.	Connect this output pin to an external logic that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.
	HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25-kΩ pull up on this pin.	
	Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image. This pin is pulled down internally by a 25–kΩ resistor when the device is powered up.	Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.

Notes to Intel Stratix 10 GX Pin Connection Guidelines

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Stratix 10 GX device variant.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.

6. Example 1 and Example 2 illustrate the power supply sharing guidelines for the Intel Stratix 10 GX devices.
7. Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response. The switching frequency range is not an Intel requirement.
8. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the *Intel Stratix 10 General Purpose I/O User Guide*.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.
11. There are no dedicated PR_REQUEST, PR_ERROR, and PR_DONE pins. If required, you can use user I/O pins for these functions.
12. The device orientation is die view (bottom of chip view).

Intel Stratix 10 MX Pin Connection Guidelines

This section contains connection guidelines that are specific to the Intel Stratix 10 MX devices. The common connection guidelines are listed in the *Intel Stratix 10 GX Pin Connection Guidelines* section.

Note: Depending on your Intel Stratix 10 MX device, it can support H-tile or E-tile transceivers. For the H-tile transceivers, refer to the *Transceiver Pins* in the *Intel Stratix 10 GX Pin Connection Guidelines* section. For the E-tile transceivers, refer to the *Intel Stratix 10 TX Transceiver Pins* in the *Intel Stratix 10 TX Pin Connection Guidelines* section.

UIB and eSRAM Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 14. UIB and eSRAM Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK_ESRAM_[0,1]p	Embedded SRAM (eSRAM) Clock Input	Dedicated positive high speed differential reference clock pin for eSRAM PLL.	Connect this pin to the positive terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime **ESRAM PLL Reference Clock Frequency** selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen: • 20 ps peak-to-peak • 1.42 ps RMS at 1e-12 BER • 1.22 ps at 1e-16 BER Connect directly to GND if unused.
CLK_ESRAM_[0,1]n	eSRAM Clock Input	Dedicated complement high speed differential reference clock pin for eSRAM PLL.	Connect this pin to the negative terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime **ESRAM PLL Reference Clock Frequency** selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen: • 20 ps peak-to-peak • 1.42 ps RMS at 1e-12 BER • 1.22 ps at 1e-16 BER Connect directly to GND if unused.
UIB_PLL_REF_CLK_[00,01]p	UIB Clock Input	Dedicated positive high speed differential reference clock pin for UIB PLL.	Connect this pin to the positive terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime HBM2 interface **PLL Reference Clock Frequency** selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen: • 10 ps peak-to-peak • 1.42 ps RMS at 1e-12 BER • 1.22 ps at 1e-16 BER Connect directly to GND if unused.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
UIB_PLL_REF_CLK_[00,01]n	UIB Clock Input	Dedicated complement high speed differential reference clock pin for UIB PLL.	Connect this pin to the negative terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime HBM2 interface **PLL Reference Clock Frequency** selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen: • 10 ps peak-to-peak • 1.42 ps RMS at 1e-12 BER • 1.22 ps at 1e-16 BER Connect directly to GND if unused.
RREF_ESRAM_[0,1]	eSRAM RREF Input	Reference resistor pin for UIB PLL and eSRAM PLL, specific to top (T) and bottom (B) of device.	If any UIB PLL or eSRAM PLL on the top or bottom side of the device is used, the corresponding RREF pin on that side of the device (top or bottom) must connect to its own individual 2K Ω +/-1% resistor to GND. The PCB trace between this pin and the reference resistor needs to be carefully routed to avoid any aggressor signals.
UIB_RREF_[00,01]	UIB RREF Input	Reference resistor pin for UIB IO ZQ calibration.	Connect each pin through an individual 240Ω +/- 1% resistor to GND. No resistor sharing between pins is allowed. Leave this pin floating if unused.

Intel Stratix 10 MX Power Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 15. Intel Stratix 10 MX Power Supply Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCM_WORD_[BL,TL]	Power	Power supply for the embedded HBM2 memory.	Connect these pins to a 2.5V power supply.
VCCIO_UIB_[BL,TL]	Power	Power supply for the Universal Interface Bus between the core and embedded HBM2 memory.	Connect these pins to a 1.2V power supply.

Notes to Intel Stratix 10 MX Pin Connection Guidelines

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Stratix 10 MX device variant.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
6. Example 7 and Example 8 illustrate the power supply sharing guidelines for the Intel Stratix 10 MX devices.
7. Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response. The switching frequency range is not an Intel requirement.
8. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the *Intel Stratix 10 General Purpose I/O User Guide*.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.

Intel Stratix 10 TX Pin Connection Guidelines

This section contains connection guidelines that are specific to the Intel Stratix 10 TX devices. The common connection guidelines are listed in the *Intel Stratix 10 GX Pin Connection Guidelines* section.

Intel Stratix 10 TX Transceiver Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 16. Intel Stratix 10 TX Transceiver Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCH_GXE(L2, L3, R1, R2, R3)	Power	Analog power, block level transmitter buffers for E-tile, specific to the left (L) side or right (R) side of the device.	Connect VCCH_GXE to a 1.1V low noise switching regulator.
VCCRT_GXE(L2, L3, R1, R2, R3)	Power	Analog power, used for the high-speed circuitry for the E-tile blocks, specific to the left (L) side or right (R) side of the device.	Connect VCCRT_GXE to VCCERAM through an LC filter. For more information about the LC filter design, refer to the *Intel Stratix 10 Power Management User Guide*.
VCCRTPLL_GXE(L2, L3, R1, R2, R3)	Power	Analog power, used for the high-speed circuitry for the E-tile blocks, specific to the left (L) side or right (R) side of the device.	You must source the VCCRTPLL_GXE from the VCCRT_GXE with proper isolation filtering. Filtering may be optional if this voltage rail can meet the noise mask requirement. For more information about the noise mask requirements, refer to the *Intel Stratix 10 Power Management User Guide*.
VCCCLK_GXE(L2, L3, R1, R2, R3)	Power	I/O power, specific to the E-tile reference clock buffers.	Connect VCCCLK_GXE to a 2.5V low noise switching regulator.
GXE(L8, R9)(A, B, C)_RX_CH[0:23]p	Input	High speed positive differential serial inputs to the receiver circuitry. Specific to the E-tile transceiver blocks on the left (L) side or right (R) side of the device.	No off-chip AC-coupling capacitor is required as long as the RX input common mode is between VCCRT_GXE and GND, and the RX input amplitude difference is <1200mVp-p. The absolute maximum input to E-Tile block SerDes is VCCRT_GXE + 300mV in order to prevent forward biasing of the ESD diodes. When using external AC-coupling capacitors, the RX termination is to the VCCH_GXE supply. For more information about the external AC-coupling, refer to the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			Leave unused pins floating.
GXE(L8, R9)(A, B, C)_RX_CH[0:23]n	Input	High speed negative differential serial inputs to the receiver circuitry. Specific to the E-tile transceiver blocks on the left (L) side or right (R) side of the device.	No off-chip AC-coupling capacitor is required as long as the RX input common mode is between VCCRT_GXE and GND, and the RX input amplitude difference is <1200mvp-p. The absolute maximum input to E-Tile block SerDes is VCCRT_GXE + 300mV in order to prevent forward biasing of the ESD diodes. When using external AC-coupling capacitors, the RX termination is to the VCCH_GXE supply. For more information about the external AC-coupling, refer to the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*. Leave unused pins floating.
GXE(L8, R9)(A, B, C)_TX_CH[0:23]p	Output	High speed positive differential serial outputs from the transmitter circuitry. Specific to the E-tile transceiver blocks on the left (L) side or right (R) side of the device.	Leave all unused GXE_TXp pins floating.
GXE(L8, R9)(A, B, C)_TX_CH[0:23]n	Output	High speed negative differential serial outputs from the transmitter circuitry. Specific to the E-tile transceiver blocks on the left (L) side or right (R) side of the device.	Leave all unused GXE_TXn pins floating.
REFCLK_GXE(L8,R9)(A,B,C)_CH[0:8]p	Input	High speed differential reference clock positive receiver channels, specific to each E-tile transceiver bank of the left (L) side or right (R) side of the device. REFCLK_GXE can be supplied to both RX and TX independently. REFCLK_GXE can be used as dedicated clock input pins for core clock generation even when the transceiver channel is not available.	No off-chip AC-coupling capacitor is required. The default internal REFCLK inputs are 2.5-V LVPECL with a 50-Ω termination. Optional external termination is 2.5-V LVPECL or 3.3-V LVPECL. For more information about the external AC-coupling, refer to the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*. Tie each unused REFCLK pin to GND through a 1-kΩ resistor. To properly disable the unused REFCLK inputs, you need to disable the internal termination and enable hysteresis. For instructions to set these registers, refer to the Reference Clocks section in the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*.
REFCLK_GXE(L8,R9)(A,B,C)_CH[0:8]n	Input	High speed differential reference clock negative receiver channels, specific to each E-tile transceiver bank of the left (L) side or right (R) side of the device. REFCLK_GXE can be supplied to both RX and TX independently. REFCLK_GXE can be used as dedicated clock input pins for core clock generation even when the transceiver channel is not available.	No off-chip AC-coupling capacitor is required. The default internal REFCLK inputs are 2.5-V LVPECL with a 50-Ω termination. Optional external termination is 2.5-V LVPECL or 3.3-V LVPECL. For more information about the external AC-coupling, refer to the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*. Tie each unused REFCLK pin to GND through a 1-kΩ resistor.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			To properly disable the unused REFCLK inputs, you need to disable the internal termination and enable hysteresis. For instructions to set these registers, refer to the Reference Clocks section in the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*.
`IO_AUX_RREF(11, 12, 20, 21, 22)`	Input	Reference resistor for the AIB auxiliary channel.	Connect to a 2-kΩ resistor (±1%) to GND.

Related Information

Intel Stratix 10 E-Tile Transceiver PHY User Guide

Notes to Intel Stratix 10 TX Pin Connection Guidelines

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Stratix 10 TX device variant.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.

6. Example 9 and example 10 illustrate the power supply sharing guidelines for the Intel Stratix 10 TX devices.
7. Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response. The switching frequency range is not an Intel requirement.
8. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the *Intel Stratix 10 General Purpose I/O User Guide*.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.

Intel Stratix 10 SX Pin Connection Guidelines

This section contains connection guidelines that are specific to the Intel Stratix 10 SX devices. The common connection guidelines are listed in the *Intel Stratix 10 GX Pin Connection Guidelines* section.

Hard Processor System (HPS) Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 17. HPS Supply Pins—Preliminary

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCL_HPS	Power	VCCL_HPS supplies power to the HPS core.	The VCCL_HPS power supply voltage could vary from 0.8V to 0.94V for –1V, –2V, or –3V devices with the SmartVID feature depending on the SmartVID setting in the device. When using –2L or –3X devices, you must connect to either 0.9V or 0.94V supply. If you are using 0.9V supply, VCCL_HPS can be connected to VCCERAM.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			VCCL_HPS can be shared with VCC and VCCP if they are at the same voltage level only when using –1V, –2V, or –3V devices (with the SmartVID feature). VCCL_HPS cannot be shared with VCC and VCCP when using –2L or –3X devices. VCCL_HPS always needs to be equal to VCCPLLDIG_HPS. Use the Intel Stratix 10 Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCCL_HPS and other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 6 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.
VCCIO_HPS	Power	The HPS dedicated I/Os support 1.8V voltage level.	Connect these pins to 1.8V power supply. If these pins have the same voltage requirement as VCCIO and VCCIO_SDM, you have the option to source VCCIO_HPS pins from the same regulator as VCCIO and VCCIO_SDM. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.
VCCPLL_HPS	Power	VCCPLL_HPS supplies analog power to the HPS PLLs.	Connect these pins to a 1.8V low noise power supply through a proper isolation filter. You have the option to share VCCPLL_HPS with the same regulator as VCCPT when all power rails require 1.8V but only with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.
VCCPLLDIG_HPS	Power	Digital power supply of the PLL in HPS.	Connect this to the VCCL_HPS with proper isolation filtering. For more information about isolation filters, refer to *AN583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs*.

You can use the HPS Component in the Platform Designer to assign the HPS Dedicated I/Os to various HPS Peripherals and one `hps_osc_clk` input. The handoff files generated by the Platform Designer during the Intel Quartus Prime compilation will set the pin mux registers (`pin0sel` through `pin47sel`) and the HPS Oscillator Clock register (`hps_osc_clk`) to their respective HPS pin functions.

For more information about the valid combinations of the HPS I/O assignments, refer to the *Hard Processor System Pin Information for Intel Stratix 10 Devices*.

Related Information

Hard Processor System Pin Information for Intel Stratix 10 Devices

HPS Oscillator Clock Input Pin

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 18. HPS Oscillator Clock Input Pin—Preliminary

You must provide one input clock source to the HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
HPS_OSC_CLK	Clock input pin that drives the main PLL. Connect a single-ended clock source to this pin. The I/O standard of the clock source must be compatible with VCCIO_HPS. For more information, refer to the valid frequency range of the clock source in the *Intel Stratix 10 Device Datasheet*.	Input	Select one of the 48 HPS dedicated I/O in Platform Designer HPS Component.

HPS JTAG Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 19. HPS JTAG Pins—Preliminary

You have the option to connect HPS JTAG pins to the HPS Dedicated I/O using the following assignments.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
JTAG_TCK	HPS JTAG test clock input pin. Connect this pin through a 1-kΩ – 10-kΩ pull-down resistor to GND. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_9
JTAG_TMS	HPS JTAG test mode select input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_10
JTAG_TDO	HPS JTAG test data output pin. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Output	HPS_IOB_11
JTAG_TDI	HPS JTAG test data input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_12

HPS GPIO Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 20. HPS GPIO Pins—Preliminary

There are two GPIO controllers (GPIO0 and GPIO1) for the Intel Stratix 10 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
GPIO0_IO[0..23]	General purpose input output. Ensure that the I/O standard used is compatible with VCCIO_HPS.	I/O	HPS_IOA_[1..24] HPS_IOB_[1..24]
GPIO1_IO[0..23]			

HPS SDMMC Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 21. HPS SDMMC Pins—Preliminary

Intel recommends adding a 1-kΩ to 10-kΩ pull-up resistor to every SDMMC data signal that is used.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
SDMMC_CCLK	SDMMC clock out	Output	HPS_IOA_1	HPS_IOB_15
SDMMC_CMD	SDMMC command line Pull this pin high on the board with a weak pull-up resistor. For example, a 10-kΩ to VCCIO_HPS.	I/O	HPS_IOA_2	HPS_IOB_14
SDMMC_DATA0	SDMMC Data 0	I/O	HPS_IOA_3	HPS_IOB_13
SDMMC_DATA1	SDMMC Data 1	I/O	HPS_IOA_4	HPS_IOB_16
SDMMC_DATA2	SDMMC Data 2	I/O	HPS_IOA_5	HPS_IOB_17
SDMMC_DATA3	SDMMC Data 3 When using SD card, there is an existing 50-kΩ pull-up on SDMMC Data Bit 3 which can be disabled in the Intel Quartus Prime software by using the	I/O	HPS_IOA_6	HPS_IOB_18

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HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
	SET_CLR_CARD_DETECT (ACMD42) command. This is not applicable to the eMMC flash.			
SDMMC_DATA4	SDMMC Data 4	I/O	HPS_IOA_7	HPS_IOB_19
SDMMC_DATA5	SDMMC Data 5	I/O	HPS_IOA_8	HPS_IOB_20
SDMMC_DATA6	SDMMC Data 6	I/O	HPS_IOA_9	HPS_IOB_21
SDMMC_DATA7	SDMMC Data 7	I/O	HPS_IOA_10	HPS_IOB_22
SDMMC_PWR_EN	SDMMC Power Enable	Output	HPS_IOA_11	HPS_IOB_23

HPS NAND Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 22. HPS NAND Pins—Preliminary

HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
NAND_ADQ0	NAND Data Bit 0	I/O	HPS_IOA_1	HPS_IOB_1
NAND_ADQ1	NAND Data Bit 1	I/O	HPS_IOA_2	HPS_IOB_2
NAND_WE_N	NAND Write Enable See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_3	HPS_IOB_3
NAND_RE_N	NAND Read Enable See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_4	HPS_IOB_4

continued...

HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
NAND_WP_N	NAND Write Protect	Output	HPS_IOA_5	HPS_IOB_5
NAND_ADQ2	NAND Data Bit 2	I/O	HPS_IOA_6	HPS_IOB_6
NAND_ADQ3	NAND Data Bit 3	I/O	HPS_IOA_7	HPS_IOB_7
NAND_CLE	NAND Command Latch Enable	Output	HPS_IOA_8	HPS_IOB_8
NAND_ADQ4	NAND Data Bit 4	I/O	HPS_IOA_9	HPS_IOB_9
NAND_ADQ5	NAND Data Bit 5	I/O	HPS_IOA_10	HPS_IOB_10
NAND_ADQ6	NAND Data Bit 6	I/O	HPS_IOA_11	HPS_IOB_11
NAND_ADQ7	NAND Data Bit 7	I/O	HPS_IOA_12	HPS_IOB_12
NAND_ALE	NAND Address Latch Enable	Output	HPS_IOA_13	HPS_IOB_13
NAND_RB	NAND Ready/Busy Connect this pin through a 1-kΩ to 10-kΩ pull-up resistor to VCCIO_HPS.	Input	HPS_IOA_14	HPS_IOB_14
NAND_CE_N	NAND Chip Enable See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_15	HPS_IOB_15
NAND_ADQ8	NAND Data Bit 8	I/O	HPS_IOA_17	HPS_IOB_17
NAND_ADQ9	NAND Data Bit 9	I/O	HPS_IOA_18	HPS_IOB_18
NAND_ADQ10	NAND Data Bit 10	I/O	HPS_IOA_19	HPS_IOB_19
NAND_ADQ11	NAND Data Bit 11	I/O	HPS_IOA_20	HPS_IOB_20
NAND_ADQ12	NAND Data Bit 12	I/O	HPS_IOA_21	HPS_IOB_21
NAND_ADQ13	NAND Data Bit 13	I/O	HPS_IOA_22	HPS_IOB_22
NAND_ADQ14	NAND Data Bit 14	I/O	HPS_IOA_23	HPS_IOB_23
NAND_ADQ15	NAND Data Bit 15	I/O	HPS_IOA_24	HPS_IOB_24

HPS USB Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 23. HPS USB Pins—Preliminary

There are two USB controllers (USB0 and USB1) for the Intel Stratix 10 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB0_CLK	USB0 Clock	Input	HPS_IOA_1
USB0_STP	USB0 Stop Data	Output	HPS_IOA_2
USB0_DIR	USB0 Direction	Input	HPS_IOA_3
USB0_DATA0	USB0 Data Bit 0	I/O	HPS_IOA_4
USB0_DATA1	USB0 Data Bit 1	I/O	HPS_IOA_5
USB0_NXT	USB0 Next Data	Input	HPS_IOA_6
USB0_DATA2	USB0 Data Bit 2	I/O	HPS_IOA_7
USB0_DATA3	USB0 Data Bit 3	I/O	HPS_IOA_8
USB0_DATA4	USB0 Data Bit 4	I/O	HPS_IOA_9
USB0_DATA5	USB0 Data Bit 5	I/O	HPS_IOA_10
USB0_DATA6	USB0 Data Bit 6	I/O	HPS_IOA_11
USB0_DATA7	USB0 Data Bit 7	I/O	HPS_IOA_12
USB1_CLK	USB1 Clock	Input	HPS_IOA_13
USB1_STP	USB1 Stop Data	Output	HPS_IOA_14
USB1_DIR	USB1 Direction	Input	HPS_IOA_15
USB1_DATA0	USB1 Data Bit 0	I/O	HPS_IOA_16
USB1_DATA1	USB1 Data Bit 1	I/O	HPS_IOA_17

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB1_NXT	USB1 Next Data	Input	HPS_IOA_18
USB1_DATA2	USB1 Data Bit 2	I/O	HPS_IOA_19
USB1_DATA3	USB1 Data Bit 3	I/O	HPS_IOA_20
USB1_DATA4	USB1 Data Bit 4	I/O	HPS_IOA_21
USB1_DATA5	USB1 Data Bit 5	I/O	HPS_IOA_22
USB1_DATA6	USB1 Data Bit 6	I/O	HPS_IOA_23
USB1_DATA7	USB1 Data Bit 7	I/O	HPS_IOA_24

HPS EMAC Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 24. HPS EMAC Pins—Preliminary

There are three EMAC controllers (EMAC0, EMAC1, and EMAC2) for the Intel Stratix 10 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC0_TX_CLK	EMAC0 Transmit Clock	Output	HPS_IOA_13
EMAC0_TX_CTL	EMAC0 Transmit Control	Output	HPS_IOA_14
EMAC0_RX_CLK	EMAC0 Receive Clock	Input	HPS_IOA_15
EMAC0_RX_CTL	EMAC0 Receive Control	Input	HPS_IOA_16
EMAC0_TXD0	EMAC0 Transmit Data Bit 0	Output	HPS_IOA_17
EMAC0_TXD1	EMAC0 Transmit Data Bit 1	Output	HPS_IOA_18
EMAC0_RXD0	EMAC0 Receive Data Bit 0	Input	HPS_IOA_19

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC0_RXD1	EMAC0 Receive Data Bit 1	Input	HPS_IOA_20
EMAC0_TXD2	EMAC0 Transmit Data Bit 2	Output	HPS_IOA_21
EMAC0_TXD3	EMAC0 Transmit Data Bit 3	Output	HPS_IOA_22
EMAC0_RXD2	EMAC0 Receive Data Bit 2	Input	HPS_IOA_23
EMAC0_RXD3	EMAC0 Receive Data Bit 3	Input	HPS_IOA_24
EMAC1_TX_CLK	EMAC1 Transmit Clock	Output	HPS_IOB_1
EMAC1_TX_CTL	EMAC1 Transmit Control	Output	HPS_IOB_2
EMAC1_RX_CLK	EMAC1 Receive Clock	Input	HPS_IOB_3
EMAC1_RX_CTL	EMAC1 Receive Control.	Input	HPS_IOB_4
EMAC1_TXD0	EMAC1 Transmit Data Bit 0	Output	HPS_IOB_5
EMAC1_TXD1	EMAC1 Transmit Data Bit 1	Output	HPS_IOB_6
EMAC1_RXD0	EMAC1 Receive Data Bit 0	Input	HPS_IOB_7
EMAC1_RXD1	EMAC1 Receive Data Bit 1	Input	HPS_IOB_8
EMAC1_TXD2	EMAC1 Transmit Data Bit 2	Output	HPS_IOB_9
EMAC1_TXD3	EMAC1 Transmit Data Bit 3	Output	HPS_IOB_10
EMAC1_RXD2	EMAC1 Receive Data Bit 2	Input	HPS_IOB_11
EMAC1_RXD3	EMAC1 Receive Data Bit 3	Input	HPS_IOB_12
EMAC2_TX_CLK	EMAC2 Transmit Clock	Output	HPS_IOB_13
EMAC2_TX_CTL	EMAC2 Transmit Control	Output	HPS_IOB_14
EMAC2_RX_CLK	EMAC2 Receive Clock	Input	HPS_IOB_15
EMAC2_RX_CTL	EMAC2 Receive Control	Input	HPS_IOB_16
EMAC2_TXD0	EMAC2 Transmit Data Bit 0	Output	HPS_IOB_17
EMAC2_TXD1	EMAC2 Transmit Data Bit 1	Output	HPS_IOB_18

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC2_RXD0	EMAC2 Receive Data Bit 0	Input	HPS_IOB_19
EMAC2_RXD1	EMAC2 Receive Data Bit 1	Input	HPS_IOB_20
EMAC2_TXD2	EMAC2 Transmit Data Bit 2	Output	HPS_IOB_21
EMAC2_TXD3	EMAC2 Transmit Data Bit 3	Output	HPS_IOB_22
EMAC2_RXD2	EMAC2 Receive Data Bit 2	Input	HPS_IOB_23
EMAC2_RXD3	EMAC2 Receive Data Bit 3	Input	HPS_IOB_24

HPS I2C_EMAC and MDIO Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

There are three sets of I2C_EMAC interfaces that can be used as I2C interfaces or as the MDIO pins for the EMACs. You must take note that the I2C_EMAC and MDIO modules must be used with the corresponding EMAC interfaces. For example, you can use either I2C_EMAC0_SDA and I2C_EMAC0_SCL or MDIO0_MDIO and MDIO0_MDC with EMAC0.

The I2C protocol requires pull-up resistors to VCCIO_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7-kΩ or lower.

Typically the MDIO pin requires an external pull-up resistor to VCCIO_HPS in the range of 1.0-kΩ to 4.7-kΩ.

Table 25. HPS I2C_EMAC and MDIO Pins—Preliminary

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
I2C_EMAC2_SDA	I2C EMAC2 Serial Data	I/O	HPS_IOA_7	HPS_IOB_9	HPS_IOB_21
I2C_EMAC2_SCL	I2C EMAC2 Serial Clock	I/O	HPS_IOA_8	HPS_IOB_10	HPS_IOB_22
I2C_EMAC1_SDA	I2C EMAC1 Serial Data	I/O	HPS_IOA_9	HPS_IOB_19	—

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
I2C_EMAC1_SCL	I2C EMAC1 Serial Clock	I/O	HPS_IOA_10	HPS_IOB_20	—
I2C_EMAC0_SDA	I2C EMAC0 Serial Data	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
I2C_EMAC0_SCL	I2C EMAC0 Serial Clock	I/O	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24
MDIO2_MDIO	EMAC2 MDIO	I/O	HPS_IOA_7	HPS_IOB_9	—
MDIO2_MDC	EMAC2 MDC	Output	HPS_IOA_8	HPS_IOB_10	—
MDIO1_MDIO	EMAC1 MDIO	I/O	HPS_IOA_9	HPS_IOB_19	—
MDIO1_MDC	EMAC1 MDC	Output	HPS_IOA_10	HPS_IOB_20	—
MDIO0_MDIO	EMAC0 MDIO	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
MDIO0_MDC	EMAC0 MDC	Output	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24

HPS I2C Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

In addition to the three I2C_EMAC controllers, there are two additional I2C controllers (I2C0 and I2C1) for dedicated I2C usage in the Intel Stratix 10 HPS.

The I2C protocol requires pull-up resistors to VCCIO_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7-kΩ or lower.

Table 26. HPS I2C Pins—Preliminary

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)			
			Group 1	Group 2	Group 3	Group 4
I2C0 _SDA	I2C0 Serial Data	I/O	HPS_IOA_5	HPS_IOA_23	HPS_IOB_3	—
I2C0 _SCL	I2C0 Serial Clock	I/O	HPS_IOA_6	HPS_IOA_24	HPS_IOB_4	—
I2C1 _SDA	I2C1 Serial Data	I/O	HPS_IOA_3	HPS_IOA_21	HPS_IOB_7	HPS_IOB_13
I2C1 _SCL	I2C1 Serial Clock	I/O	HPS_IOA_4	HPS_IOA_22	HPS_IOB_8	HPS_IOB_14

HPS SPI Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 27. HPS SPI Pins—Preliminary

There are two SPI Master (SPIM0 and SPIM1) and two SPI Slave (SPIS0 and SPIS1) controllers for the Intel Stratix 10 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIM0_CLK	SPIM0 Clock	Output	HPS_IOA_5	HPS_IOB_21	HPS_IOB_21
SPIM0_MOSI	SPIM0 Master Out Slave In	Output	HPS_IOA_6	HPS_IOB_22	HPS_IOB_22
SPIM0_MISO	SPIM0 Master In Slave Out	Input	HPS_IOA_7	HPS_IOB_19	HPS_IOB_23
SPIM0_SS0_N	SPIM0 Slave Select 0 See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_8	HPS_IOB_20	HPS_IOB_24
SPIM0_SS1_N	SPIM0 Slave Select 1 See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_1	HPS_IOB_18	HPS_IOB_18

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIM1_CLK	SPIM1 Clock	Output	HPS_IOA_9	HPS_IOA_21	HPS_IOB_1
SPIM1_MOSI	SPIM1 Master Out Slave In	Output	HPS_IOA_10	HPS_IOA_22	HPS_IOB_2
SPIM1_MISO	SPIM1 Master In Slave Out	Input	HPS_IOA_11	HPS_IOA_23	HPS_IOB_3
SPIM1_SS0_N	SPIM1 Slave Select 0 See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_12	HPS_IOA_24	HPS_IOB_4
SPIM1_SS1_N	SPIM1 Slave Select 1 See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_2	HPS_IOA_20	HPS_IOB_5
SPIS0_CLK	SPIS0 Clock	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_9
SPIS0_MOSI	SPIS0 Master Out Slave In	Input	HPS_IOA_2	HPS_IOA_22	HPS_IOB_10
SPIS0_MISO	SPIS0 Master In Slave Out	Output	HPS_IOA_4	HPS_IOA_24	HPS_IOB_12
SPIS0_SS0_N	SPIS0 Slave Select 0 See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Input	HPS_IOA_3	HPS_IOA_23	HPS_IOB_11
SPIS1_CLK	SPIS1 Clock	Input	HPS_IOA_9	HPS_IOB_5	HPS_IOB_21
SPIS1_MOSI	SPIS1 Master Out Slave In	Input	HPS_IOA_10	HPS_IOB_6	HPS_IOB_22
SPIS1_MISO	SPIS1 Master In Slave Out	Output	HPS_IOA_12	HPS_IOB_8	HPS_IOB_23
SPIS1_SS0_N	SPIS1 Slave Select 0 See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Input	HPS_IOA_11	HPS_IOB_7	HPS_IOB_24

HPS UART Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 28. HPS UART Pins—Preliminary

There are two UART (UART0 and UART1) controllers for the Intel Stratix 10 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
UART0_CTS_N	UART0 Clear to Send See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_1
UART0_RTS_N	UART0 Request to Send See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_2	HPS_IOA_22	HPS_IOB_2
UART0_TX	UART0 Transmit	Output	HPS_IOA_3	HPS_IOA_23	HPS_IOB_3
UART0_RX	UART0 Receive	Input	HPS_IOA_4	HPS_IOA_24	HPS_IOB_4
UART1_CTS_N	UART1 Clear to Send See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Input	HPS_IOA_5	HPS_IOB_5	HPS_IOB_17
UART1_RTS_N	UART1 Request to Send See Note 11 in Notes to Intel Stratix 10 SX Pin Connection Guidelines.	Output	HPS_IOA_6	HPS_IOB_6	HPS_IOB_18
UART1_TX	UART1 Transmit	Output	HPS_IOA_7	HPS_IOB_7	HPS_IOB_15
UART1_RX	UART1 Receive	Input	HPS_IOA_8	HPS_IOB_8	HPS_IOB_16

HPS Trace Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 29. HPS Trace Pins—Preliminary

You can select up to 16 trace output pins in the Intel Stratix 10 HPS. These pins do not have to be located in the same quadrant.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
Trace_CLK	Trace Clock	Output	HPS_IOA_20
			HPS_IOB_20
Trace_D0	Trace Data 0	Output	HPS_IOA_21
			HPS_IOB_21
Trace_D1	Trace Data 1	Output	HPS_IOA_22
			HPS_IOB_22
Trace_D2	Trace Data 2	Output	HPS_IOA_23
			HPS_IOB_23
Trace_D3	Trace Data 3	Output	HPS_IOA_24
			HPS_IOB_24
Trace_D4	Trace Data 4	Output	HPS_IOA_19
			HPS_IOA_7
			HPS_IOB_19
			HPS_IOB_7
Trace_D5	Trace Data 5	Output	HPS_IOA_18
			HPS_IOA_6
			HPS_IOB_18

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
			HPS_IOB_6
Trace_D6	Trace Data 6	Output	HPS_IOA_17
			HPS_IOA_5
			HPS_IOB_17
			HPS_IOB_5
Trace_D7	Trace Data 7	Output	HPS_IOA_16
			HPS_IOA_4
			HPS_IOB_16
			HPS_IOB_4
Trace_D8	Trace Data 8	Output	HPS_IOA_15
			HPS_IOA_3
			HPS_IOB_15
			HPS_IOB_3
Trace_D9	Trace Data 9	Output	HPS_IOA_14
			HPS_IOA_2
			HPS_IOB_14
			HPS_IOB_2
Trace_D10	Trace Data 10	Output	HPS_IOA_13
			HPS_IOA_1
			HPS_IOB_13
			HPS_IOB_1
Trace_D11	Trace Data 11	Output	HPS_IOA_12
			HPS_IOB_12
Trace_D12	Trace Data 12	Output	HPS_IOA_11

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
			HPS_IOB_11
Trace_D13	Trace Data 13	Output	HPS_IOA_10
			HPS_IOB_10
Trace_D14	Trace Data 14	Output	HPS_IOA_9
			HPS_IOB_9
Trace_D15	Trace Data 15	Output	HPS_IOA_8
			HPS_IOB_8

Notes to Intel Stratix 10 SX Pin Connection Guidelines

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are based on the Intel Stratix 10 SX device variant.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA must have its own dedicated breakout via.

6. Low Noise Switching Regulator - a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response. The switching frequency range is not an Intel requirement.
7. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the *Intel Stratix 10 General Purpose I/O User Guide*.
8. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires that the AC-coupling capacitor is placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
9. For item [#], refer to the device pin table for the pin-out mapping.
10. The peripheral pins are programmable through pin multiplexors. Each pin may have multiple functions. HPS and SDM dedicated I/O pin multiplexing is programmable using the Quartus Prime software. The pin mux determines how the pins are used.
11. These pins are inverted or active-low signals.
12. Example 3 through Example 6 illustrate the power supply sharing guidelines for the Intel Stratix 10 SX devices.

Power Supply Sharing Guidelines for Intel Stratix 10 Devices

Intel Stratix 10 devices have specific power-up and power-down sequence requirements. For more information, refer to the *AN692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria® 10, and Intel Stratix 10 Devices* and *Intel Stratix 10 Power Management User Guide*.

Related Information

- AN692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
- Intel Stratix 10 Power Management User Guide

Example 1—Intel Stratix 10 GX

Table 30. Power Supply Sharing Guidelines for Intel Stratix 10 GX with Transceiver Data Rate <= 15 Gbps—Preliminary

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.85 SmartVID	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane.
VCCP						
VCCERAM	2	0.9	± 30mV	Switcher (*)	Share	Connect the VCCERAM to a dedicated 0.9V power supply. You may connect the VCCPLLDIG_SDM power to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCR_GXB[L,R]	3	1.03	± 30mV	Switcher (*)	Share	You have the option to source the VCCR_GXB and VCCT_GXB from the same regulator when all the power rails require the same voltage level. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCT_GXB[L,R]						
VCCPT	4	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, and VCCADC to the same power plane
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCBAT		Varies				with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	5	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

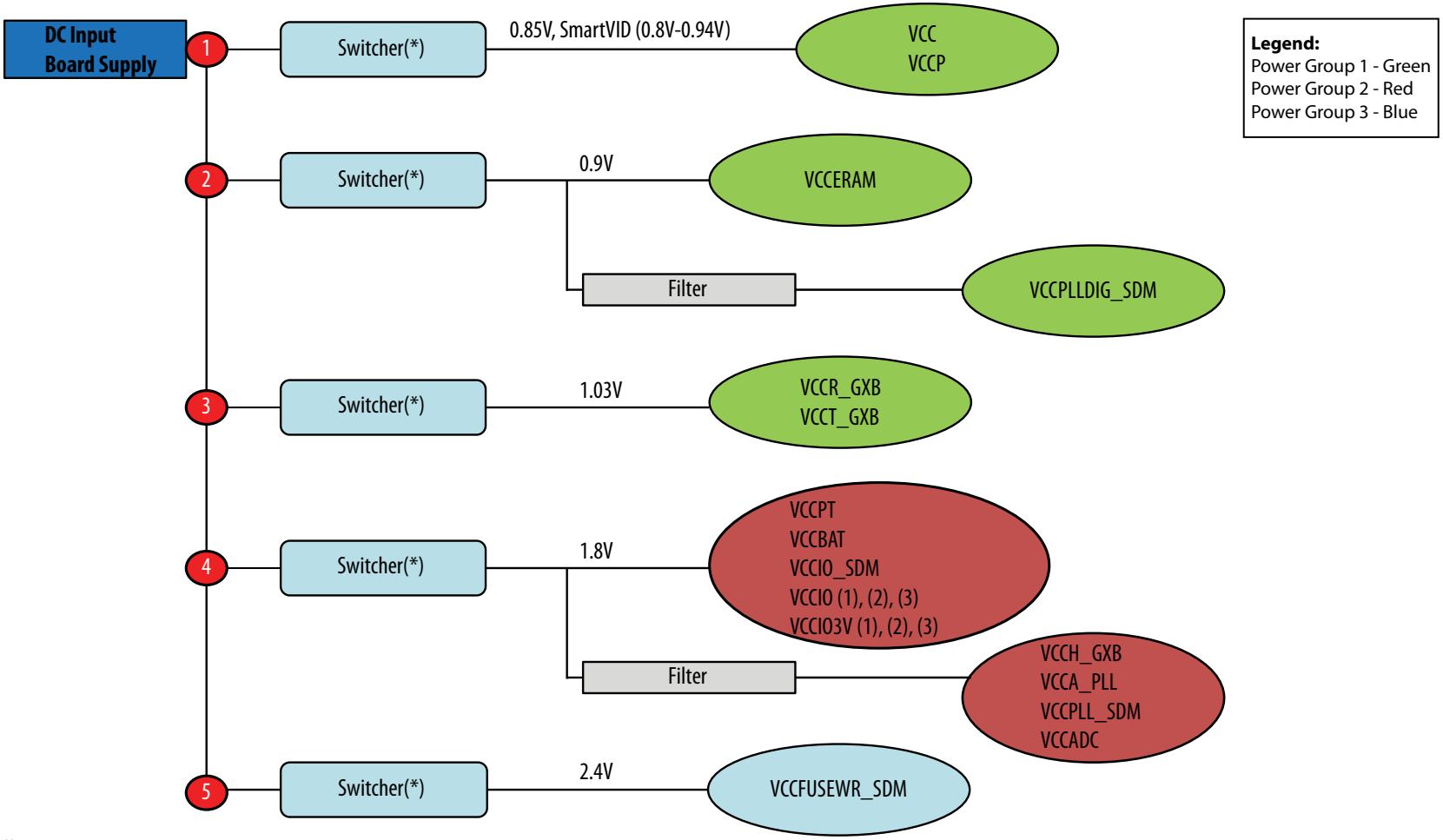
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Stratix 10 GX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 GX device is provided in Figure 1.

The voltage level for each power rail is preliminary.

Figure 1. Example Power Supply Sharing Guidelines for Intel Stratix 10 GX with Transceiver Data Rate ≤ 15 Gbps—Preliminary



Notes:
(1) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.
(2) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.
(3) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.
(4) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT pin function.

Example 2—Intel Stratix 10 GX

Table 31. Power Supply Sharing Guidelines for Intel Stratix 10 GX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps—Preliminary

Example Requiring 6 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.85 SmartVID	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane.
VCCP						
VCCERAM	2	0.9	± 30mV	Switcher (*)	Isolate	Connect the VCCERAM to a dedicated 0.9V power supply. You may connect the VCCPLLDIG_SDM power to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCR_GXB[L,R]	3	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCR_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCT_GXB[L,R]	4	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCT_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCPT	5	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, and VCCADC to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCBAT		Varies				
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	6	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

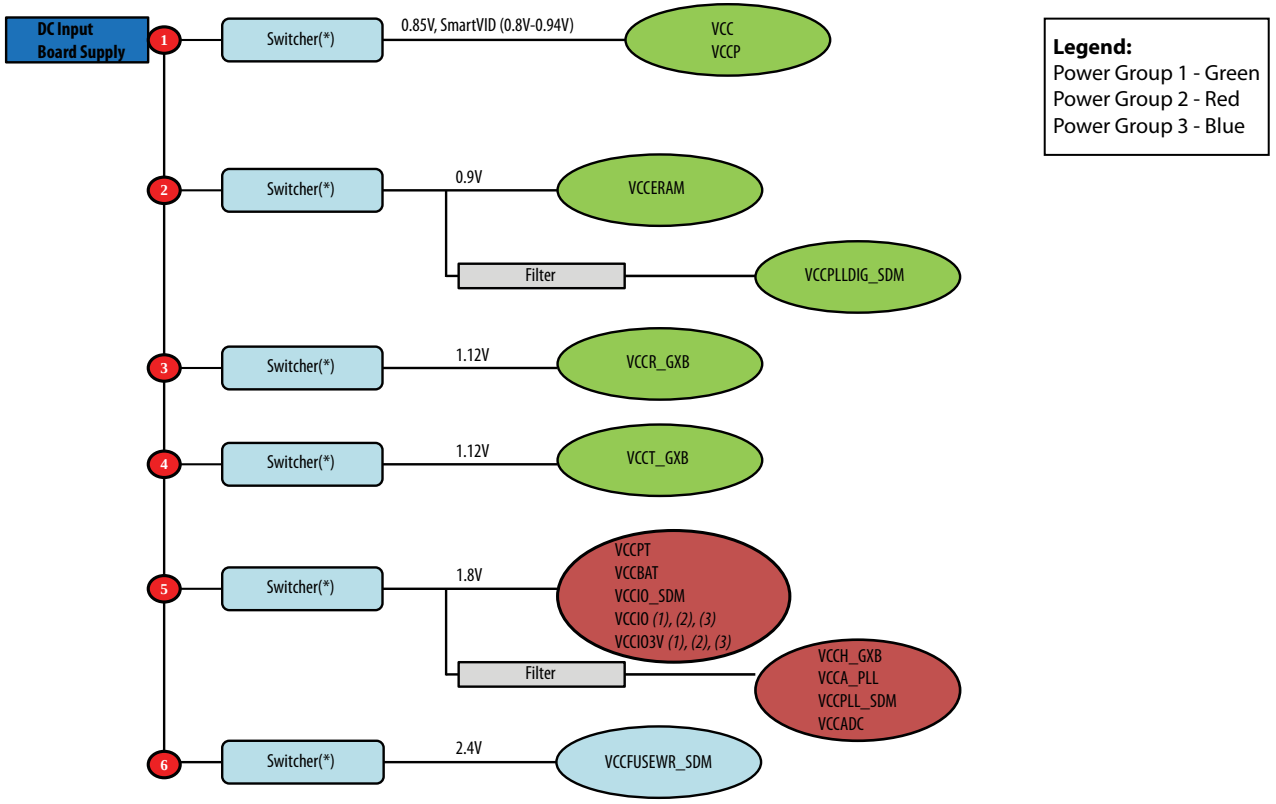
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Stratix 10 GX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 GX device is provided in Figure 2.

The voltage level for each power rail is preliminary.

Figure 2. Example Power Supply Sharing Guidelines for Intel Stratix 10 GX with 15 Gbps < Transceiver Data Rate ≤ 28.3 Gbps—Preliminary



Notes:

(1) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.

(2) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.

(3) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.

(4) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT pin function.

Example 3—Intel Stratix 10 SX (–1V, –2V, and –3V parts)

Table 32. Power Supply Sharing Guidelines for Intel Stratix 10 SX (–1V, –2V, and –3V parts) with Transceiver Data Rate <= 15 Gbps—Preliminary

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCP						
VCCL_HPS						
VCCPLLDIG_HPS					Filter	
VCCERAM	2	0.9	± 30mV	Switcher (*)	Isolate	Connect the VCCERAM to a dedicated 0.9V power supply. You may connect the VCCPLLDIG_SDM power to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCR_GXB[L,R]	3	1.03	± 30mV	Switcher (*)	Share	You have the option to source the VCCR_GXB and VCCT_GXB from the same regulator when all the power rails require the same voltage level. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth.
VCCT_GXB[L,R]						

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCPT	4	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND.
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				
VCCBAT		Varies				
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	5	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

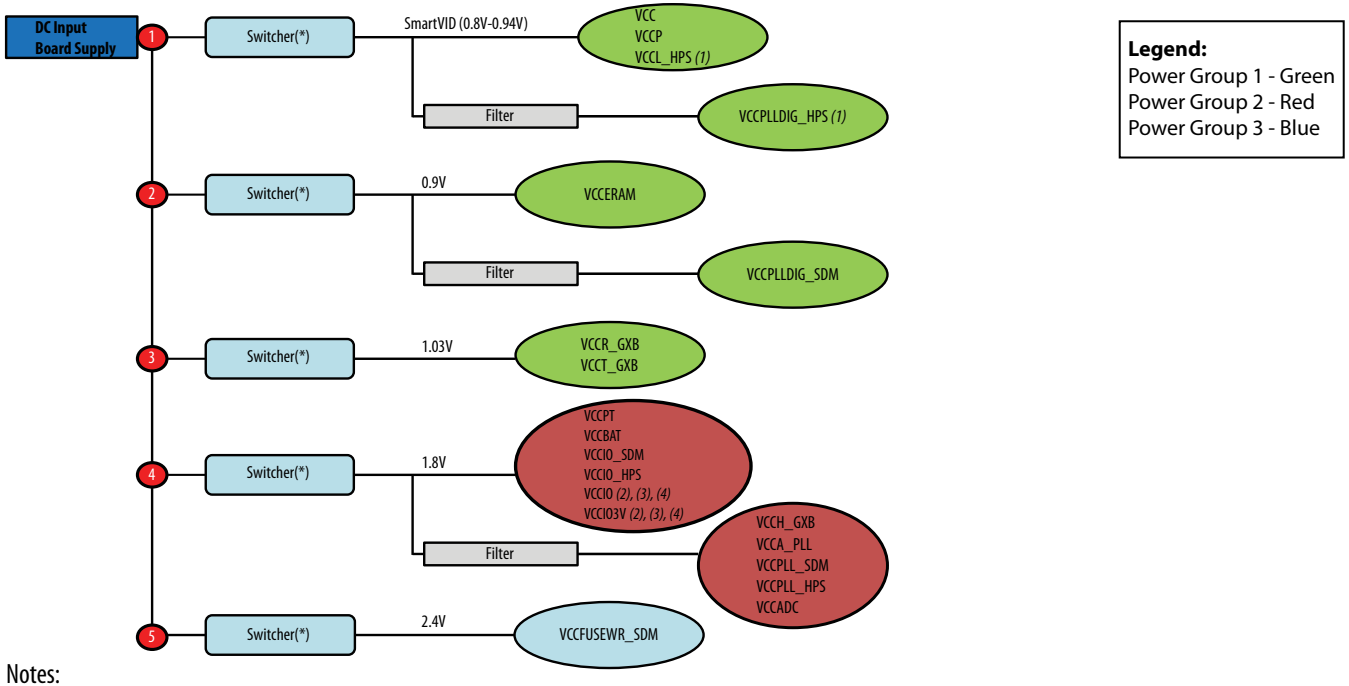
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 6 of the *Notes to Intel Stratix 10 SX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 SX device is provided in Figure 3.

The voltage level for each power rail is preliminary.

Figure 3. Example Power Supply Sharing Guidelines for Intel Stratix 10 SX (–1V, –2V, and –3V parts) with Transceiver Data Rate <= 15 Gbps—Preliminary



Notes:

(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator. Optionally, you can connect VCCL_HPS and VCCPLLDIG_HPS to a fixed 0.9V. If you are connecting VCCL_HPS and VCCPLLDIG_HPS to 0.9V, they can share the same power regulator with VCCERAM.

(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.

(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.

(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.

(5) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT pin function.

Example 4—Intel Stratix 10 SX (–2L and –3X parts)

Table 33. Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with Transceiver Data Rate <= 15 Gbps—Preliminary

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCP	1	0.85	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCERAM VCCL_HPS VCCPLLDIG_SDM VCCPLLDIG_HPS	2	0.9	± 30mV	Switcher (*)	Share Filter	Connect the VCCERAM to a dedicated 0.9V power supply. You have the option to connect VCCL_HPS to the same regulator as VCCERAM when the power rails require the same voltage level. You may also connect the VCCPLLDIG_SDM and VCCPLLDIG_HPS power rails to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCR_GXB[L,R] VCCT_GXB[L,R]	3	1.03	± 30mV	Switcher (*)	Share	You have the option to source the VCCR_GXB and VCCT_GXB from the same regulator when all the power rails require the same voltage level. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCPT	4	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND.
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				
VCCBAT		Varies				
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	5	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

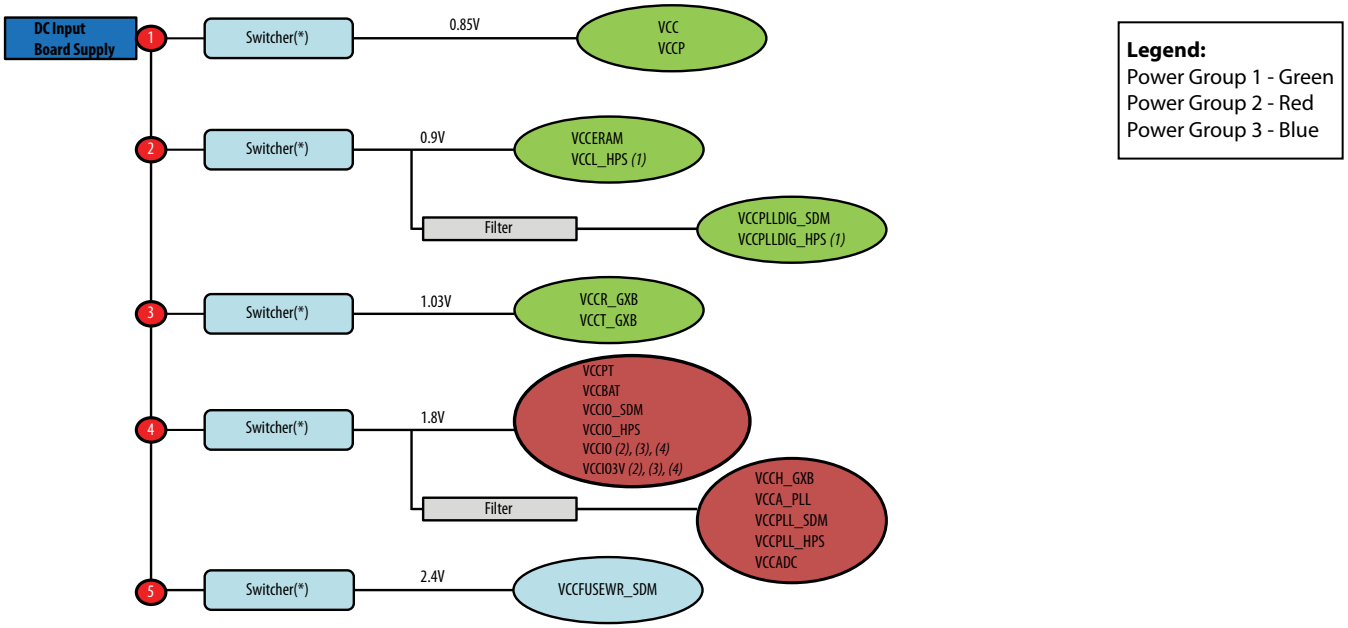
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 6 of the *Notes to Intel Stratix 10 SX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 SX device is provided in Figure 4.

The voltage level for each power rail is preliminary.

Figure 4. Example Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with Transceiver Data Rate <= 15 Gbps—Preliminary



Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator.
(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.
(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.
(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.

Example 5—Intel Stratix 10 SX (–1V, –2V, and –3V parts)

Table 34. Power Supply Sharing Guidelines for Intel Stratix 10 SX (–1V, –2V, and –3V parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps—Preliminary

Example Requiring 6 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCP						
VCCL_HPS						
VCCPLLDIG_HPS					Filter	
VCCERAM	2	0.9	± 30mV	Switcher (*)	Isolate	Connect the VCCERAM to a dedicated 0.9V power supply. You may connect the VCCPLLDIG_SDM power to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCR_GXB[L,R]	3	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCR_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCT_GXB[L,R]	4	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCT_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCPT	5	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND.
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				
VCCBAT		Varies				
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	6	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

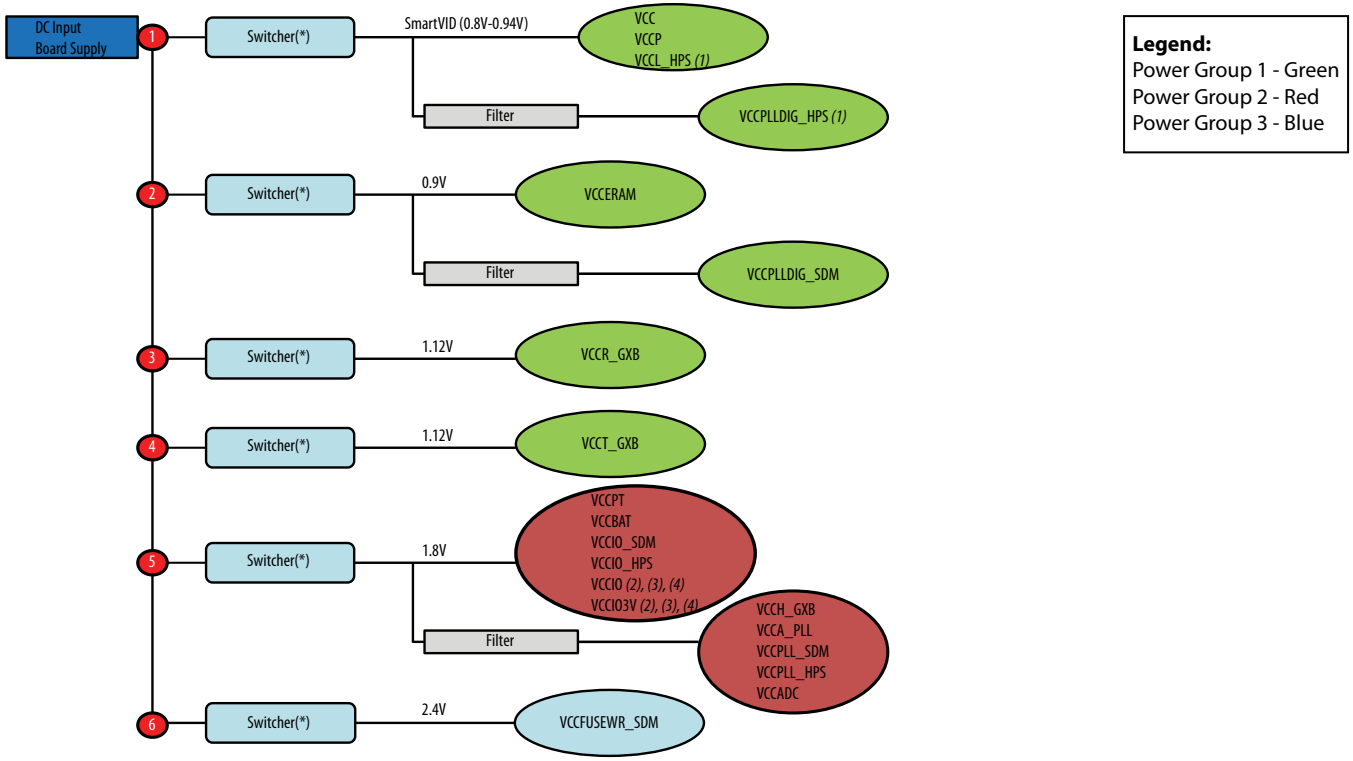
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 6 of the *Notes to Intel Stratix 10 SX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 SX device is provided in Figure 5.

The voltage level for each power rail is preliminary.

Figure 5. Example Power Supply Sharing Guidelines for Intel Stratix 10 SX (–1V, –2V, and –3V parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps—Preliminary



Notes:

(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator. Optionally, you can connect VCCL_HPS and VCCPLLDIG_HPS to a fixed 0.9V. If you are connecting VCCL_HPS and VCCPLLDIG_HPS to 0.9V, they can share the same power regulator with VCCERAM.

(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.

(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.

(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.

(5) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT pin function.

Example 6—Intel Stratix 10 SX (–2L and –3X parts)

Table 35. Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps—Preliminary

Example Requiring 6 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCP	1	0.85	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCERAM VCCL_HPS VCCPLLDIG_SDM VCCPLLDIG_HPS	2	0.9	± 30mV	Switcher (*)	Share Filter	Connect the VCCERAM to a dedicated 0.9V power supply. You have the option to connect VCCL_HPS to the same regulator as VCCERAM when the power rails require the same voltage level. You may also connect the VCCPLLDIG_SDM and VCCPLLDIG_HPS power rails to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCR_GXB[L,R]	3	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCR_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCT_GXB[L,R]	4	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCT_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCPT	5	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND.
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				
VCCBAT		Varies				
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	6	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

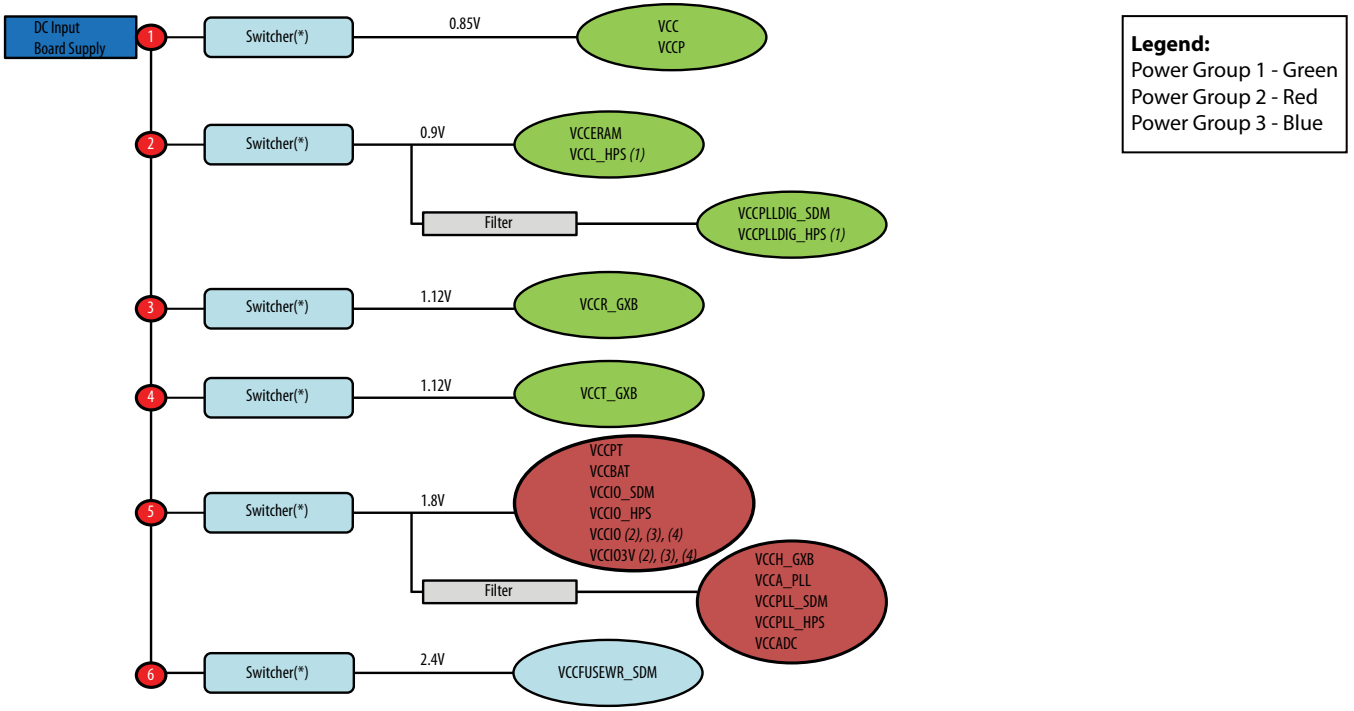
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 6 of the *Notes to Intel Stratix 10 SX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 SX device is provided in Figure 6.

The voltage level for each power rail is preliminary.

Figure 6. Example Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps—Preliminary



Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator.
(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.
(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.
(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.

Example 7—Intel Stratix 10 MX (–1V, –2V, and –3V parts)

Table 36. Power Supply Sharing Guidelines for Intel Stratix 10 MX (–1V, –2V, and –3V parts) with Transceiver Data Rate <= 15 Gbps—Preliminary

Example Requiring 7 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 MX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCP						
VCCL_HPS						
VCCPLLDIG_HPS					Filter	
VCCERAM	2	0.9	± 30mV	Switcher (*)	Isolate	Connect the VCCERAM to a dedicated 0.9V power supply. You may connect the VCCPLLDIG_SDM power to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCR_GXB[L,R]	3	1.03	± 30mV	Switcher (*)	Share	You have the option to source the VCCR_GXB and VCCT_GXB from the same regulator when all the power rails require the same voltage level. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth.
VCCT_GXB[L,R]						

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCPT	4	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. If you do not intend to utilize the HPS in the Intel Stratix 10 MX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				
VCCBAT		Varies				
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				
VCCM_WORD_(BL,TL)	5	2.5	± 100mV	Switcher (*)	Share	Connect VCCM_WORD_(BL,TL) to a 2.5V power supply. You have the option to share VCCM_WORD_(BL,TL) with other 2.5V power supplies such as 2.5V VCCIO, if applicable.
VCCIO_UIB_(BL,TL)	6	1.2	± 30mV	Switcher (*)	Isolate	Connect VCCIO_UIB_(BL,TL) to a 1.2V power supply.
VCCFUSEWR_SDM	7	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

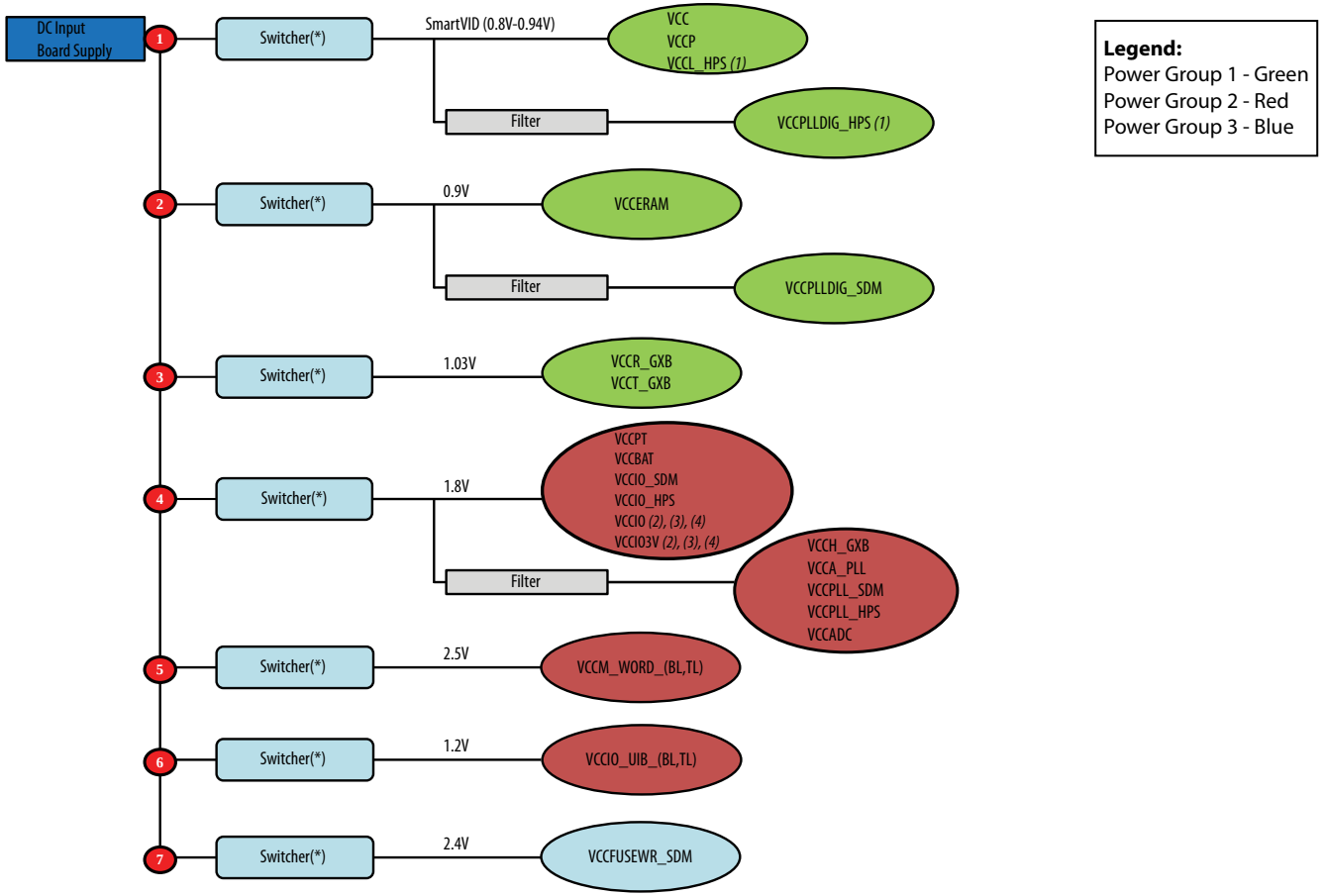
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 7 of the *Notes to Intel Stratix 10 MX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 MX device is provided in Figure 7.

The voltage level for each power rail is preliminary.

Figure 7. Example Power Supply Sharing Guidelines for Intel Stratix 10 MX (–1V, –2V, and –3V parts) with Transceiver Data Rate <= 15 Gbps—Preliminary



Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator. Optionally, you can connect VCCL_HPS and VCCPLLDIG_HPS to a fixed 0.9V. If you are connecting VCCL_HPS and VCCPLLDIG_HPS to 0.9V, they can share the same power regulator with VCCERAM.
(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.
(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.
(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.
(5) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT pin function.

Example 8—Intel Stratix 10 MX (–1V, –2V, and –3V parts)

Table 37. Power Supply Sharing Guidelines for Intel Stratix 10 MX (–1V, –2V, and –3V parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps—Preliminary

Example Requiring 8 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 MX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCP						
VCCL_HPS						
VCCPLLDIG_HPS					Filter	
VCCERAM	2	0.9	± 30mV	Switcher (*)	Isolate	Connect the VCCERAM to a dedicated 0.9V power supply. You may connect the VCCPLLDIG_SDM power to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCR_GXB[L,R]	3	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCR_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCT_GXB[L,R]	4	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCT_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCPT	5	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. If you do not intend to utilize the HPS in the Intel Stratix 10 MX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				
VCCBAT		Varies				
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCM_WORD_(BL, TL)	6	2.5	± 100mV	Switcher (*)	Share	Connect VCCM_WORD_(BL,TL) to a 2.5V power supply. You have the option to share VCCM_WORD_(BL,TL) with other 2.5V power supplies such as 2.5V VCCIO, if applicable.
VCCIO_UIB_(BL, TL)	7	1.2	± 30mV	Switcher (*)	Isolate	Connect VCCIO_UIB_(BL,TL) to a 1.2V power supply.
VCCFUSEWR_SDM	8	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

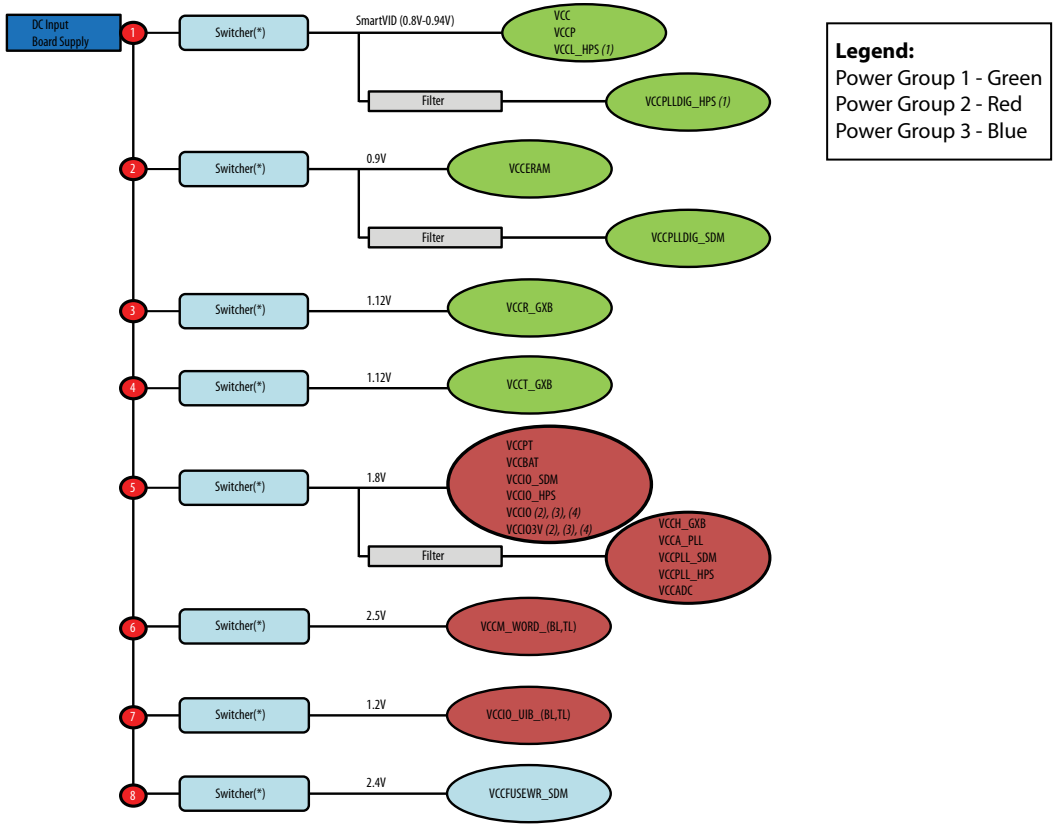
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 7 of the *Notes to Intel Stratix 10 MX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 MX device is provided in Figure 8.

The voltage level for each power rail is preliminary.

Figure 8. Example Power Supply Sharing Guidelines for Intel Stratix 10 MX (–1V, –2V, and –3V parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps—Preliminary



Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator. Optionally, you can connect VCCL_HPS and VCCPLLDIG_HPS to a fixed 0.9V. If you are connecting VCCL_HPS and VCCPLLDIG_HPS to 0.9V, they can share the same power regulator with VCCERAM.
(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.
(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.
(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.
(5) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT pin function.

Example 9—Intel Stratix 10 TX (–1V, –2V, and –3V parts)

Table 38. Power Supply Sharing Guidelines for Intel Stratix 10 TX (–1V, –2V, and –3V parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps—Preliminary

Example Requiring 8 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 TX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCP						
VCCL_HPS						
VCCPLLDIG_HPS					Filter	
VCCERAM	2	0.9	± 30mV	Switcher (*)	Isolate	Connect the VCCERAM to a dedicated 0.9V power supply. You may connect the VCCPLLDIG_SDM power to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCRT_GXE					Filter	Connect VCCRT_GXE to VCCERAM through an LC filter. For more information about the LC filter design, refer to the *Intel Stratix 10 Power Management User Guide*.
VCCRTPLL_GXE					Filter	You may source VCCRTPLL_GXE from the same regulator as VCCRT_GXE through a ferrite bead.

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						Filtering may be optional if this voltage rail can meet the noise mask requirement. For more information about the noise mask requirements, refer to the *Intel Stratix 10 Power Management User Guide*.
VCCR_GXB[L,R]	3	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCR_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCT_GXB[L,R]	4	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCT_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCH_GXE	5	1.1	± 5% (**)	Switcher (*)	Isolate	Connect the VCCH_GXE to a dedicated 1.1V power supply.
VCCCLK_GXE	6	2.5	± 5% (**)	Switcher (*)	Isolate	Connect VCCCLK_GXE to a dedicated 2.5V power supply.
VCCPT	7	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCBAT		Varies				isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. If you do not intend to utilize the HPS in the Intel Stratix 10 TX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCH_GXB[L,R]		1.8			Filter	
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	8	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

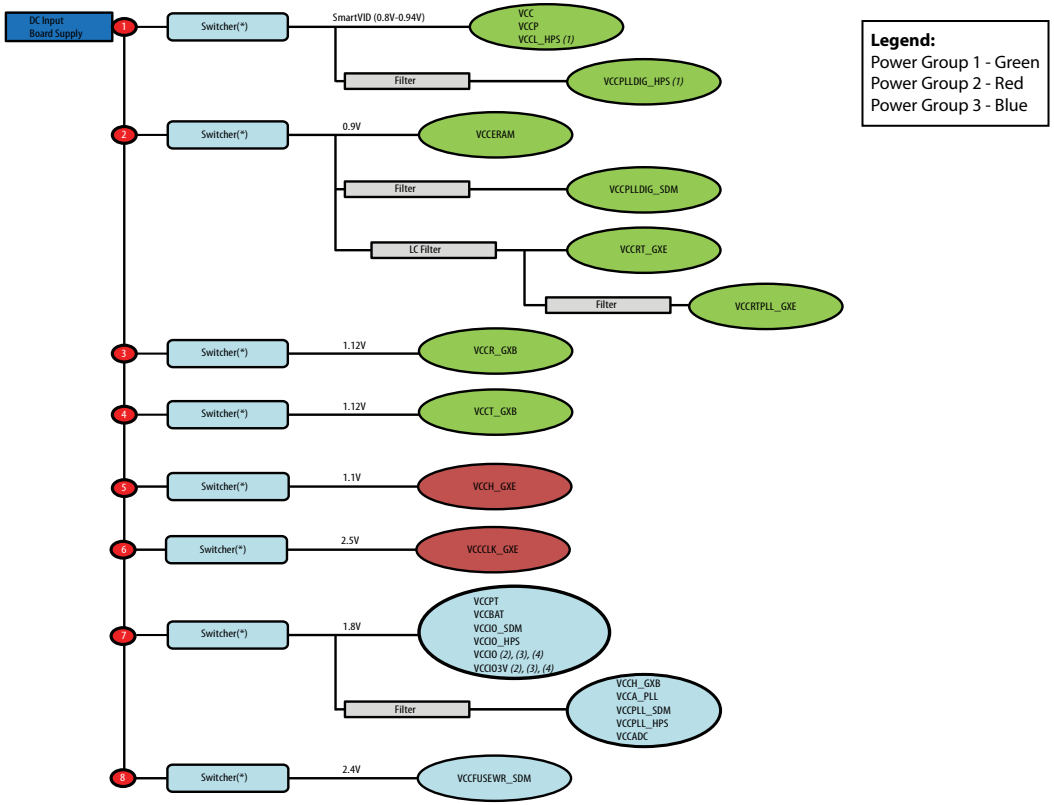
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 7 of the *Notes to Intel Stratix 10 TX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 TX device is provided in Figure 9.

The voltage level for each power rail is preliminary.

Figure 9. Example Power Supply Sharing Guidelines for Intel Stratix 10 TX (–1V, –2V, and –3V parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps—Preliminary



Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator. Optionally, you can connect VCCL_HPS and VCCPLLDIG_HPS to a fixed 0.9V. If you are connecting VCCL_HPS and VCCPLLDIG_HPS to 0.9V, they can share the same power regulator with VCCERAM.
(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.
(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.
(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.
(5) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT pin function.

Example 10—Intel Stratix 10 TX (–2L and –3X parts)

Table 39. Power Supply Sharing Guidelines for Intel Stratix 10 TX (–2L and –3X parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps—Preliminary

Example Requiring 8 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCP	1	0.85	± 30mV	Switcher (*)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCERAM VCCL_HPS	2	0.9	± 30mV	Switcher (*)	Share	Connect the VCCERAM to a dedicated 0.9V power supply. You have the option to connect VCCL_HPS to the same regulator as VCCERAM when the power rails require the same voltage level. You may connect the VCCPLLDIG_SDM and VCCPLLDIG_HPS power rails to the VCCERAM power plane with proper isolation filtering. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Stratix 10 TX device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS and VCCPLLDIG_HPS floating or connect them to GND.
VCCPLLDIG_SDM VCCPLLDIG_HPS					Filter	
VCCRT_GXE					Filter	Connect VCCRT_GXE to VCCERAM through an LC filter. For more information about the LC filter design, refer to the *Intel Stratix 10 Power Management User Guide*.
VCCRTPLL_GXE					Filter	You may source VCCRTPLL_GXE from the same regulator as VCCRT_GXE through a ferrite bead. Filtering may be optional if this voltage rail can meet the noise mask requirement. For more information about

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						the noise mask requirements, refer to the *Intel Stratix 10 Power Management User Guide*.
VCCR_GXB[L,R]	3	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCR_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCT_GXB[L,R]	4	1.12	± 20mV	Switcher (*)	Isolate	Connect the VCCT_GXB to a dedicated 1.12V power supply. The VCCR_GXB and VCCT_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the *Intel Stratix 10 Device Datasheet*.
VCCH_GXE	5	1.1	± 5% (**)	Switcher (*)	Isolate	Connect the VCCH_GXE to a dedicated 1.1V power supply.
VCCCLK_GXE	6	2.5	± 5% (**)	Switcher (*)	Isolate	Connect VCCCLK_GXE to a dedicated 2.5V power supply.
VCCPT	7	1.8	± 5% (**)	Switcher (*)	Share if 1.8V	You may source VCCPT and VCCIO_SDM from the same regulator. You may connect the VCCIO, VCCIO3V, VCCIO_HPS, and VCCBAT to the same power plane if the those power rails are at the same voltage level. You may also connect the VCCH_GXB, VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC to the same power plane with proper isolation filtering. Depending on the
VCCIO_SDM		1.8				
VCCIO		Varies				
VCCIO3V		Varies				
VCCIO_HPS		1.8				
VCCBAT		Varies				

continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCH_GXB[L,R]		1.8			Filter	regulator capabilities, you have the option to share this supply with multiple Intel Stratix 10 devices. If you do not intend to utilize the HPS in the Intel Stratix 10 TX device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS and VCCPLL_HPS floating or connect them to GND. TX device, When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCA_PLL		1.8				
VCCPLL_SDM		1.8				
VCCPLL_HPS		1.8				
VCCADC		1.8				
VCCFUSEWR_SDM	8	2.4	± 50mV	Switcher (*)	Isolate	Connect VCCFUSEWR_SDM to a dedicated 2.4V power supply if the SDM fuses need to be written. Leave VCCFUSEWR_SDM unconnected or tie it to VCCPT 1.8V power if the SDM fuses do not need to be written. Do not tie this pin to GND.

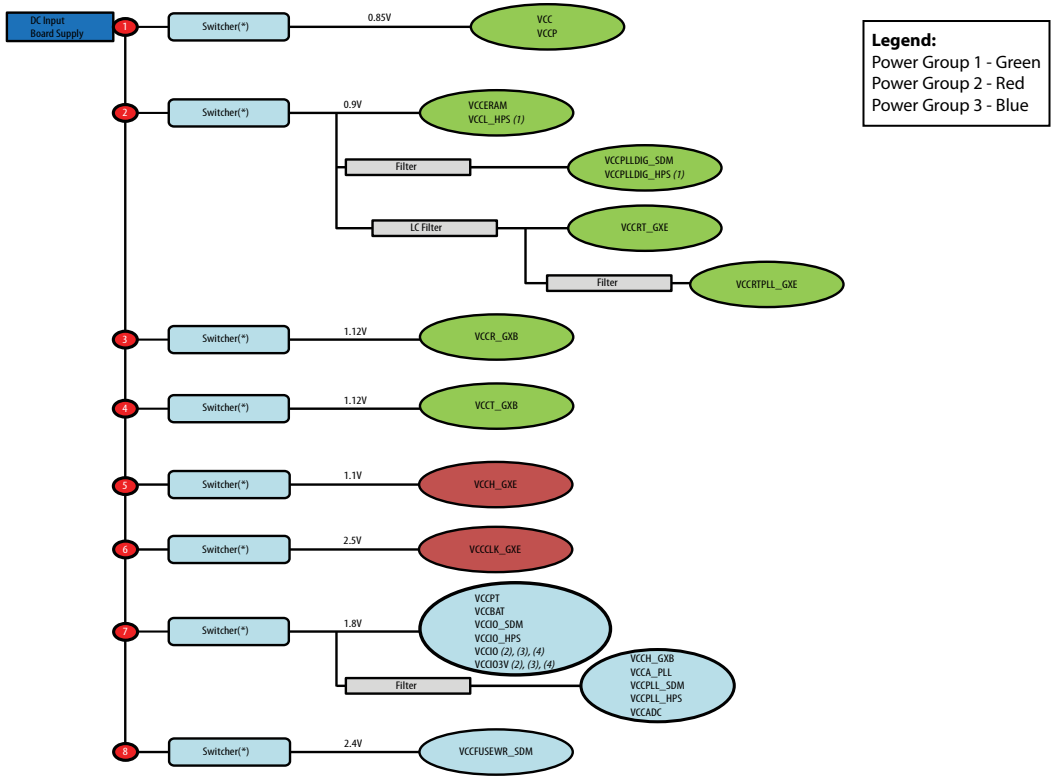
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined as defined in note 7 of the *Notes to Intel Stratix 10 TX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Stratix 10 Device Datasheet*. Use the EPE (Early Power Estimator) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Stratix 10 TX device is provided in Figure 10.

The voltage level for each power rail is preliminary.

Figure 10. Example Power Supply Sharing Guidelines for Intel Stratix 10 TX (–2L and –3X parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps—Preliminary



Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.94V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator.
(2) For all VCCIO and VCCIO3V banks that are 1.8V, all the VCCIO and VCCIO3V banks can share the same 1.8-V regulator with the Group 2 power rails.
(3) For all VCCIO and VCCIO3V banks that are 1.8V and driven from a separate regulator, then they need to be in the Group 3 power rails.
(4) For all VCCIO and VCCIO3V banks other than 1.8V, they need to be in the Group 3 power rails.

Document Revision History for the Intel Stratix 10 Device Family Pin Connection Guidelines

Document Version	Changes
2019.01.31	• Added a note to include the H-tile and E-tile transceivers' reference in the *Intel Stratix 10 MX Pin Connection Guidelines* section. • Removed 0.8V support for VCC and VCCP supplies for the fixed voltage –2L and –3X devices in the following power supply sharing guidelines: — Example 1—Power Supply Sharing Guidelines for Intel Stratix 10 GX with Transceiver Data Rate <= 15 Gbps — Example 2—Power Supply Sharing Guidelines for Intel Stratix 10 GX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Example 4—Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with Transceiver Data Rate <= 15 Gbps — Example 6—Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Example 10—Power Supply Sharing Guidelines for Intel Stratix 10 TX (–2L and –3X parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps • Removed VCCM_WORD and VCCIO_UIB supplies from the following power supply sharing guidelines: — Example 9—Power Supply Sharing Guidelines for Intel Stratix 10 TX (–1V, –2V, and –3V parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps — Example 10—Power Supply Sharing Guidelines for Intel Stratix 10 TX (–2L and –3X parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps
2019.01.03	• Updated the connection guidelines for the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] pins. • Updated the notes of the VCCR_GXB[L,R] and VCCT_GXB[L,R] in the following power supply sharing guidelines: — Example 1—Power Supply Sharing Guidelines for Intel Stratix 10 GX with Transceiver Data Rate <= 15 Gbps — Example 2—Power Supply Sharing Guidelines for Intel Stratix 10 GX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Example 3—Power Supply Sharing Guidelines for Intel Stratix 10 SX (–1V, –2V, and –3V parts) with Transceiver Data Rate <= 15 Gbps — Example 4—Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with Transceiver Data Rate <= 15 Gbps — Example 5—Power Supply Sharing Guidelines for Intel Stratix 10 SX (–1V, –2V, and –3V parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Example 6—Power Supply Sharing Guidelines for Intel Stratix 10 SX (–2L and –3X parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Example 7—Power Supply Sharing Guidelines for Intel Stratix 10 MX (–1V, –2V, and –3V parts) with Transceiver Data Rate <= 15 Gbps — Example 8—Power Supply Sharing Guidelines for Intel Stratix 10 MX (–1V, –2V, and –3V parts) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Example 9—Power Supply Sharing Guidelines for Intel Stratix 10 TX (–1V, –2V, and –3V parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps — Example 10—Power Supply Sharing Guidelines for Intel Stratix 10 TX (–2L and –3X parts) with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps
2018.12.14	• Added Direct to Factory Image pin function to SDM_IO0, SDM_IO10, SDM_IO11, SDM_IO12, SDM_IO13, SDM_IO14, SDM_IO15, and SDM_IO16 pins. • Added SEU_ERROR and CvP_CONFDONE pin functions to SDM_IO0, SDM_IO10, SDM_IO11, SDM_IO12, SDM_IO13, SDM_IO14, SDM_IO15, and SDM_IO16 pins. • Added a description to *Transceiver Pins* section for reference to the OSC_CLK_1 pin. • Updated the pin description and connection guidelines of the OSC_CLK_1 pin. • Updated the connection guidelines of the nCONFIG pin.

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Document Version	Changes
	• Updated the pin function and connection guidelines of the nSTATUS pin. • Updated the pin description and connection guidelines of the IO3V[0,1,2,3,4,5,6,7]_[10,12,20,22] pins. • Updated the pin description and connection guidelines of the VCCFUSEWR_SDM pin. • Updated the connection guidelines of the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N], and VCCH_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N] pins. • Updated the connection guidelines of the REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_CH[B,T]p and REFCLK_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]_CH[B,T]n pins. • Updated the pin description for the INIT_DONE function in SDM_IO0, SDM_IO5, and SDM_IO16 pins. • Updated the connection guidelines of the VCCRT_GXE(L2, L3, R1, R2, R3) and VCCRTPLL_GXE(L2, L3, R1, R2, R3) pins. • Updated the connection guidelines of the HPS_COLD_nRESET function in SDM_IO0, SDM_IO10, SDM_IO11, SDM_IO12, SDM_IO13, SDM_IO14, SDM_IO15, and SDM_IO16 pins. • Updated the connection guidelines of the CLK_ESRAM_[0,1]p and CLK_ESRAM_[0,1]n pins. • Updated the following power supply sharing guidelines: — Example 7—Intel Stratix 10 MX (–1V, –2V, and –3V parts) — Example 8—Intel Stratix 10 MX (–1V, –2V, and –3V parts) — Example 9—Intel Stratix 10 TX (–1V, –2V, and –3V parts) — Example 10—Intel Stratix 10 TX (–2L and –3X parts) • Removed the following power supply sharing guidelines: — Intel Stratix 10 MX (–2L and –3X parts) • Removed support for the Pulse-Width Modulation (PWM) mode. • Removed a note regarding the SEU_ERROR and CvP_CONFDONE pins from the *Notes to Intel Stratix 10 GX Pin Connection Guidelines* section and added the connection guidelines of the SEU_ERROR and CvP_CONFDONE pins in their respective SDM pin functions.
2018.08.16	• Added description that these pins can be used for the HPS in the TCK, TMS, TDO, TDI, JTAG_TCK, JTAG_TMS, JTAG_TDO, and JTAG_TDI pins. • Added note 13 to the *Notes to Intel Stratix 10 GX Pin Connection Guidelines* section. • Added the HPS_COLD_nRESET function to SDM_IO0, SDM_IO10, SDM_IO11, SDM_IO12, SDM_IO13, SDM_IO14, SDM_IO15, and SDM_IO16 pins. • Added a description to *Transceiver Pins* section for reference to the nPERST[L,R][0:2] pins. • Added the PWRMGT_ALERT pin function in the SDM_IO0 and SDM_IO12 pins. • Updated the connection guidelines of the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] pins. • Updated the VCCH_GXB[L,R] pin name to VCCH_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]. • Updated the connection guidelines for the GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_RX_CH[0:5]p, GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]_REFCLK[0:5]p, GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_RX_CH[0:5]n, and GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]_REFCLK[0:5]n pins. • Updated the pin description for the REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]_CH[B,T]p and REFCLK_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]_CH[B,T]n pins.

Document Version	Changes
	• Updated the connection guidelines of the VCCIO3V pin. • Updated the connection guidelines for the –V device for the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_PWM0 pin functions of the SDM_IO pins. • Updated the connection guidelines of the VCCRTPLL_GXE(L2, L3, R1, R2, R3) pins. • Updated the connection guidelines to leave the unused pins floating of the GXE(L8, R9)(A, B, C)_RX_CH[0:23]p and GXE(L8, R9)(A, B, C)_RX_CH[0:23]n pins. • Updated the connection guidelines of the REFCLK_GXE(L8,R9)(A,B,C)_CH[0:8]p and REFCLK_GXE(L8,R9)(A,B,C)_CH[0:8]n pins. • Updated the connection guidelines of the VCCL_HPS pin. • Updated note 12 in the Notes to Intel Stratix 10 GX Pin Connection Guidelines. • Updated the *Power Supply Sharing Guidelines for Intel Stratix 10 Devices* section to include references for the power-up and power-down sequence requirements. • Removed support of the NAND configuration scheme. • Added the following power supply sharing guidelines: — Example 4—Intel Stratix 10 SX (–2L and –3X parts) — Example 6—Intel Stratix 10 SX (–2L and –3X parts) — Example 8—Intel Stratix 10 MX (–2L and –3X parts) — Example 10—Intel Stratix 10 MX (–2L and –3X parts) — Example 12—Intel Stratix 10 TX (–2L and –3X parts) • Updated the following power supply sharing guidelines: — Example 3—Intel Stratix 10 SX (–1V, –2V, and –3V parts) — Example 5—Intel Stratix 10 SX (–1V, –2V, and –3V parts) — Example 7—Intel Stratix 10 MX (–1V, –2V, and –3V parts) — Example 9—Intel Stratix 10 MX (–1V, –2V, and –3V parts) — Example 11—Intel Stratix 10 TX (–1V, –2V, and –3V parts)

Date	Version	Description of Changes
December 2017	2017.12.21	• Added the following Intel Stratix 10 TX pins: — VCCH_GXE(L2, L3, R1, R2, R3) — VCCRT_GXE(L2, L3, R1, R2, R3) — VCCRTPLL_GXE(L2, L3, R1, R2, R3) — VCCCLK_GXE(L2, L3, R1, R2, R3) — GXE(L8, R9)(A, B, C)_RX_CH[0:23]p — GXE(L8, R9)(A, B, C)_RX_CH[0:23]n — GXE(L8, R9)(A, B, C)_TX_CH[0:23]p — GXE(L8, R9)(A, B, C)_TX_CH[0:23]n — REFCLK_GXE(L8,R9)(A,B,C)_CH[0:8]p — REFCLK_GXE(L8,R9)(A,B,C)_CH[0:8]n — IO_AUX_RREF(11, 12, 20, 21, 22) • Added the following HPS sections: — HPS Oscillator Clock Input Pin — HPS JTAG Pins — HPS GPIO Pins — HPS SDMMC Pins — HPS NAND Pins — HPS USB Pins — HPS EMAC Pins — HPS I2C_EMAC and MDIO Pins — HPS I2C Pins — HPS SPI Pins — HPS UART Pins — HPS Trace Pins • Added the Power Supply Sharing Guidelines for Intel Stratix 10 TX with 10 Gbps < Transceiver Data Rate <= 57.8 Gbps.

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Date	Version	Description of Changes
		• Updated the following pin names: — CLK_ESRAM_[0,1]p — CLK_ESRAM_[0,1]n — RREF_ESRAM_[0,1] • Updated the connection guidelines for the following pins: — CLK_ESRAM_[0,1]p — CLK_ESRAM_[0,1]n — UIB_PLL_REF_CLK_[00,01]p — UIB_PLL_REF_CLK_[00,01]n • Updated the connection guidelines for the VREFP_ADC and VREFN_ADC pins. • Updated the connection guidelines for the TEMPDIODEp[0..6] and TEMPDIODEn[0..6] pins. • Updated the connection guidelines for the VCCLSENSE and GNDSENSE pins. • Updated the connection guidelines for the OSC_CLK_1 pin. • Updated the connection guidelines for the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] pins. • Updated the pin names for the VCCM_WORD_(BL,TL) and VCCIO_UIB_(BL,TL) pins. • Updated the pin description for all SDM_IO pins to include the resistor information upon device power up. • Updated the pin description for the INIT_DONE function in SDM_IO0, SDM_IO5, and SDM_IO16. • Updated the pin description of the PWRMGT_SCL function in the SDM_IO0 and SDM_IO14 pins. • Updated the pin description of the PWRMGT_SDA function in the SDM_IO11, SDM_IO12, and SDM_IO16 pins. • Updated note 12 in the Notes to Intel Stratix 10 GX Pin Connection Guidelines. • Added a note for the VCCL_HPS, VCCPLL_HPS, VCCIO_HPS, and VCCPLLDIG_HPS power rails in the following power supply sharing guidelines: — Power Supply Sharing Guidelines for Intel Stratix 10 SX with Transceiver Data Rate <= 15 Gbps — Power Supply Sharing Guidelines for Intel Stratix 10 SX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps
July 2017	2017.07.14	Added the TEMPDIODEp[0..6] and TEMPDIODEn[0..6] pins.
June 2017	2017.06.16	• Added the INIT_DONE function to SDM_IO5 and SDM_IO16 pins. • Added link to the External Memory Interface Pin Information for Intel Stratix 10 Devices. • Updated the connection guidelines of the PLL_[2][A,B,C,F,G,H,I,J,K,L,M,N]_FB[0], PLL_[3][A,B,C,F,G,H,I,J,K,L]_FB[0], PLL_[2][A,B,C,F,G,H,I,J,K,L,M,N]_FBp, PLL_[3][A,B,C,F,G,H,I,J,K,L]_FBp, PLL_[3][A,B,C,F,G,H,I,J,K,L]_FBn, PLL_[2][A,B,C,F,G,H,I,J,K,L,M,N]_CLKOUT[0:1], PLL_[3][A,B,C,F,G,H,I,J,K,L]_CLKOUT[0:1], PLL_[2][A,B,C,F,G,H,I,J,K,L,M,N]_CLKOUT[0:1]p, PLL_[3][A,B,C,F,G,H,I,J,K,L]_CLKOUT[0:1]p, PLL_[2][A,B,C,F,G,H,I,J,K,L,M,N]_CLKOUT[0:1]n, and PLL_[3][A,B,C,F,G,H,I,J,K,L]_CLKOUT[0:1]n pins.

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Date	Version	Description of Changes
		• Updated the pin description and connection guidelines of the OSC_CLK_1 pin. • Updated the I/O standards supported in the pin description of the IO3V[0,1,2,3,4,5,6,7]_[10,12,20,22] pins. • Updated the pin functions and connection guidelines of the RZQ_[2] [A,B,C,F,G,H,I,J,K,L,M ,N] and RZQ_[3] [A,B,C,D,E,F,G,H,I,J,K ,L] pins. • Updated the connection guidelines of the VCCIO([2][A,B,C,F,L,M,N],[3][A,B,C,I,J,K,L]) pins. • Updated the pin description of the VCCERAM. • Updated the connection guidelines of the VCCFUSEWR_SDM pin. • Updated the connection guidelines of the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] pins. • Updated the pin description for the CONF_DONE function in the SDM_IO5 pin. • Added the INIT_DONE function to SDM_IO5 and SDM_IO16 pins. • Updated note 12 in the *Notes to Stratix 10 GX and MX Pin Connecti0n Guidelines*. • Updated the V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ supply to 0.94V. • Updated the connection guidelines for the VCCL_HPS pin. • Updated the notes for V_{CC} and V_{CCP} power rails in the following tables: — Power Supply Sharing Guidelines for Stratix 10 GX with Transceiver Data Rate <= 15 Gbps — Power Supply Sharing Guidelines for Stratix 10 GX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps • Updated the notes for V_{CC}, V_{CCP}, V_{CCL_HPS}, and $V_{CCPLLDIG\_HPS}$ power rails in the following examples: — Power Supply Sharing Guidelines for Stratix 10 SX with Transceiver Data Rate <= 15 Gbps — Power Supply Sharing Guidelines for Stratix 10 SX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Power Supply Sharing Guidelines for Stratix 10 MX with Transceiver Data Rate <= 15 Gbps — Power Supply Sharing Guidelines for Stratix 10 MX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps

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Date	Version	Description of Changes
		• Updated voltage of the V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ supply in note 1 of the following figures: — Example Power Supply Sharing Guidelines for Stratix 10 SX with Transceiver Data Rate <= 15 Gbps — Example Power Supply Sharing Guidelines for Stratix 10 SX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps — Example Power Supply Sharing Guidelines for Stratix 10 MX with Transceiver Data Rate <= 15 Gbps — Example Power Supply Sharing Guidelines for Stratix 10 MX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps • Updated the VCCM's tolerance to ± 100mV. • Removed PowerPlay text from tool name.
February 2017	2017.02.24	• Added the following pins for the MX device variant: — VCCM[B,T] — VCCIO_UIB_[B,T] — ESRAM_PLL_REF_CLK_[0,1]p — ESRAM_PLL_REF_CLK_[0,1]n — UIB_PLL_REF_CLK_[00,01,10,11]p — UIB_PLL_REF_CLK_[00,01,10,11]n — ESRAM_RREF_[B,T] — UIB_RREF_[00,01,10,11] • Added the following power supply sharing guidelines for the MX device variant: — Example 5. Power Supply Sharing Guidelines for Stratix 10 MX with Transceiver Data Rate <= 15 Gbps — Example 6. Power Supply Sharing Guidelines for Stratix 10 MX with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps • Updated IO3V[0,1,2,3,4,5,6,7]_[10,12,20,22] pin name. • Updated the connection guidelines for the SDM_IO13 pin. • Updated the pin description of the CONF_DONE function in SDM_IO5 and SDM_IO16 pins. • Updated note 7 in the Notes to Stratix 10 GX and MX Pin Connecti0n Guidelines. • Updated note 6 in the Notes to Stratix 10 SX Pin Connection Guidelines. • Updated the transceiver data rate from 30 Gbps to 28.3 Gbps.
October 2016	2016.10.31	Initial release.