

Dedicated Pin	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	49-Pin Ultra FineLine BGA
INPUT/GCLK1	43	37	41	A5
INPUT/GCLRn	1	39	43	A3
INPUT/OE1	44	38	42	A4
INPUT/OE2/GCLK2	2	40	44	B4
TDI (1)	7	1	2	B1
TMS (1)	13	7	8	F1
TCK (1)	32	26	29	F7
TDO (1)	38	32	35	B7
VREFA (2)	11	5	6	D1
VREFB (2)	31	25	28	E7
GNDINT	22, 42	16, 36	18, 40	B5, F4
GNDIO	10, 30	4, 24	5, 27	C2, E6
VCCINT (2.5 V)	3, 23	17, 41	19, 45	B3, E4
VCCIO1 (1.8 V, 2.5 V, or 3.3 V)	15	9	10	E2
VCCIO2 (1.8 V, 2.5 V, or 3.3 V)	35	29	32	C6
No Connect (N.C.)	–	–	1, 13, 24, 37	D2, D3, D4, D5, D6
Total User I/O Pins (3)	36	36	36	36

LAB	MC	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	49-Pin Ultra FineLine BGA	IOGND Groups (200mA)	IOVCC Groups (100 mA)	I/O Bank
A	1	4	42	46	C3	A	A	1
A	2	5	43	47	A2	A	A	1
A	3	6	44	48	A1	A	A	1
A	4	7 (1)	1 (1)	2 (1)	B1 (1)	A	A	1
A	5	8	2	3	B2	A	A	1
A	6	9	3	4	C1	A	A	1
A	7	11 (2)	5 (2)	6 (2)	D1 (2)	B	A	1
A	8	12	6	7	E1	B	A	1
A	9	13 (1)	7 (1)	8 (1)	F1 (1)	B	A	1
A	10	14	8	9	F2	B	A	1
A	11	16	10	11	G1	B	B	1
A	12	17	11	12	G2	B	B	1
A	13	18	12	14	F3	B	B	1
A	14	19	13	15	G3	B	B	1
A	15	20	14	16	E3	B	B	1
A	16	21	15	17	G4	B	B	1
B	17	41	35	39	C4	A	D	2
B	18	40	34	38	C5	A	D	2
B	19	39	33	36	A6	A	D	2
B	20	38 (1)	32 (1)	35 (1)	B7 (1)	A	D	2
B	21	37	31	34	A7	A	D	2
B	22	36	30	33	B6	A	D	2
B	23	34	28	31	C7	A	C	2
B	24	33	27	30	D7	A	C	2
B	25	32 (1)	26 (1)	29 (1)	F7 (1)	A	C	2
B	26	31 (2)	25 (2)	28 (2)	E7 (2)	A	C	2
B	27	29	23	26	F6	B	C	2
B	28	28	22	25	G7	B	C	2
B	29	27	21	23	G6	B	C	2
B	30	26	20	22	F5	B	C	2
B	31	25	19	21	G5	B	C	2
B	32	24	18	20	E5	B	C	2

Notes:

- (1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.
- (2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, this pin is not available as a user I/O pin.
- (3) The user I/O pin count includes dedicated input pins and all I/O pins.

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