Pin Information for the MAX® V 5M40Z Device
Version 1.1
Note (1)

Bank Number	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	M64
1	IO			DIFFIO_L1p	A1
1	IO			DIFFIO_L1n	B1
1	IO				C2
1	IO				D2
1	IO	CLK1			E2
1	IO				F1
1	IO				F3
1	TMS		TMS		G1
1	TDI		TDI		H1
1	TCK		TCK		H2
1	TDO		TDO		G3
1	IO			DIFFIO_B1p	H3
1	IO			DIFFIO_B1n	H4
1	IO			DIFFIO_B2p	H5
1	IO			DIFFIO_B2n	H6
1	IO				F5
1	IO		DEV_OE	DIFFIO_B3p	F6
1	IO		DEV_CLRn	DIFFIO_B3n	H7
1	IO				G7
1	IO			DIFFIO_B4p	G8
1	IO			DIFFIO_B4n	H8
2	IO				F8
2	IO	CLK2			D8
2	IO			DIFFIO_R2n	B7
2	IO			DIFFIO_R2p	C8
2	IO			DIFFIO_R1n	B8
2	IO			DIFFIO_R1p	A8
2	IO				C6
2	IO			DIFFIO_T3n	A6
2	IO			DIFFIO_T3p	C5
2	IO			DIFFIO_T2n	A4
2	IO			DIFFIO_T2p	A3
2	IO			DIFFIO_T1n	A2
2	IO			DIFFIO_T1p	B2
	GND				C1
	GND				D1
	GND				E1
	GND				F2
	GND				G2
	GND				G4
	GND				F4
	GND				G5
	GND				G6
	GND				F7
	GND				E7
	GND				E8
	GND				C7
	GND				A7
	GND				B6
	GND				B5
	GND				A5
	GND				B4

Bank Number	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	M64
	GND				C3
	GND				B3
	GND				D4
	GND				D7
	GND				E4
	GND				E5
	GND				E6
	VCCIO1				D3
	VCCIO1				E3
	VCCIO2				C4
	VCCIO2				D5
	VCCINT				D6

Note:
(1) For more information about pin definitions and pin connection guidelines, refer to the MAX V Device Family Pin Connection Guidelines.

Bank Number	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	E64 *(2)*
1	IO			DIFFIO_L1p	64
1	IO			DIFFIO_L1n	1
1	IO				2
1	IO			DIFFIO_L2p	3
1	IO			DIFFIO_L2n	4
1	IO				5
1	IO	CLK0			7
1	IO	CLK1			9
1	IO				10
1	IO			DIFFIO_L3p	11
1	IO			DIFFIO_L3n	12
1	IO				13
1	TMS		TMS		14
1	TDI		TDI		15
1	TCK		TCK		16
1	TDO		TDO		17
1	IO			DIFFIO_B1p	18
1	IO			DIFFIO_B1n	19
1	IO			DIFFIO_B2p	20
1	IO			DIFFIO_B2n	21
1	IO			DIFFIO_B3p	22
1	IO			DIFFIO_B3n	24
1	IO				25
1	IO			DIFFIO_B4p	26
1	IO			DIFFIO_B4n	27
1	IO		DEV_OE	DIFFIO_B5p	28
1	IO		DEV_CLRn	DIFFIO_B5n	29
1	IO			DIFFIO_B6p	30
1	IO			DIFFIO_B6n	31
1	IO			DIFFIO_B7p	32
1	IO			DIFFIO_B7n	33
2	IO			DIFFIO_R4n	34
2	IO			DIFFIO_R4p	35
2	IO			DIFFIO_R3n	36
2	IO			DIFFIO_R3p	37
2	IO				38
2	IO	CLK2			40
2	IO	CLK3			42
2	IO			DIFFIO_R2n	43
2	IO			DIFFIO_R2p	44
2	IO				45
2	IO			DIFFIO_R1n	46
2	IO			DIFFIO_R1p	47
2	IO				48
2	IO			DIFFIO_T6n	49
2	IO			DIFFIO_T6p	50
2	IO				51
2	IO			DIFFIO_T5n	52
2	IO			DIFFIO_T5p	53
2	IO			DIFFIO_T4n	54
2	IO			DIFFIO_T4p	55
2	IO			DIFFIO_T3n	56

Bank Number	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	E64 *(2)*
2	IO			DIFFIO_T3p	58
2	IO			DIFFIO_T2n	59
2	IO			DIFFIO_T2p	60
2	IO			DIFFIO_T1n	61
2	IO				62
2	IO			DIFFIO_T1p	63
	VCCIO1				6
	VCCIO1				23
	VCCIO2				39
	VCCIO2				57
	VCCINT				8
	VCCINT				41

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
MAX V Device Family Pin Connection Guidelines.
(2) The E64 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB.
This exposed pad is used for electrical connectivity and not for thermal purposes.

Version Number	Date	Changes Made
1.0	12/3/2010	Initial release.
1.1	3/19/2013	Updated pin H7 of pin list M64 from DIFFIO_B5n to DIFFIO_B3n.