Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	V81
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	C2
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	C1
1B	VREFB1N0	IO		JTAGEN				D2
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	D3
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	D4
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	E1
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	E2
1B	VREFB1N0	IO						E3
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	F1
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	F2
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	G2
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	G1
2	VREFB2N0	IO			DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed	F3
2	VREFB2N0	IO			DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	G3
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	H3
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	J2
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	G4
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	G5
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	J3
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	H4
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	J4
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	J5
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	H6
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	J6
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	G6
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	H7
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	J7
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	J8
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	G7
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	F7
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	G8
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	G9
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	F8
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	F9
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	E8
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	E7
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	D8
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	D9
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	C8
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	C9
6	VREFB6N0	IO	PLL_R_CLKOUTp		DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	C7
6	VREFB6N0	IO	PLL_R_CLKOUTn		DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	B7
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	A7
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B6
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	A6
8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	A5
8	VREFB8N0	IO		CONFIG_SEL				C6
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	A4
8	VREFB8N0	Input_only		nCONFIG				D6
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	B5
8	VREFB8N0	IO		CRC_ERROR				C5
8	VREFB8N0	IO						A3
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	B3
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	C4
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	C3
		GND						H9
		GND						H5
		GND						H1
		GND						F6
		GND						F4
		GND						E9
		GND						E5
		GND						D7
		GND						D1
		GND						B4
		GND						A9
		GND						A1
		VCC						H8
		VCC						H2
		VCC						B9
		VCC						B2
		VCCD_PLL2						A8
		VCCIO1_2						E4
		VCCIO3						F5
		VCCIO5_6						E6
		VCCIO8						D5
		VCCA1						J1
		VCCA2						B8
		VCCA3						B1
		VCCA4						J9

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the
MAX 10 FPGA Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F256
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	F5
1A	VREFB1N0	IO			DIFFIO_RX_L2n	DIFFOUT_L2n	Low_Speed	C4
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	F4
1A	VREFB1N0	IO			DIFFIO_RX_L2p	DIFFOUT_L2p	Low_Speed	C3
1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	H5
1A	VREFB1N0	IO			DIFFIO_RX_L4n	DIFFOUT_L4n	Low_Speed	E3
1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	G5
1A	VREFB1N0	IO			DIFFIO_RX_L4p	DIFFOUT_L4p	Low_Speed	F2
1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	G2
1A	VREFB1N0	IO			DIFFIO_RX_L6n	DIFFOUT_L6n	Low_Speed	C2
1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	F1
1A	VREFB1N0	IO			DIFFIO_RX_L6p	DIFFOUT_L6p	Low_Speed	B2
1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	E1
1A	VREFB1N0	IO			DIFFIO_RX_L8n	DIFFOUT_L8n	Low_Speed	B1
1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	D1
1A	VREFB1N0	IO			DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	C1
1B	VREFB1N0	IO		JTAGEN				G6
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	H2
1B	VREFB1N0	IO	VREFB1N0					J1
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	H3
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	G1
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	H1
1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed	J5
1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	H6
1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	J3
1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	J2
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	M3
2	VREFB2N0	IO			DIFFIO_RX_L19n	DIFFOUT_L19n	High_Speed	L1
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	L3
2	VREFB2N0	IO			DIFFIO_RX_L19p	DIFFOUT_L19p	High_Speed	K2
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	J6
2	VREFB2N0	IO			DIFFIO_RX_L21n	DIFFOUT_L21n	High_Speed	M2
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	K6
2	VREFB2N0	IO			DIFFIO_RX_L21p	DIFFOUT_L21p	High_Speed	L2
2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed	N2
2	VREFB2N0	IO	VREFB2N0					M1
2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	P1
2	VREFB2N0	IO						N1
2	VREFB2N0	IO			DIFFIO_RX_L25n	DIFFOUT_L25n	High_Speed	K5
2	VREFB2N0	IO			DIFFIO_RX_L25p	DIFFOUT_L25p	High_Speed	L6
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed	N3
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	N4
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	P4
3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed	P2
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	N5
3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed	R1
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	M6
3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed	R3
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	L7
3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed	R2
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	R4
3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	T3
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	P5
3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed	T2
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	R6
3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed	T5
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	R5
3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed	T4
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	M7
3	VREFB3N0	IO	VREFB3N0					T7
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	L8
3	VREFB3N0	IO						T6
3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed	R7
3	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	High_Speed	T8
3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	P6
3	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	High_Speed	R8
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	P9
3	VREFB3N0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	High_Speed	T9
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	P8
3	VREFB3N0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	High_Speed	R9
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	M8
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	M9
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	T11
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	R10
4	VREFB4N0	IO			DIFFIO_TX_RX_B18n	DIFFOUT_B18n	High_Speed	P10
4	VREFB4N0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	High_Speed	R11
4	VREFB4N0	IO			DIFFIO_TX_RX_B18p	DIFFOUT_B18p	High_Speed	P11
4	VREFB4N0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	High_Speed	R12
4	VREFB4N0	IO			DIFFIO_TX_RX_B20n	DIFFOUT_B20n	High_Speed	M10
4	VREFB4N0	IO	VREFB4N0					T13
4	VREFB4N0	IO			DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed	L9
4	VREFB4N0	IO						T12
4	VREFB4N0	IO			DIFFIO_TX_RX_B21n	DIFFOUT_B21n	High_Speed	P13
4	VREFB4N0	IO			DIFFIO_TX_RX_B21p	DIFFOUT_B21p	High_Speed	P12
4	VREFB4N0	IO			DIFFIO_TX_RX_B27n	DIFFOUT_B27n	High_Speed	M11
4	VREFB4N0	IO			DIFFIO_TX_RX_B27p	DIFFOUT_B27p	High_Speed	L10
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	P14
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	T14
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	R14
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	T15
5	VREFB5N0	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	High_Speed	L11

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F256
5	VREFB5N0	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	High_Speed	L12
5	VREFB5N0	IO			DIFFIO_RX_R5p	DIFFOUT_R5p	High_Speed	N14
5	VREFB5N0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	High_Speed	M15
5	VREFB5N0	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	High_Speed	P15
5	VREFB5N0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	High_Speed	M14
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	N16
5	VREFB5N0	IO						R15
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	P16
5	VREFB5N0	IO	VREFB5N0					R16
5	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	High_Speed	K11
5	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	High_Speed	K12
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	K14
5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	M16
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	L15
5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	L16
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	J11
6	VREFB6N0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	High_Speed	J14
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	J12
6	VREFB6N0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	High_Speed	K15
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	J15
6	VREFB6N0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	High_Speed	H15
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	J16
6	VREFB6N0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	High_Speed	H16
6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	D16
6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed	C16
6	VREFB6N0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed	H11
6	VREFB6N0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	High_Speed	H12
6	VREFB6N0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed	G14
6	VREFB6N0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	High_Speed	G16
6	VREFB6N0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	High_Speed	G15
6	VREFB6N0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	High_Speed	F16
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed	G11
6	VREFB6N0	IO	VREFB6N0					B15
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	G12
6	VREFB6N0	IO						B16
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	F14
6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed	E15
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	E14
6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed	E16
6	VREFB6N0	IO	PLL_R_CLKOUTp		DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	D14
6	VREFB6N0	IO			DIFFIO_RX_R34p	DIFFOUT_R34p	High_Speed	D15
6	VREFB6N0	IO	PLL_R_CLKOUTn		DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	C14
6	VREFB6N0	IO			DIFFIO_RX_R34n	DIFFOUT_R34n	High_Speed	C15
7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed	D12
7	VREFB7N0	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	High_Speed	C13
7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed	E11
7	VREFB7N0	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	High_Speed	C12
7	VREFB7N0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	High_Speed	F11
7	VREFB7N0	IO						A14
7	VREFB7N0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	High_Speed	F12
7	VREFB7N0	IO	VREFB7N0					A15
7	VREFB7N0	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	High_Speed	F10
7	VREFB7N0	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	High_Speed	E10
7	VREFB7N0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed	B13
7	VREFB7N0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	High_Speed	A13
8	VREFB8N0	IO			DIFFIO_RX_T12p	DIFFOUT_T12p	Low_Speed	D9
8	VREFB8N0	IO			DIFFIO_RX_T12n	DIFFOUT_T12n	Low_Speed	C9
8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed	F9
8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low_Speed	B12
8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed	E9
8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed	B11
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	C10
8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed	A11
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B10
8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed	A12
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	B8
8	VREFB8N0	IO						A10
8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	B7
8	VREFB8N0	IO	VREFB8N0					A9
8	VREFB8N0	IO		CONFIG_SEL				F8
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	B9
8	VREFB8N0	Input_only		nCONFIG				E8
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	A8
8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	B6
8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low_Speed	A7
8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	C6
8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	A6
8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed	B5
8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed	B4
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed	C5
8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low_Speed	A5
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	F7
8	VREFB8N0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	Low_Speed	A3
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	E7
8	VREFB8N0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	Low_Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	B3
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	A4
		GND						D2
		GND						E2
		GND						T16
		GND						T10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F256
		GND						T1
		GND						R13
		GND						P7
		GND						P3
		GND						N9
		GND						N15
		GND						N12
		GND						M4
		GND						L14
		GND						K9
		GND						K7
		GND						K3
		GND						K16
		GND						K1
		GND						J10
		GND						H7
		GND						H14
		GND						G8
		GND						G3
		GND						G10
		GND						F15
		GND						E6
		GND						E13
		GND						D6
		GND						D3
		GND						C8
		GND						C11
		GND						B14
		GND						A16
		GND						A1
		VCC						K8
		VCC						K10
		VCC						J9
		VCC						J8
		VCC						J7
		VCC						H9
		VCC						H8
		VCC						H10
		VCC						G9
		VCC						G7
		VCC						F6
		VCCD_PLL1						M5
		VCCD_PLL2						D13
		VCCIO1A						H4
		VCCIO1A						G4
		VCCIO1B						J4
		VCCIO2						L4
		VCCIO2						K4
		VCCIO3						N8
		VCCIO3						N7
		VCCIO3						N6
		VCCIO4						N11
		VCCIO4						N10
		VCCIO5						M13
		VCCIO5						L13
		VCCIO5						K13
		VCCIO6						J13
		VCCIO6						H13
		VCCIO6						G13
		VCCIO6						F13
		VCCIO7						D11
		VCCIO7						D10
		VCCIO8						D8
		VCCIO8						D7
		VCCIO8						C7
		NC						N13
		NC						F3
		NC						D4
		VCCA1						L5
		VCCA2						E12
		VCCA3						E4
		VCCA3						D5
		VCCA3						E5
		VCCA4						M12

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	D4
1A	VREFB1N0	IO			DIFFIO_RX_L2n	DIFFOUT_L2n	Low_Speed	C2
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	E4
1A	VREFB1N0	IO			DIFFIO_RX_L2p	DIFFOUT_L2p	Low_Speed	D2
1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	G6
1A	VREFB1N0	IO			DIFFIO_RX_L4n	DIFFOUT_L4n	Low_Speed	B1
1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	H6
1A	VREFB1N0	IO			DIFFIO_RX_L4p	DIFFOUT_L4p	Low_Speed	C1
1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	F5
1A	VREFB1N0	IO			DIFFIO_RX_L6n	DIFFOUT_L6n	Low_Speed	D1
1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	E5
1A	VREFB1N0	IO			DIFFIO_RX_L6p	DIFFOUT_L6p	Low_Speed	E1
1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	G3
1A	VREFB1N0	IO			DIFFIO_RX_L8n	DIFFOUT_L8n	Low_Speed	F1
1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	F2
1A	VREFB1N0	IO			DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	G1
1B	VREFB1N0	IO			DIFFIO_RX_L9n	DIFFOUT_L9n	Low_Speed	G7
1B	VREFB1N0	IO			DIFFIO_RX_L10n	DIFFOUT_L10n	Low_Speed	H2
1B	VREFB1N0	IO		JTAGEN	DIFFIO_RX_L9p	DIFFOUT_L9p	Low_Speed	H7
1B	VREFB1N0	IO			DIFFIO_RX_L10p	DIFFOUT_L10p	Low_Speed	H1
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	J7
1B	VREFB1N0	IO	VREFB1N0					J3
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	J8
1B	VREFB1N0	IO						J4
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	H3
1B	VREFB1N0	IO			DIFFIO_RX_L13n	DIFFOUT_L13n	Low_Speed	J2
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	H4
1B	VREFB1N0	IO			DIFFIO_RX_L13p	DIFFOUT_L13p	Low_Speed	J1
1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed	J6
1B	VREFB1N0	IO			DIFFIO_RX_L15n	DIFFOUT_L15n	Low_Speed	K2
1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	K7
1B	VREFB1N0	IO			DIFFIO_RX_L15p	DIFFOUT_L15p	Low_Speed	K1
1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	K4
1B	VREFB1N0	IO			DIFFIO_RX_L17n	DIFFOUT_L17n	Low_Speed	L1
1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	K3
1B	VREFB1N0	IO			DIFFIO_RX_L17p	DIFFOUT_L17p	Low_Speed	L2
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	L3
2	VREFB2N0	IO			DIFFIO_RX_L19n	DIFFOUT_L19n	High_Speed	M1
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	M3
2	VREFB2N0	IO			DIFFIO_RX_L19p	DIFFOUT_L19p	High_Speed	M2
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	K8
2	VREFB2N0	IO			DIFFIO_RX_L21n	DIFFOUT_L21n	High_Speed	N1
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	L8
2	VREFB2N0	IO			DIFFIO_RX_L21p	DIFFOUT_L21p	High_Speed	P1
2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed	M4
2	VREFB2N0	IO	VREFB2N0					R1
2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	N3
2	VREFB2N0	IO						R2
2	VREFB2N0	IO			DIFFIO_RX_L23n	DIFFOUT_L23n	High_Speed	R3
2	VREFB2N0	IO			DIFFIO_RX_L24n	DIFFOUT_L24n	High_Speed	P2
2	VREFB2N0	IO			DIFFIO_RX_L23p	DIFFOUT_L23p	High_Speed	T3
2	VREFB2N0	IO			DIFFIO_RX_L24p	DIFFOUT_L24p	High_Speed	P3
2	VREFB2N0	IO			DIFFIO_RX_L25n	DIFFOUT_L25n	High_Speed	L7
2	VREFB2N0	IO			DIFFIO_RX_L26n	DIFFOUT_L26n	High_Speed	T1
2	VREFB2N0	IO			DIFFIO_RX_L25p	DIFFOUT_L25p	High_Speed	M7
2	VREFB2N0	IO			DIFFIO_RX_L26p	DIFFOUT_L26p	High_Speed	T2
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed	N4
2	VREFB2N0	IO			DIFFIO_RX_L28n	DIFFOUT_L28n	High_Speed	U1
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	P4
2	VREFB2N0	IO			DIFFIO_RX_L28p	DIFFOUT_L28p	High_Speed	U2
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	R4
3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed	U3
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	T4
3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed	V2
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	P6
3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed	V3
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	P5
3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed	V4
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	R5
3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	U5
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	R6
3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed	V5
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	T5
3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed	T7
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	T6
3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed	T8
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	N7
3	VREFB3N0	IO	VREFB3N0					U6
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	N8
3	VREFB3N0	IO						V6
3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed	R8
3	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	High_Speed	U7
3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	R9
3	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	High_Speed	V7
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	V9
3	VREFB3N0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	High_Speed	U8
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	U9
3	VREFB3N0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	High_Speed	V8
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	M8
3	VREFB3N0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	High_Speed	V10
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	M9

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
3	VREFB3N0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	High_Speed	V11
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	T9
3	VREFB3N0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	High_Speed	V12
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	T10
3	VREFB3N0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	High_Speed	U11
4	VREFB4N0	IO			DIFFIO_TX_RX_B18n	DIFFOUT_B18n	High_Speed	P10
4	VREFB4N0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	High_Speed	U12
4	VREFB4N0	IO			DIFFIO_TX_RX_B18p	DIFFOUT_B18p	High_Speed	N11
4	VREFB4N0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	High_Speed	U13
4	VREFB4N0	IO			DIFFIO_TX_RX_B20n	DIFFOUT_B20n	High_Speed	M10
4	VREFB4N0	IO	VREFB4N0					T11
4	VREFB4N0	IO			DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed	L10
4	VREFB4N0	IO						T12
4	VREFB4N0	IO			DIFFIO_TX_RX_B21n	DIFFOUT_B21n	High_Speed	R10
4	VREFB4N0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	High_Speed	V13
4	VREFB4N0	IO			DIFFIO_TX_RX_B21p	DIFFOUT_B21p	High_Speed	R11
4	VREFB4N0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	High_Speed	V14
4	VREFB4N0	IO			DIFFIO_TX_RX_B23n	DIFFOUT_B23n	High_Speed	R12
4	VREFB4N0	IO			DIFFIO_RX_B24n	DIFFOUT_B24n	High_Speed	T13
4	VREFB4N0	IO			DIFFIO_TX_RX_B23p	DIFFOUT_B23p	High_Speed	R13
4	VREFB4N0	IO			DIFFIO_RX_B24p	DIFFOUT_B24p	High_Speed	T14
4	VREFB4N0	IO			DIFFIO_TX_RX_B25n	DIFFOUT_B25n	High_Speed	R14
4	VREFB4N0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	High_Speed	V15
4	VREFB4N0	IO			DIFFIO_TX_RX_B25p	DIFFOUT_B25p	High_Speed	T15
4	VREFB4N0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	High_Speed	U15
4	VREFB4N0	IO			DIFFIO_TX_RX_B27n	DIFFOUT_B27n	High_Speed	U16
4	VREFB4N0	IO			DIFFIO_RX_B28n	DIFFOUT_B28n	High_Speed	V16
4	VREFB4N0	IO			DIFFIO_TX_RX_B27p	DIFFOUT_B27p	High_Speed	U17
4	VREFB4N0	IO			DIFFIO_RX_B28p	DIFFOUT_B28p	High_Speed	V17
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	N14
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	T16
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	P14
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	R16
5	VREFB5N0	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	High_Speed	M12
5	VREFB5N0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	High_Speed	U18
5	VREFB5N0	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	High_Speed	M11
5	VREFB5N0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	High_Speed	T18
5	VREFB5N0	IO			DIFFIO_RX_R5p	DIFFOUT_R5p	High_Speed	N15
5	VREFB5N0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	High_Speed	N16
5	VREFB5N0	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	High_Speed	M15
5	VREFB5N0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	High_Speed	M16
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	R15
5	VREFB5N0	IO						P16
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	P15
5	VREFB5N0	IO	VREFB5N0					P17
5	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	High_Speed	L12
5	VREFB5N0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	High_Speed	T17
5	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	High_Speed	L11
5	VREFB5N0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	High_Speed	R17
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	L15
5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	L16
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	K15
5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	K16
5	VREFB5N0	IO			DIFFIO_RX_R12p	DIFFOUT_R12p	High_Speed	R18
5	VREFB5N0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	High_Speed	N18
5	VREFB5N0	IO			DIFFIO_RX_R12n	DIFFOUT_R12n	High_Speed	P18
5	VREFB5N0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	High_Speed	M18
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	K12
6	VREFB6N0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	High_Speed	M17
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	K11
6	VREFB6N0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	High_Speed	L18
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	L17
6	VREFB6N0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	High_Speed	K18
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	K17
6	VREFB6N0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	High_Speed	J18
6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	H18
6	VREFB6N0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	High_Speed	H17
6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed	G18
6	VREFB6N0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	High_Speed	G17
6	VREFB6N0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed	J11
6	VREFB6N0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	High_Speed	J12
6	VREFB6N0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed	J15
6	VREFB6N0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	High_Speed	J16
6	VREFB6N0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	High_Speed	H15
6	VREFB6N0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	High_Speed	H16
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed	H11
6	VREFB6N0	IO	VREFB6N0					F18
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	H12
6	VREFB6N0	IO						E18
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	F15
6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed	G16
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	G15
6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed	F16
6	VREFB6N0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	High_Speed	E16
6	VREFB6N0	IO			DIFFIO_RX_R30p	DIFFOUT_R30p	High_Speed	D18
6	VREFB6N0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	High_Speed	D16
6	VREFB6N0	IO			DIFFIO_RX_R30n	DIFFOUT_R30n	High_Speed	E17
6	VREFB6N0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	High_Speed	G11
6	VREFB6N0	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	C18
6	VREFB6N0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	High_Speed	G12
6	VREFB6N0	IO			DIFFIO_RX_R32n	DIFFOUT_R32n	High_Speed	B18

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
6	VREFB6N0	IO	PLL_R_CLKOUTp		DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	E15
6	VREFB6N0	IO			DIFFIO_RX_R34p	DIFFOUT_R34p	High_Speed	D17
6	VREFB6N0	IO	PLL_R_CLKOUTn		DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	D15
6	VREFB6N0	IO			DIFFIO_RX_R34n	DIFFOUT_R34n	High_Speed	C17
7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed	E14
7	VREFB7N0	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	High_Speed	B17
7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed	D14
7	VREFB7N0	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	High_Speed	B16
7	VREFB7N0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	High_Speed	D12
7	VREFB7N0	IO						A17
7	VREFB7N0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	High_Speed	D13
7	VREFB7N0	IO	VREFB7N0					A16
7	VREFB7N0	IO			DIFFIO_RX_T4p	DIFFOUT_T4p	High_Speed	C16
7	VREFB7N0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	High_Speed	A15
7	VREFB7N0	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	High_Speed	C15
7	VREFB7N0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	High_Speed	A14
7	VREFB7N0	IO			DIFFIO_RX_T6p	DIFFOUT_T6p	High_Speed	C14
7	VREFB7N0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	High_Speed	B14
7	VREFB7N0	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	High_Speed	C13
7	VREFB7N0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	High_Speed	B13
7	VREFB7N0	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	High_Speed	F11
7	VREFB7N0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	High_Speed	C12
7	VREFB7N0	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	High_Speed	F12
7	VREFB7N0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	High_Speed	B12
7	VREFB7N0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed	C11
7	VREFB7N0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	High_Speed	A13
7	VREFB7N0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	High_Speed	B11
7	VREFB7N0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	High_Speed	A12
8	VREFB8N0	IO			DIFFIO_RX_T12p	DIFFOUT_T12p	Low_Speed	D10
8	VREFB8N0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	Low_Speed	A11
8	VREFB8N0	IO			DIFFIO_RX_T12n	DIFFOUT_T12n	Low_Speed	D9
8	VREFB8N0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	Low_Speed	A10
8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed	F10
8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low_Speed	A9
8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed	G10
8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed	A8
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	B9
8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed	C10
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B8
8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed	C9
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	D8
8	VREFB8N0	IO						A7
8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	D7
8	VREFB8N0	IO	VREFB8N0					B7
8	VREFB8N0	IO		CONFIG_SEL				G9
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	A6
8	VREFB8N0	Input_only		nCONFIG				H9
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	A5
8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	C6
8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low_Speed	C8
8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B5
8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	C7
8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed	C5
8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed	A4
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed	C4
8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low_Speed	B4
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	G8
8	VREFB8N0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	Low_Speed	A3
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	H8
8	VREFB8N0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	Low_Speed	B3
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	D6
8	VREFB8N0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	Low_Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	D5
8	VREFB8N0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	Low_Speed	B2
		GND						E2
		GND						E3
		GND						V18
		GND						V1
		GND						U4
		GND						U14
		GND						U10
		GND						R7
		GND						N5
		GND						N2
		GND						N17
		GND						N12
		GND						N10
		GND						M14
		GND						L4
		GND						K9
		GND						K6
		GND						K13
		GND						J17
		GND						J10
		GND						H14
		GND						G4
		GND						G2
		GND						F8
		GND						F17
		GND						E6
		GND						E13

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
		GND						E10
		GND						D3
		GND						B6
		GND						B15
		GND						B10
		GND						A18
		GND						A1
		VCC						L9
		VCC						K10
		VCC						J9
		VCC						H10
		VCC						C3
		VCCD_PLL1						N6
		VCCD_PLL2						F13
		VCCIO1A						H5
		VCCIO1A						G5
		VCCIO1B						K5
		VCCIO1B						J5
		VCCIO2						M5
		VCCIO2						L6
		VCCIO2						L5
		VCCIO3						P9
		VCCIO3						P8
		VCCIO3						P7
		VCCIO3						N9
		VCCIO4						P12
		VCCIO4						P11
		VCCIO5						M13
		VCCIO5						L14
		VCCIO5						L13
		VCCIO5						K14
		VCCIO6						J14
		VCCIO6						J13
		VCCIO6						H13
		VCCIO6						G14
		VCCIO6						G13
		VCCIO7						E12
		VCCIO7						E11
		VCCIO7						D11
		VCCIO8						F9
		VCCIO8						E9
		VCCIO8						E8
		VCCIO8						E7
		NC						N13
		NC						F7
		VCCA1						M6
		VCCA2						F14
		VCCA3						F3
		VCCA3						F6
		VCCA3						F4
		VCCA4						P13

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F484
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	F5
1A	VREFB1N0	IO			DIFFIO_RX_L2n	DIFFOUT_L2n	Low_Speed	E4
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	F4
1A	VREFB1N0	IO			DIFFIO_RX_L2p	DIFFOUT_L2p	Low_Speed	E3
1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	J8
1A	VREFB1N0	IO			DIFFIO_RX_L4n	DIFFOUT_L4n	Low_Speed	G4
1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	J9
1A	VREFB1N0	IO			DIFFIO_RX_L4p	DIFFOUT_L4p	Low_Speed	F3
1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	J4
1A	VREFB1N0	IO			DIFFIO_RX_L6n	DIFFOUT_L6n	Low_Speed	H4
1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	H3
1A	VREFB1N0	IO			DIFFIO_RX_L6p	DIFFOUT_L6p	Low_Speed	G3
1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	K5
1A	VREFB1N0	IO			DIFFIO_RX_L8n	DIFFOUT_L8n	Low_Speed	K4
1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	K6
1A	VREFB1N0	IO			DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	J3
1B	VREFB1N0	IO			DIFFIO_RX_L9n	DIFFOUT_L9n	Low_Speed	K8
1B	VREFB1N0	IO			DIFFIO_RX_L10n	DIFFOUT_L10n	Low_Speed	D3
1B	VREFB1N0	IO		JTAGEN	DIFFIO_RX_L9p	DIFFOUT_L9p	Low_Speed	K9
1B	VREFB1N0	IO			DIFFIO_RX_L10p	DIFFOUT_L10p	Low_Speed	D2
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	H2
1B	VREFB1N0	IO	VREFB1N0					C1
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	G2
1B	VREFB1N0	IO						D1
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	L4
1B	VREFB1N0	IO			DIFFIO_RX_L13n	DIFFOUT_L13n	Low_Speed	K2
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	M5
1B	VREFB1N0	IO			DIFFIO_RX_L13p	DIFFOUT_L13p	Low_Speed	L2
1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed	L8
1B	VREFB1N0	IO			DIFFIO_RX_L15n	DIFFOUT_L15n	Low_Speed	E1
1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	L9
1B	VREFB1N0	IO			DIFFIO_RX_L15p	DIFFOUT_L15p	Low_Speed	F2
1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	H1
1B	VREFB1N0	IO			DIFFIO_RX_L17n	DIFFOUT_L17n	Low_Speed	G1
1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	J1
1B	VREFB1N0	IO			DIFFIO_RX_L17p	DIFFOUT_L17p	Low_Speed	F1
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	N4
2	VREFB2N0	IO			DIFFIO_RX_L19n	DIFFOUT_L19n	High_Speed	P4
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	N5
2	VREFB2N0	IO			DIFFIO_RX_L19p	DIFFOUT_L19p	High_Speed	P5
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	M8
2	VREFB2N0	IO			DIFFIO_RX_L21n	DIFFOUT_L21n	High_Speed	N3
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	M9
2	VREFB2N0	IO			DIFFIO_RX_L21p	DIFFOUT_L21p	High_Speed	N2
2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed	P3
2	VREFB2N0	IO	VREFB2N0					M2
2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	R3
2	VREFB2N0	IO						M1
2	VREFB2N0	IO			DIFFIO_RX_L23n	DIFFOUT_L23n	High_Speed	R4
2	VREFB2N0	IO			DIFFIO_RX_L24n	DIFFOUT_L24n	High_Speed	T1
2	VREFB2N0	IO			DIFFIO_RX_L23p	DIFFOUT_L23p	High_Speed	R5
2	VREFB2N0	IO			DIFFIO_RX_L24p	DIFFOUT_L24p	High_Speed	T2
2	VREFB2N0	IO			DIFFIO_RX_L25n	DIFFOUT_L25n	High_Speed	N8
2	VREFB2N0	IO			DIFFIO_RX_L26n	DIFFOUT_L26n	High_Speed	P1
2	VREFB2N0	IO			DIFFIO_RX_L25p	DIFFOUT_L25p	High_Speed	N9
2	VREFB2N0	IO			DIFFIO_RX_L26p	DIFFOUT_L26p	High_Speed	N1
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed	T5
2	VREFB2N0	IO			DIFFIO_RX_L28n	DIFFOUT_L28n	High_Speed	R1
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	T6
2	VREFB2N0	IO			DIFFIO_RX_L28p	DIFFOUT_L28p	High_Speed	R2
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	W5
3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed	V4
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	W6
3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed	V5
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	U6
3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed	Y1
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	U7
3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed	Y2
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	W4
3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	AA1
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	W3
3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed	AA2
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	W7
3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed	Y3
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	W8
3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed	Y4
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	R10
3	VREFB3N0	IO	VREFB3N0					AA3
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	P10
3	VREFB3N0	IO						AB4
3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed	AA6
3	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	High_Speed	AA5
3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	AA7
3	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	High_Speed	AB5
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	V9
3	VREFB3N0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	High_Speed	AB6
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	V10
3	VREFB3N0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	High_Speed	AB7
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	R11
3	VREFB3N0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	High_Speed	AA8
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	P11

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F484
3	VREFB3N0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	High_Speed	AB8
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	Y10
3	VREFB3N0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	High_Speed	AA9
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	AA10
3	VREFB3N0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	High_Speed	AB9
4	VREFB4N0	IO			DIFFIO_TX_RX_B18n	DIFFOUT_B18n	High_Speed	V13
4	VREFB4N0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	High_Speed	W12
4	VREFB4N0	IO			DIFFIO_TX_RX_B18p	DIFFOUT_B18p	High_Speed	W14
4	VREFB4N0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	High_Speed	W13
4	VREFB4N0	IO			DIFFIO_TX_RX_B20n	DIFFOUT_B20n	High_Speed	R13
4	VREFB4N0	IO	VREFB4N0					AA13
4	VREFB4N0	IO			DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed	P13
4	VREFB4N0	IO						AB14
4	VREFB4N0	IO			DIFFIO_TX_RX_B21n	DIFFOUT_B21n	High_Speed	Y13
4	VREFB4N0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	High_Speed	AA14
4	VREFB4N0	IO			DIFFIO_TX_RX_B21p	DIFFOUT_B21p	High_Speed	Y14
4	VREFB4N0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	High_Speed	AB15
4	VREFB4N0	IO			DIFFIO_TX_RX_B23n	DIFFOUT_B23n	High_Speed	V14
4	VREFB4N0	IO			DIFFIO_RX_B24n	DIFFOUT_B24n	High_Speed	AA15
4	VREFB4N0	IO			DIFFIO_TX_RX_B23p	DIFFOUT_B23p	High_Speed	W15
4	VREFB4N0	IO			DIFFIO_RX_B24p	DIFFOUT_B24p	High_Speed	Y16
4	VREFB4N0	IO			DIFFIO_TX_RX_B25n	DIFFOUT_B25n	High_Speed	U15
4	VREFB4N0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	High_Speed	AB16
4	VREFB4N0	IO			DIFFIO_TX_RX_B25p	DIFFOUT_B25p	High_Speed	V16
4	VREFB4N0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	High_Speed	AA16
4	VREFB4N0	IO			DIFFIO_TX_RX_B27n	DIFFOUT_B27n	High_Speed	W17
4	VREFB4N0	IO			DIFFIO_RX_B28n	DIFFOUT_B28n	High_Speed	AB17
4	VREFB4N0	IO			DIFFIO_TX_RX_B27p	DIFFOUT_B27p	High_Speed	V17
4	VREFB4N0	IO			DIFFIO_RX_B28p	DIFFOUT_B28p	High_Speed	AB18
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	U18
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	AA21
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	U17
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	AA22
5	VREFB5N0	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	High_Speed	R15
5	VREFB5N0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	High_Speed	T21
5	VREFB5N0	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	High_Speed	R14
5	VREFB5N0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	High_Speed	T22
5	VREFB5N0	IO			DIFFIO_RX_R5p	DIFFOUT_R5p	High_Speed	T19
5	VREFB5N0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	High_Speed	T20
5	VREFB5N0	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	High_Speed	T18
5	VREFB5N0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	High_Speed	R20
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	U21
5	VREFB5N0	IO						R22
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	U22
5	VREFB5N0	IO	VREFB5N0					P22
5	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	High_Speed	P15
5	VREFB5N0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	High_Speed	P21
5	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	High_Speed	P14
5	VREFB5N0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	High_Speed	N22
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	R18
5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	P19
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	P18
5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	P20
5	VREFB5N0	IO			DIFFIO_RX_R12p	DIFFOUT_R12p	High_Speed	M21
5	VREFB5N0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	High_Speed	N21
5	VREFB5N0	IO			DIFFIO_RX_R12n	DIFFOUT_R12n	High_Speed	L22
5	VREFB5N0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	High_Speed	M22
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	N14
6	VREFB6N0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	High_Speed	H22
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	N15
6	VREFB6N0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	High_Speed	H21
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	K22
6	VREFB6N0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	High_Speed	J22
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	K21
6	VREFB6N0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	High_Speed	J21
6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	G20
6	VREFB6N0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	High_Speed	G22
6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed	G19
6	VREFB6N0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	High_Speed	F22
6	VREFB6N0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed	M15
6	VREFB6N0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	High_Speed	E22
6	VREFB6N0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	High_Speed	M14
6	VREFB6N0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	High_Speed	E21
6	VREFB6N0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed	N18
6	VREFB6N0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	High_Speed	M20
6	VREFB6N0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	High_Speed	N19
6	VREFB6N0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	High_Speed	N20
6	VREFB6N0	IO			DIFFIO_RX_R24p	DIFFOUT_R24p	High_Speed	F21
6	VREFB6N0	IO			DIFFIO_RX_R25p	DIFFOUT_R25p	High_Speed	D22
6	VREFB6N0	IO			DIFFIO_RX_R24n	DIFFOUT_R24n	High_Speed	F20
6	VREFB6N0	IO			DIFFIO_RX_R25n	DIFFOUT_R25n	High_Speed	C22
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed	L14
6	VREFB6N0	IO	VREFB6N0					D21
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	L15
6	VREFB6N0	IO						C21
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	M18
6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed	L19
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	L18
6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed	L20
6	VREFB6N0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	High_Speed	E19
6	VREFB6N0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	High_Speed	F18

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F484
6	VREFB6N0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	High_Speed	K14
6	VREFB6N0	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	C20
6	VREFB6N0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	High_Speed	K15
6	VREFB6N0	IO			DIFFIO_RX_R32n	DIFFOUT_R32n	High_Speed	D19
6	VREFB6N0	IO	PLL_R_CLKOUTp		DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	H17
6	VREFB6N0	IO			DIFFIO_RX_R34p	DIFFOUT_R34p	High_Speed	D18
6	VREFB6N0	IO	PLL_R_CLKOUTn		DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	G17
6	VREFB6N0	IO			DIFFIO_RX_R34n	DIFFOUT_R34n	High_Speed	E18
7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed	E16
7	VREFB7N0	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	High_Speed	D17
7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed	E15
7	VREFB7N0	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	High_Speed	C17
7	VREFB7N0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	High_Speed	H14
7	VREFB7N0	IO						A15
7	VREFB7N0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	High_Speed	J13
7	VREFB7N0	IO	VREFB7N0					B15
7	VREFB7N0	IO			DIFFIO_RX_T4p	DIFFOUT_T4p	High_Speed	C14
7	VREFB7N0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	High_Speed	A14
7	VREFB7N0	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	High_Speed	C13
7	VREFB7N0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	High_Speed	B14
7	VREFB7N0	IO			DIFFIO_RX_T6p	DIFFOUT_T6p	High_Speed	D14
7	VREFB7N0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	High_Speed	E12
7	VREFB7N0	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	High_Speed	E13
7	VREFB7N0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	High_Speed	D13
7	VREFB7N0	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	High_Speed	H12
7	VREFB7N0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	High_Speed	A7
7	VREFB7N0	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	High_Speed	J11
7	VREFB7N0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	High_Speed	A8
7	VREFB7N0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed	B10
7	VREFB7N0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	High_Speed	A9
7	VREFB7N0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	High_Speed	C9
7	VREFB7N0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	High_Speed	B8
8	VREFB8N0	IO			DIFFIO_RX_T12p	DIFFOUT_T12p	Low_Speed	E11
8	VREFB8N0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	Low_Speed	C8
8	VREFB8N0	IO			DIFFIO_RX_T12n	DIFFOUT_T12n	Low_Speed	E10
8	VREFB8N0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	Low_Speed	C7
8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed	J10
8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low_Speed	B7
8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed	H11
8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed	A6
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	D8
8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed	A5
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	D9
8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed	A4
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	D10
8	VREFB8N0	IO						C6
8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	E9
8	VREFB8N0	IO	VREFB8N0					D7
8	VREFB8N0	IO		CONFIG_SEL				H10
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	A2
8	VREFB8N0	Input_only		nCONFIG				H9
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	A3
8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	B3
8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low_Speed	B5
8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B4
8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	C4
8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed	E8
8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed	C5
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed	F7
8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low_Speed	D5
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	G9
8	VREFB8N0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	Low_Speed	B2
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	F8
8	VREFB8N0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	Low_Speed	B1
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	D6
8	VREFB8N0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	Low_Speed	C3
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	E6
8	VREFB8N0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	Low_Speed	C2
		GND						F6
		GND						E5
		GND						G5
		GND						K3
		GND						H5
		GND						Y9
		GND						Y15
		GND						Y12
		GND						W21
		GND						V6
		GND						V2
		GND						V19
		GND						U13
		GND						U10
		GND						T8
		GND						T4
		GND						T16
		GND						T14
		GND						R21
		GND						R19
		GND						P6
		GND						P2
		GND						P17

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F484
		GND						N13
		GND						N11
		GND						M7
		GND						M19
		GND						M16
		GND						M10
		GND						L5
		GND						L21
		GND						L17
		GND						L13
		GND						K12
		GND						K10
		GND						J6
		GND						J2
		GND						J19
		GND						J16
		GND						G8
		GND						G6
		GND						G21
		GND						G18
		GND						G15
		GND						F13
		GND						F10
		GND						E7
		GND						E2
		GND						D4
		GND						D20
		GND						D16
		GND						D11
		GND						B9
		GND						B6
		GND						B18
		GND						B13
		GND						AB22
		GND						AB1
		GND						AA4
		GND						AA18
		GND						A22
		GND						A1
		VCC						N12
		VCC						N10
		VCC						M13
		VCC						M12
		VCC						M11
		VCC						L12
		VCC						L11
		VCC						L10
		VCC						K13
		VCC						K11
		VCC						J7
		DNU						L3
		VCCD_PLL1						T7
		VCCD_PLL2						G16
		VCCIO1A						L6
		VCCIO1A						K7
		VCCIO1B						M6
		VCCIO1B						L7
		VCCIO2						R6
		VCCIO2						P7
		VCCIO2						N7
		VCCIO2						N6
		VCCIO3						U9
		VCCIO3						U8
		VCCIO3						T9
		VCCIO3						T11
		VCCIO3						T10
		VCCIO4						U14
		VCCIO4						U12
		VCCIO4						U11
		VCCIO4						T13
		VCCIO4						T12
		VCCIO5						T17
		VCCIO5						R17
		VCCIO5						R16
		VCCIO5						P16
		VCCIO5						N16
		VCCIO6						N17
		VCCIO6						M17
		VCCIO6						L16
		VCCIO6						K17
		VCCIO6						K16
		VCCIO6						J17
		VCCIO6						H16
		VCCIO7						G14
		VCCIO7						G13
		VCCIO7						G12
		VCCIO7						F14
		VCCIO7						F12
		VCCIO8						G11
		VCCIO8						G10
		VCCIO8						F9

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F484
		VCCIO8						F11
		NC						Y8
		NC						Y7
		NC						Y6
		NC						Y5
		NC						Y22
		NC						Y21
		NC						Y20
		NC						Y19
		NC						Y18
		NC						Y17
		NC						Y11
		NC						W9
		NC						W22
		NC						W20
		NC						W2
		NC						W19
		NC						W18
		NC						W16
		NC						W11
		NC						W10
		NC						W1
		NC						V8
		NC						V7
		NC						V3
		NC						V22
		NC						V21
		NC						V20
		NC						V18
		NC						V15
		NC						V12
		NC						V11
		NC						V1
		NC						U5
		NC						U4
		NC						U3
		NC						U20
		NC						U2
		NC						U19
		NC						U16
		NC						U1
		NC						T3
		NC						R9
		NC						R7
		NC						R12
		NC						P9
		NC						P8
		NC						P12
		NC						M4
		NC						M3
		NC						L1
		NC						K20
		NC						K19
		NC						K18
		NC						K1
		NC						J5
		NC						J20
		NC						J18
		NC						J15
		NC						J14
		NC						J12
		NC						H20
		NC						H19
		NC						H18
		NC						H13
		NC						G7
		NC						F19
		NC						F17
		NC						F16
		NC						F15
		NC						E20
		NC						E17
		NC						E14
		NC						D15
		NC						D12
		NC						C19
		NC						C18
		NC						C16
		NC						C15
		NC						C12
		NC						C11
		NC						C10
		NC						B22
		NC						B21
		NC						B20
		NC						B19
		NC						B17
		NC						B16
		NC						B12
		NC						B11
		NC						AB3

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	F484
		NC						AB21
		NC						AB20
		NC						AB2
		NC						AB19
		NC						AB13
		NC						AB12
		NC						AB11
		NC						AB10
		NC						AA20
		NC						AA19
		NC						AA17
		NC						AA12
		NC						AA11
		NC						A21
		NC						A20
		NC						A19
		NC						A18
		NC						A17
		NC						A16
		NC						A13
		NC						A12
		NC						A11
		NC						A10
		VCCA1						R8
		VCCA2						H15
		VCCA3						H6
		VCCA3						H8
		VCCA3						H7
		VCCA4						T15

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the
MAX 10 FPGA Device Family Pin Connection Guidelines.

Date	Version	Changes Made
September 2014	2014.09.22	Initial release.
December 2014	2014.12.15	-Updated the BOOT_SEL pin name to CONFIG_SEL pin name. -Removed differential pair pins for non-differential function support.
December 2016	2016.12.23	Removed I/O performance for single-ended pins.
February 2017	2017.02.21	Rebranded as Intel.