| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | VCCD_PLL7 | | | L29 | | | |
| | | VCCA_PLL7 | | | M29 | | | |
| | | GNDA_PLL7 | | | K29 | | | |
| | | GNDA_PLL7 | | | K30 | | | |
| B2 | | FPLL7CLKp | INPUT | | C39 | | | |
| B2 | | FPLL7CLKn | INPUT | | C38 | | | |
| | | NC (Note 3) | | | D38 | | | |
| | | NC (Note 4) | | | J32 | | | |
| | | NC (Note 4) | | | J31 | | | |
| | | NC (Note 4) | | | C37 | | | |
| | | NC (Note 4) | | | C36 | | | |
| | | NC (Note 4) | | | L31 | | | |
| | | NC (Note 4) | | | L30 | | | |
| | | NC (Note 4) | | | D37 | | | |
| | | NC (Note 4) | | | D36 | | | |
| | | NC (Note 4) | | | K32 | | | |
| | | NC (Note 4) | | | K31 | | | |
| | | NC (Note 4) | | | B38 | | | |
| | | NC (Note 4) | | | B37 | | | |
| | | NC (Note 4) | | | H32 | | | |
| | | NC (Note 4) | | | H31 | | | |
| | | NC (Note 4) | | | J34 | | | |
| | | NC (Note 4) | | | J33 | | | |
| | | NC (Note 4) | | | F35 | | | |
| | | NC (Note 4) | | | F34 | | | |
| | | NC (Note 4) | | | G35 | | | |
| | | NC (Note 4) | | | G34 | | | |
| | | NC (Note 4) | | | L33 | | | |
| | | NC (Note 4) | | | L32 | | | |
| | | NC (Note 3) | | | G33 | | | |
| | | NC (Note 4) | | | H35 | | | |
| | | NC (Note 4) | | | H34 | | | |
| | | NC (Note 4) | | | M31 | | | |
| | | NC (Note 4) | | | M30 | | | |
| | | NC (Note 4) | | | E37 | | | |
| | | NC (Note 4) | | | E36 | | | |
| | | NC (Note 4) | | | E35 | | | |
| | | NC (Note 4) | | | E34 | | | |
| | | NC (Note 4) | | | F37 | | | |
| | | NC (Note 4) | | | F36 | | | |
| B2 | | IO | DIFFIO_TX71p | | M33 | | | |
| B2 | | IO | DIFFIO_TX71n | | M32 | | | |
| B2 | | IO | DIFFIO_RX70p | | K35 | | | |
| B2 | | IO | DIFFIO_RX70n | | K34 | | | |
| B2 | | IO | DIFFIO_TX70p | | N31 | | | |
| B2 | | IO | DIFFIO_TX70n | | N30 | | | |
| B2 | | IO | DIFFIO_RX69p | | E39 | | | |
| B2 | | IO | DIFFIO_RX69n | | E38 | | | |
| B2 | | IO | DIFFIO_TX69p | | N29 | | | |
| B2 | | IO | DIFFIO_TX69n | | N28 | | | |
| B2 | | IO | DIFFIO_RX68p | | F39 | | | |
| B2 | | IO | DIFFIO_RX68n | | F38 | | | |
| B2 | | IO | DIFFIO_TX68p | | P27 | | | |
| B2 | | IO | DIFFIO_TX68n | | P26 | | | |
| B2 | | IO | DIFFIO_RX67p | | L35 | | | |
| B2 | | IO | DIFFIO_RX67n | | L34 | | | |
| B2 | | IO | DIFFIO_TX67p | | P29 | | | |
| B2 | | IO | DIFFIO_TX67n | | P28 | | | |
| B2 | | IO | DIFFIO_RX66p | | G39 | | | |
| B2 | | IO | DIFFIO_RX66n | | G38 | | | |
| B2 | | IO | DIFFIO_TX66p | | R28 | | | |
| B2 | | IO | DIFFIO_TX66n | | R27 | | | |
| B2 | | IO | DIFFIO_RX65p | | J37 | | | |
| B2 | | IO | DIFFIO_RX65n | | J36 | | | |
| B2 | | IO | DIFFIO_TX65p | | N33 | | | |
| B2 | | IO | DIFFIO_TX65n | | N32 | | | |
| | | NC (Note 3) | | | J35 | | | |
| B2 | | IO | DIFFIO_RX64p | | H37 | | | |
| B2 | | IO | DIFFIO_RX64n | | H36 | | | |
| B2 | | IO | DIFFIO_TX64p | | M35 | | | |
| B2 | | IO | DIFFIO_TX64n | | M34 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B2 | | IO | DIFFIO_RX63p | | G37 | | | |
| B2 | | IO | DIFFIO_RX63n | | G36 | | | |
| B2 | | IO | DIFFIO_TX63p | | P31 | | | |
| B2 | | IO | DIFFIO_TX63n | | P30 | | | |
| B2 | | IO | DIFFIO_RX62p | | L37 | | | |
| B2 | | IO | DIFFIO_RX62n | | L36 | | | |
| B2 | | IO | DIFFIO_TX62p | | P33 | | | |
| B2 | | IO | DIFFIO_TX62n | | P32 | | | |
| B2 | | IO | DIFFIO_RX61p | | K37 | | | |
| B2 | | IO | DIFFIO_RX61n | | K36 | | | |
| B2 | | IO | DIFFIO_TX61p | | R32 | | | |
| B2 | | IO | DIFFIO_TX61n | | R31 | | | |
| B2 | | IO | DIFFIO_RX60p | | M37 | | | |
| B2 | | IO | DIFFIO_RX60n | | M36 | | | |
| B2 | | IO | DIFFIO_TX60p | | N35 | | | |
| B2 | | IO | DIFFIO_TX60n | | N34 | | | |
| B2 | | IO | DIFFIO_RX59p | | H39 | | | |
| B2 | | IO | DIFFIO_RX59n | | H38 | | | |
| B2 | | IO | DIFFIO_TX59p | | R30 | | | |
| B2 | | IO | DIFFIO_TX59n | | R29 | | | |
| B2 | | IO | DIFFIO_RX58p | | J39 | | | |
| B2 | | IO | DIFFIO_RX58n | | J38 | | | |
| B2 | | IO | DIFFIO_TX58p | | P35 | | | |
| B2 | | IO | DIFFIO_TX58n | | P34 | | | |
| B2 | | IO | DIFFIO_RX57p | | N37 | | | |
| B2 | | IO | DIFFIO_RX57n | | N36 | | | |
| B2 | | IO | DIFFIO_TX57p | | T30 | | | |
| B2 | | IO | DIFFIO_TX57n | | T29 | | | |
| B2 | | IO | DIFFIO_RX56p | | K39 | | | |
| B2 | | IO | DIFFIO_RX56n | | K38 | | | |
| B2 | | IO | DIFFIO_TX56p | | T32 | | | |
| B2 | | IO | DIFFIO_TX56n | | T31 | | | |
| | | NC (Note 3) | | | R35 | | | |
| B2 | | IO | DIFFIO_RX55p | | L39 | | | |
| B2 | | IO | DIFFIO_RX55n | | L38 | | | |
| B2 | | IO | DIFFIO_TX55p | | R34 | | | |
| B2 | | IO | DIFFIO_TX55n | | R33 | | | |
| B2 | | IO | DIFFIO_RX54p | | M39 | | | |
| B2 | | IO | DIFFIO_RX54n | | M38 | | | |
| B2 | | IO | DIFFIO_TX54p | | T34 | | | |
| B2 | | IO | DIFFIO_TX54n | | T33 | | | |
| B2 | | IO | DIFFIO_RX53p | | N39 | | | |
| B2 | | IO | DIFFIO_RX53n | | N38 | | | |
| B2 | | IO | DIFFIO_TX53p | | T28 | | | |
| B2 | | IO | DIFFIO_TX53n | | T27 | | | |
| B2 | | IO | DIFFIO_RX52p | | T36 | | | |
| B2 | | IO | DIFFIO_RX52n | | T35 | | | |
| B2 | | IO | DIFFIO_TX52p | | U32 | | | |
| B2 | | IO | DIFFIO_TX52n | | U31 | | | |
| B2 | | IO | DIFFIO_RX51p | | R37 | | | |
| B2 | | IO | DIFFIO_RX51n | | R36 | | | |
| B2 | | IO | DIFFIO_TX51p | | U30 | | | |
| B2 | | IO | DIFFIO_TX51n | | U29 | | | |
| B2 | | IO | DIFFIO_RX50p | | P37 | | | |
| B2 | | IO | DIFFIO_RX50n | | P36 | | | |
| B2 | | IO | DIFFIO_TX50p | | U34 | | | |
| B2 | | IO | DIFFIO_TX50n | | U33 | | | |
| B2 | | IO | DIFFIO_RX49p | | P39 | | | |
| B2 | | IO | DIFFIO_RX49n | | P38 | | | |
| B2 | | IO | DIFFIO_TX49p | | U28 | | | |
| B2 | | IO | DIFFIO_TX49n | | U27 | | | |
| B2 | | IO | DIFFIO_RX48p | | U37 | | | |
| B2 | | IO | DIFFIO_RX48n | | U36 | | | |
| B2 | | IO | DIFFIO_TX48p | | V28 | | | |
| B2 | | IO | DIFFIO_TX48n | | V27 | | | |
| B2 | | IO | DIFFIO_RX47p | | V36 | | | |
| B2 | | IO | DIFFIO_RX47n | | V35 | | | |
| B2 | | IO | DIFFIO_TX47p | | V32 | | | |
| B2 | | IO | DIFFIO_TX47n | | V31 | | | |
| | | NC (Note 3) | | | W34 | | | |
| B2 | | IO | DIFFIO_RX46p | | T38 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B2 | | IO | DIFFIO_RX46n | | T37 | | | |
| B2 | | IO | DIFFIO_TX46p | | V34 | | | |
| B2 | | IO | DIFFIO_TX46n | | V33 | | | |
| B2 | | IO | DIFFIO_RX45p | | R39 | | | |
| B2 | | IO | DIFFIO_RX45n | | R38 | | | |
| B2 | | IO | DIFFIO_TX45p | | W33 | | | |
| B2 | | IO | DIFFIO_TX45n | | W32 | | | |
| B2 | | IO | DIFFIO_RX44p | | V38 | | | |
| B2 | | IO | DIFFIO_RX44n | | V37 | | | |
| B2 | | IO | DIFFIO_TX44p | | W28 | | | |
| B2 | | IO | DIFFIO_TX44n | | W27 | | | |
| B2 | | IO | DIFFIO_RX43p | | U39 | | | |
| B2 | | IO | DIFFIO_RX43n | | U38 | | | |
| B2 | | IO | DIFFIO_TX43p | | Y27 | | | |
| B2 | | IO | DIFFIO_TX43n | | Y26 | | | |
| B2 | | IO | CLK0n/DIFFIO_RX_C0n | | W38 | | | |
| B2 | | IO | CLK0p/DIFFIO_RX_C0p | | W39 | | | |
| B2 | | CLK1n | INPUT | | W36 | | | |
| B2 | | CLK1p | INPUT | | W37 | | | |
| | | VCCD_PLL1 | | | V29 | | | |
| | | VCCA_PLL1 | | | V30 | | | |
| | | GNDA_PLL1 | | | W30 | | | |
| | | GNDA_PLL1 | | | W31 | | | |
| | | GNDA_PLL2 | | | Y29 | | | |
| | | GNDA_PLL2 | | | Y30 | | | |
| | | VCCA_PLL2 | | | W29 | | | |
| | | VCCD_PLL2 | | | Y28 | | | |
| B1 | | IO | CLK2p/DIFFIO_RX_C1p | | Y39 | | | |
| B1 | | IO | CLK2n/DIFFIO_RX_C1n | | Y38 | | | |
| B1 | | CLK3p | INPUT | | Y37 | | | |
| B1 | | CLK3n | INPUT | | Y36 | | | |
| B1 | | IO | DIFFIO_RX42p | | AA39 | | | |
| B1 | | IO | DIFFIO_RX42n | | AA38 | | | |
| B1 | | IO | DIFFIO_TX42p | | AA31 | | | |
| B1 | | IO | DIFFIO_TX42n | | AA30 | | | |
| B1 | | IO | DIFFIO_RX41p | | AA37 | | | |
| B1 | | IO | DIFFIO_RX41n | | AA36 | | | |
| B1 | | IO | DIFFIO_TX41p | | AA29 | | | |
| B1 | | IO | DIFFIO_TX41n | | AA28 | | | |
| B1 | | IO | DIFFIO_RX40p | | AB38 | | | |
| B1 | | IO | DIFFIO_RX40n | | AB37 | | | |
| B1 | | IO | DIFFIO_TX40p | | Y33 | | | |
| B1 | | IO | DIFFIO_TX40n | | Y32 | | | |
| | | NC (Note 3) | | | AA34 | | | |
| B1 | | IO | DIFFIO_RX39p | | AC39 | | | |
| B1 | | IO | DIFFIO_RX39n | | AC38 | | | |
| B1 | | IO | DIFFIO_TX39p | | AA33 | | | |
| B1 | | IO | DIFFIO_TX39n | | AA32 | | | |
| B1 | | IO | DIFFIO_RX38p | | AB36 | | | |
| B1 | | IO | DIFFIO_RX38n | | AB35 | | | |
| B1 | | IO | DIFFIO_TX38p | | Y35 | | | |
| B1 | | IO | DIFFIO_TX38n | | Y34 | | | |
| B1 | | IO | DIFFIO_RX37p | | AE39 | | | |
| B1 | | IO | DIFFIO_RX37n | | AE38 | | | |
| B1 | | IO | DIFFIO_TX37p | | AB30 | | | |
| B1 | | IO | DIFFIO_TX37n | | AB29 | | | |
| B1 | | IO | DIFFIO_RX36p | | AD38 | | | |
| B1 | | IO | DIFFIO_RX36n | | AD37 | | | |
| B1 | | IO | DIFFIO_TX36p | | AA27 | | | |
| B1 | | IO | DIFFIO_TX36n | | AA26 | | | |
| B1 | | IO | DIFFIO_RX35p | | AC37 | | | |
| B1 | | IO | DIFFIO_RX35n | | AC36 | | | |
| B1 | | IO | DIFFIO_TX35p | | AB32 | | | |
| B1 | | IO | DIFFIO_TX35n | | AB31 | | | |
| B1 | | IO | DIFFIO_RX34p | | AE37 | | | |
| B1 | | IO | DIFFIO_RX34n | | AE36 | | | |
| B1 | | IO | DIFFIO_TX34p | | AB34 | | | |
| B1 | | IO | DIFFIO_TX34n | | AB33 | | | |
| B1 | | IO | DIFFIO_RX33p | | AD36 | | | |
| B1 | | IO | DIFFIO_RX33n | | AD35 | | | |
| B1 | | IO | DIFFIO_TX33p | | AB28 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B1 | | IO | DIFFIO_TX33n | | AB27 | | | |
| B1 | | IO | DIFFIO_RX32p | | AF39 | | | |
| B1 | | IO | DIFFIO_RX32n | | AF38 | | | |
| B1 | | IO | DIFFIO_TX32p | | AC30 | | | |
| B1 | | IO | DIFFIO_TX32n | | AC29 | | | |
| | | NC (Note 3) | | | AG35 | | | |
| B1 | | IO | DIFFIO_RX31p | | AG39 | | | |
| B1 | | IO | DIFFIO_RX31n | | AG38 | | | |
| B1 | | IO | DIFFIO_TX31p | | AC28 | | | |
| B1 | | IO | DIFFIO_TX31n | | AC27 | | | |
| B1 | | IO | DIFFIO_RX30p | | AH39 | | | |
| B1 | | IO | DIFFIO_RX30n | | AH38 | | | |
| B1 | | IO | DIFFIO_TX30p | | AC32 | | | |
| B1 | | IO | DIFFIO_TX30n | | AC31 | | | |
| B1 | | IO | DIFFIO_RX29p | | AF37 | | | |
| B1 | | IO | DIFFIO_RX29n | | AF36 | | | |
| B1 | | IO | DIFFIO_TX29p | | AC34 | | | |
| B1 | | IO | DIFFIO_TX29n | | AC33 | | | |
| B1 | | IO | DIFFIO_RX28p | | AJ39 | | | |
| B1 | | IO | DIFFIO_RX28n | | AJ38 | | | |
| B1 | | IO | DIFFIO_TX28p | | AD32 | | | |
| B1 | | IO | DIFFIO_TX28n | | AD31 | | | |
| B1 | | IO | DIFFIO_RX27p | | AK39 | | | |
| B1 | | IO | DIFFIO_RX27n | | AK38 | | | |
| B1 | | IO | DIFFIO_TX27p | | AD34 | | | |
| B1 | | IO | DIFFIO_TX27n | | AD33 | | | |
| B1 | | IO | DIFFIO_RX26p | | AG37 | | | |
| B1 | | IO | DIFFIO_RX26n | | AG36 | | | |
| B1 | | IO | DIFFIO_TX26p | | AD29 | | | |
| B1 | | IO | DIFFIO_TX26n | | AD28 | | | |
| B1 | | IO | DIFFIO_RX25p | | AL39 | | | |
| B1 | | IO | DIFFIO_RX25n | | AL38 | | | |
| B1 | | IO | DIFFIO_TX25p | | AD27 | | | |
| B1 | | IO | DIFFIO_TX25n | | AD26 | | | |
| B1 | | IO | DIFFIO_RX24p | | AH37 | | | |
| B1 | | IO | DIFFIO_RX24n | | AH36 | | | |
| B1 | | IO | DIFFIO_TX24p | | AE31 | | | |
| B1 | | IO | DIFFIO_TX24n | | AE30 | | | |
| B1 | | IO | DIFFIO_RX23p | | AM39 | | | |
| B1 | | IO | DIFFIO_RX23n | | AM38 | | | |
| B1 | | IO | DIFFIO_TX23p | | AE33 | | | |
| B1 | | IO | DIFFIO_TX23n | | AE32 | | | |
| | | NC (Note 3) | | | AN35 | | | |
| B1 | | IO | DIFFIO_RX22p | | AJ37 | | | |
| B1 | | IO | DIFFIO_RX22n | | AJ36 | | | |
| B1 | | IO | DIFFIO_TX22p | | AE35 | | | |
| B1 | | IO | DIFFIO_TX22n | | AE34 | | | |
| B1 | | IO | DIFFIO_RX21p | | AL37 | | | |
| B1 | | IO | DIFFIO_RX21n | | AL36 | | | |
| B1 | | IO | DIFFIO_TX21p | | AF33 | | | |
| B1 | | IO | DIFFIO_TX21n | | AF32 | | | |
| B1 | | IO | DIFFIO_RX20p | | AK37 | | | |
| B1 | | IO | DIFFIO_RX20n | | AK36 | | | |
| B1 | | IO | DIFFIO_TX20p | | AF35 | | | |
| B1 | | IO | DIFFIO_TX20n | | AF34 | | | |
| B1 | | IO | DIFFIO_RX19p | | AH35 | | | |
| B1 | | IO | DIFFIO_RX19n | | AH34 | | | |
| B1 | | IO | DIFFIO_TX19p | | AE29 | | | |
| B1 | | IO | DIFFIO_TX19n | | AE28 | | | |
| B1 | | IO | DIFFIO_RX18p | | AG34 | | | |
| B1 | | IO | DIFFIO_RX18n | | AG33 | | | |
| B1 | | IO | DIFFIO_TX18p | | AF30 | | | |
| B1 | | IO | DIFFIO_TX18n | | AF29 | | | |
| B1 | | IO | DIFFIO_RX17p | | AN39 | | | |
| B1 | | IO | DIFFIO_RX17n | | AN38 | | | |
| B1 | | IO | DIFFIO_TX17p | | AE27 | | | |
| B1 | | IO | DIFFIO_TX17n | | AE26 | | | |
| B1 | | IO | DIFFIO_RX16p | | AP39 | | | |
| B1 | | IO | DIFFIO_RX16n | | AP38 | | | |
| B1 | | IO | DIFFIO_TX16p | | AF28 | | | |
| B1 | | IO | DIFFIO_TX16n | | AF27 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B1 | | IO | DIFFIO_RX15p | | AJ35 | | | |
| B1 | | IO | DIFFIO_RX15n | | AJ34 | | | |
| B1 | | IO | DIFFIO_TX15p | | AG32 | | | |
| B1 | | IO | DIFFIO_TX15n | | AG31 | | | |
| | | NC (Note 4) | | | AR39 | | | |
| | | NC (Note 4) | | | AR38 | | | |
| B1 | | IO | DIFFIO_TX14p | | AG30 | | | |
| B1 | | IO | DIFFIO_TX14n | | AG29 | | | |
| | | NC (Note 3) | | | AL33 | | | |
| | | NC (Note 4) | | | AM37 | | | |
| | | NC (Note 4) | | | AM36 | | | |
| | | NC (Note 4) | | | AH33 | | | |
| | | NC (Note 4) | | | AH32 | | | |
| | | NC (Note 4) | | | AK35 | | | |
| | | NC (Note 4) | | | AK34 | | | |
| | | NC (Note 4) | | | AG28 | | | |
| | | NC (Note 4) | | | AG27 | | | |
| | | NC (Note 4) | | | AN37 | | | |
| | | NC (Note 4) | | | AN36 | | | |
| | | NC (Note 4) | | | AH29 | | | |
| | | NC (Note 4) | | | AH28 | | | |
| | | NC (Note 4) | | | AL35 | | | |
| | | NC (Note 4) | | | AL34 | | | |
| | | NC (Note 4) | | | AH31 | | | |
| | | NC (Note 4) | | | AH30 | | | |
| | | NC (Note 4) | | | AV38 | | | |
| | | NC (Note 4) | | | AV37 | | | |
| | | NC (Note 4) | | | AJ33 | | | |
| | | NC (Note 4) | | | AJ32 | | | |
| | | NC (Note 4) | | | AP37 | | | |
| | | NC (Note 4) | | | AP36 | | | |
| | | NC (Note 4) | | | AJ31 | | | |
| | | NC (Note 4) | | | AJ30 | | | |
| | | NC (Note 4) | | | AM35 | | | |
| | | NC (Note 4) | | | AM34 | | | |
| | | NC (Note 4) | | | AT35 | | | |
| | | NC (Note 4) | | | AT34 | | | |
| | | NC (Note 4) | | | AU37 | | | |
| | | NC (Note 4) | | | AU36 | | | |
| | | NC (Note 4) | | | AR35 | | | |
| | | NC (Note 4) | | | AR34 | | | |
| | | NC (Note 4) | | | AR37 | | | |
| | | NC (Note 4) | | | AR36 | | | |
| | | NC (Note 4) | | | AN34 | | | |
| | | NC (Note 4) | | | AN33 | | | |
| | | NC (Note 3) | | | AT38 | | | |
| | | NC (Note 4) | | | AT37 | | | |
| | | NC (Note 4) | | | AT36 | | | |
| | | NC (Note 4) | | | AK32 | | | |
| | | NC (Note 4) | | | AK31 | | | |
| | | NC (Note 4) | | | AP35 | | | |
| | | NC (Note 4) | | | AP34 | | | |
| | | NC (Note 4) | | | AL32 | | | |
| | | NC (Note 4) | | | AL31 | | | |
| | | NC (Note 4) | | | AM32 | | | |
| | | NC (Note 4) | | | AM31 | | | |
| B1 | | FPLL8CLKn | INPUT | | AU38 | | | |
| B1 | | FPLL8CLKp | INPUT | | AU39 | | | |
| | | GNDA_PLL8 | | | AK29 | | | |
| | | GNDA_PLL8 | | | AL29 | | | |
| | | VCCA_PLL8 | | | AJ29 | | | |
| | | VCCD_PLL8 | | | AK30 | | | |
| B8 | VREFB8N0 | TDI | | TDI | AN31 | | | |
| B8 | VREFB8N0 | TMS | | TMS | AP33 | | | |
| B8 | VREFB8N0 | TCK | | TCK | AP32 | | | |
| B8 | VREFB8N0 | TRST | | TRST | AW37 | | | |
| B8 | VREFB8N0 | nCONFIG | | nCONFIG | AM30 | | | |
| B8 | VREFB8N0 | VCCSEL | | VCCSEL | AV36 | | | |
| B8 | VREFB8N0 | IO | | | AP29 | | | |
| B8 | VREFB8N0 | IO | | | AM29 | | | |
| B8 | VREFB8N0 | IO | | CS | AR32 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B8 | VREFB8N0 | IO | | CLKUSR | AP30 | | | |
| B8 | VREFB8N0 | IO | | nWS | AR31 | | | |
| B8 | VREFB8N0 | IO | | nRS | AR30 | | | |
| B8 | VREFB8N0 | VREFB8N0 | VREFB8N0 | | AR33 | | | |
| B8 | VREFB8N0 | IO | | | AN29 | | | |
| B8 | VREFB8N0 | IO | DQ17B | | AU34 | DQ8B | | |
| B8 | VREFB8N0 | IO | DQSn17B | | AV35 | DQ8B | DQ3B | DQ1B |
| B8 | VREFB8N0 | IO | DQ17B | | AU35 | DQ8B | DQ3B | |
| B8 | VREFB8N0 | IO | DQ17B | | AW35 | DQ8B | DQ3B | DQ1B |
| B8 | VREFB8N0 | IO | DQ17B | | AW34 | DQ8B | DQ3B | DQ1B |
| B8 | VREFB8N0 | IO | DQS17B | | AV34 | DQVLD8B | | |
| | | NC (Note 4) | | | AJ28 | | | |
| B8 | VREFB8N0 | IO | | | AK28 | | | |
| B8 | VREFB8N0 | IO | | | AR29 | | | |
| B8 | VREFB8N0 | IO | | | AR28 | | | |
| B8 | VREFB8N0 | IO | | | AL28 | | | |
| B8 | VREFB8N0 | IO | | | AM28 | | | |
| B8 | VREFB8N0 | IO | | | AN28 | | | |
| | | NC (Note 4) | | | AH27 | | | |
| B8 | VREFB8N1 | IO | DQ16B | | AT33 | DQ8B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQSn16B | | AU33 | DQSn8B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQ16B | | AT32 | DQ8B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQ16B | | AW33 | DQ8B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQ16B | | AV33 | DQ8B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQS16B | | AU32 | DQS8B | DQVLD3B | |
| B8 | VREFB8N0 | IO | | | AJ27 | | | |
| B8 | VREFB8N1 | IO | | | AK27 | | | |
| B8 | VREFB8N1 | IO | | | AR27 | | | |
| B8 | VREFB8N1 | VREFB8N1 | VREFB8N1 | | AP31 | | | |
| B8 | VREFB8N1 | IO | | | AG26 | | | |
| | | NC (Note 4) | | | AL27 | | | |
| B8 | VREFB8N1 | IO | | | AN27 | | | |
| B8 | VREFB8N1 | IO | | | AP27 | | | |
| B8 | VREFB8N1 | IO | | | AM27 | | | |
| B8 | VREFB8N1 | IO | DQ15B | | AV32 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQSn15B | | AV31 | DQ7B | DQSn3B | DQ1B |
| B8 | VREFB8N1 | IO | DQ15B | | AT31 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQ15B | | AU31 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQ15B | | AW32 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N1 | IO | DQS15B | | AW31 | DQVLD7B | DQS3B | |
| | | NC (Note 4) | | | AH26 | | | |
| B8 | VREFB8N1 | IO | | | AP26 | | | |
| B8 | VREFB8N1 | IO | | | AR26 | | | |
| B8 | VREFB8N1 | IO | | | AJ26 | | | |
| B8 | VREFB8N1 | IO | | | AL26 | | | |
| | | NC (Note 4) | | | AN26 | | | |
| B8 | VREFB8N1 | IO | | | AK26 | | | |
| B8 | VREFB8N1 | IO | | | AM26 | | | |
| B8 | VREFB8N2 | IO | DQ14B | | AT29 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N2 | IO | DQSn14B | | AU30 | DQSn7B | DQ3B | DQ1B |
| B8 | VREFB8N2 | IO | DQ14B | | AT30 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N2 | IO | DQ14B | | AW30 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N2 | IO | DQ14B | | AU29 | DQ7B | DQ3B | DQ1B |
| B8 | VREFB8N2 | IO | DQS14B | | AV30 | DQS7B | | |
| B8 | VREFB8N2 | IO | | | AG25 | | | |
| B8 | VREFB8N2 | IO | | | AH25 | | | |
| | | NC (Note 4) | | | AR25 | | | |
| B8 | VREFB8N2 | VREFB8N2 | VREFB8N2 | | AP28 | | | |
| B8 | VREFB8N2 | IO | | | AJ25 | | | |
| B8 | VREFB8N2 | IO | | | AL25 | | | |
| B8 | VREFB8N2 | IO | | | AN25 | | | |
| B8 | VREFB8N2 | IO | | | AK25 | | | |
| | | NC (Note 4) | | | AM25 | | | |
| B8 | VREFB8N2 | IO | DQ13B | | AV29 | DQ6B | | |
| B8 | VREFB8N2 | IO | DQSn13B | | AU28 | DQ6B | DQ2B | DQSn1B |
| B8 | VREFB8N2 | IO | DQ13B | | AT28 | DQ6B | DQ2B | DQ1B |
| B8 | VREFB8N2 | IO | DQ13B | | AW29 | DQ6B | DQ2B | DQ1B |
| B8 | VREFB8N2 | IO | DQ13B | | AW28 | DQ6B | DQ2B | DQ1B |
| B8 | VREFB8N2 | IO | DQS13B | | AV28 | DQVLD6B | | DQS1B |
| B8 | VREFB8N2 | IO | | | AG24 | | | |
| B8 | VREFB8N2 | IO | | | AH24 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | NC (Note 4) | | | AR24 | | | |
| B8 | VREFB8N2 | IO | | | AJ24 | | | |
| | | NC (Note 4) | | | AK24 | | | |
| B8 | VREFB8N2 | IO | | | AP24 | | | |
| B8 | VREFB8N2 | IO | | | AL24 | | | |
| B8 | VREFB8N2 | IO | | | AM24 | | | |
| B8 | VREFB8N3 | IO | DQ12B | | AU26 | DQ6B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQSn12B | | AU27 | DQSn6B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQ12B | | AT27 | DQ6B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQ12B | | AT26 | DQ6B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQ12B | | AW27 | DQ6B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQS12B | | AV27 | DQS6B | DQVLD2B | DQVLD1B |
| B8 | VREFB8N3 | IO | | | AG23 | | | |
| | | NC (Note 4) | | | AH23 | | | |
| B8 | VREFB8N3 | IO | | | AN24 | | | |
| B8 | VREFB8N3 | VREFB8N3 | VREFB8N3 | | AP25 | | | |
| B8 | VREFB8N3 | IO | | | AJ23 | | | |
| B8 | VREFB8N3 | IO | | | AG22 | | | |
| B8 | VREFB8N3 | IO | | | AP23 | | | |
| B8 | VREFB8N3 | IO | | | AK23 | | | |
| | | NC (Note 4) | | | AL23 | | | |
| B8 | VREFB8N3 | IO | DQ11B | | AT25 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQSn11B | | AU25 | DQ5B | DQSn2B | DQ1B |
| B8 | VREFB8N3 | IO | DQ11B | | AW26 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQ11B | | AW25 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQ11B | | AV26 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N3 | IO | DQS11B | | AV25 | DQVLD5B | DQS2B | |
| B8 | VREFB8N3 | IO | | | AH22 | | | |
| B8 | VREFB8N3 | IO | | | AM23 | | | |
| B8 | VREFB8N3 | IO | | | AN23 | | | |
| B8 | VREFB8N3 | IO | | | AJ22 | | | |
| | | NC (Note 4) | | | AN22 | | | |
| B8 | VREFB8N3 | IO | | | AM22 | | | |
| B8 | VREFB8N3 | IO | | | AG21 | | | |
| B8 | VREFB8N4 | IO | | | AH21 | | | |
| B8 | VREFB8N4 | IO | DQ10B | | AU24 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N4 | IO | DQSn10B | | AU23 | DQSn5B | DQ2B | DQ1B |
| B8 | VREFB8N4 | IO | DQ10B | | AT24 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N4 | IO | DQ10B | | AW23 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N4 | IO | DQ10B | | AV24 | DQ5B | DQ2B | DQ1B |
| B8 | VREFB8N4 | IO | DQS10B | | AV23 | DQS5B | | |
| B8 | VREFB8N4 | VREFB8N4 | VREFB8N4 | | AT23 | | | |
| B8 | VREFB8N4 | IO | | | AL22 | | | |
| | | NC (Note 4) | | | AM21 | | | |
| B8 | VREFB8N4 | IO | | | AP22 | | | |
| B8 | VREFB8N4 | IO | | RUnLU | AM20 | | | |
| B8 | VREFB8N4 | IO | DEV_OE | DEV_OE | AN20 | | | |
| B8 | VREFB8N4 | IO | DEV_CLRn | DEV_CLRn | AN21 | | | |
| B8 | VREFB8N4 | IO | | nCS | AP21 | | | |
| B12 | VREFB8N4 | IO | PLL12_FBn/OUT2n | | AR22 | | | |
| B12 | VREFB8N4 | IO | PLL12_FBp/OUT2p | | AT22 | | | |
| B8 | VREFB8N4 | IO | | | AP20 | | | |
| B12 | VREFB8N4 | IO | PLL12_OUT1n | | AU22 | | | |
| B12 | VREFB8N4 | IO | PLL12_OUT1p | | AV22 | | | |
| B12 | VREFB8N4 | IO | PLL12_OUT0n | | AV21 | | | |
| B12 | VREFB8N4 | IO | PLL12_OUT0p | | AW21 | | | |
| B8 | VREFB8N4 | IO | CLK5n | | AT21 | | | |
| B8 | VREFB8N4 | IO | CLK5p | | AU21 | | | |
| B8 | VREFB8N4 | IO | CLK4n | | AT20 | | | |
| B8 | VREFB8N4 | IO | CLK4p | | AU20 | | | |
| B12 | | VCC_PLL12_OUT | | | AK22 | | | |
| | | VCCD_PLL12 | | | AK20 | | | |
| | | VCCA_PLL12 | | | AL21 | | | |
| | | GNDA_PLL12 | | | AJ21 | | | |
| | | GNDA_PLL12 | | | AK21 | | | |
| | | GNDA_PLL6 | | | AJ19 | | | |
| | | GNDA_PLL6 | | | AK19 | | | |
| | | VCCA_PLL6 | | | AL19 | | | |
| | | VCCD_PLL6 | | | AJ20 | | | |
| B10 | | VCC_PLL6_OUT | | | AK18 | | | |
| B7 | VREFB7N0 | IO | CLK7p | | AU19 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B7 | VREFB7N0 | IO | CLK7n | | AT19 | | | |
| B7 | VREFB7N0 | IO | CLK6p | | AW20 | | | |
| B7 | VREFB7N0 | IO | CLK6n | | AV20 | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT1p | | AV18 | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT1n | | AU18 | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT0p | | AW19 | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT0n | | AV19 | | | |
| B10 | VREFB7N0 | IO | PLL6_FBp/OUT2p | | AT18 | | | |
| B10 | VREFB7N0 | IO | PLL6_FBn/OUT2n | | AR18 | | | |
| B7 | VREFB7N0 | IO | | | AM19 | | | |
| B7 | VREFB7N0 | IO | | | AN19 | | | |
| B7 | VREFB7N0 | VREFB7N0 | VREFB7N0 | | AP17 | | | |
| B7 | VREFB7N0 | IO | | | AM18 | | | |
| B7 | VREFB7N0 | IO | DQ9B | | AV17 | DQ4B | | |
| B7 | VREFB7N0 | IO | DQSn9B | | AT17 | DQ4B | DQ1B | DQ0B |
| B7 | VREFB7N0 | IO | DQ9B | | AP16 | DQ4B | DQ1B | |
| B7 | VREFB7N0 | IO | DQ9B | | AR16 | DQ4B | DQ1B | DQ0B |
| B7 | VREFB7N0 | IO | DQ9B | | AU17 | DQ4B | DQ1B | DQ0B |
| B7 | VREFB7N0 | IO | DQS9B | | AT16 | DQVLD4B | | |
| | | NC (Note 4) | | | AL18 | | | |
| B7 | VREFB7N0 | IO | | | AH20 | | | |
| B7 | VREFB7N0 | IO | | | AR20 | | | |
| B7 | VREFB7N0 | IO | | | AN18 | | | |
| B7 | VREFB7N1 | IO | | | AP19 | | | |
| B7 | VREFB7N0 | IO | DQ8B | | AW17 | DQ4B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQSn8B | | AV16 | DQSn4B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ8B | | AU15 | DQ4B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ8B | | AV15 | DQ4B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ8B | | AW15 | DQ4B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQS8B | | AU16 | DQS4B | DQVLD1B | |
| | | NC (Note 4) | | | AG20 | | | |
| B7 | VREFB7N1 | IO | | | AL17 | | | |
| B7 | VREFB7N1 | IO | | | AM17 | | | |
| B7 | VREFB7N1 | IO | | | AH19 | | | |
| | | NC (Note 4) | | | AJ18 | | | |
| B7 | VREFB7N1 | IO | DQ7B | | AW14 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQSn7B | | AU14 | DQ3B | DQSn1B | DQ0B |
| B7 | VREFB7N1 | VREFB7N1 | VREFB7N1 | | AP15 | | | |
| B7 | VREFB7N1 | IO | DQ7B | | AR15 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ7B | | AT15 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ7B | | AV14 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQS7B | | AT14 | DQVLD3B | DQS1B | |
| B7 | VREFB7N1 | IO | | | AK17 | | | |
| B7 | VREFB7N1 | IO | | | AN17 | | | |
| B7 | VREFB7N1 | IO | | | AP18 | | | |
| B7 | VREFB7N1 | IO | | | AG19 | | | |
| | | NC (Note 4) | | | AL16 | | | |
| B7 | VREFB7N1 | IO | DQ6B | | AW13 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQSn6B | | AV13 | DQSn3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ6B | | AP14 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ6B | | AR14 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQ6B | | AT13 | DQ3B | DQ1B | DQ0B |
| B7 | VREFB7N1 | IO | DQS6B | | AU13 | DQS3B | | |
| B7 | VREFB7N1 | IO | | | AH18 | | | |
| | | NC (Note 4) | | | AM16 | | | |
| B7 | VREFB7N1 | IO | | | AN16 | | | |
| B7 | VREFB7N2 | IO | | | AJ17 | | | |
| | | NC (Note 4) | | | AK16 | | | |
| B7 | VREFB7N2 | IO | DQ5B | | AU12 | DQ2B | | |
| B7 | VREFB7N2 | IO | DQSn5B | | AT12 | DQ2B | DQ0B | DQSn0B |
| B7 | VREFB7N2 | IO | DQ5B | | AP13 | DQ2B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQ5B | | AR13 | DQ2B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQ5B | | AV12 | DQ2B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQS5B | | AR12 | DQVLD2B | | DQS0B |
| B7 | VREFB7N2 | IO | | | AG18 | | | |
| B7 | VREFB7N2 | IO | | | AM15 | | | |
| B7 | VREFB7N2 | IO | | | AN15 | | | |
| B7 | VREFB7N2 | VREFB7N2 | VREFB7N2 | | AP12 | | | |
| | | NC (Note 4) | | | AJ16 | | | |
| B7 | VREFB7N2 | IO | DQ4B | | AW11 | DQ2B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQSn4B | | AV11 | DQSn2B | DQ0B | DQ0B |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B7 | VREFB7N2 | IO | DQ4B | | AT11 | DQ2B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQ4B | | AR11 | DQ2B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQ4B | | AW12 | DQ2B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQS4B | | AU11 | DQS2B | DQVLD0B | DQVLD0B |
| B7 | VREFB7N2 | IO | | | AH17 | | | |
| | | NC (Note 4) | | | AK15 | | | |
| B7 | VREFB7N2 | IO | | | AL15 | | | |
| B7 | VREFB7N2 | IO | | | AG17 | | | |
| | | NC (Note 4) | | | AL14 | | | |
| B7 | VREFB7N2 | IO | DQ3B | | AW10 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQSn3B | | AV10 | DQ1B | DQSn0B | DQ0B |
| B7 | VREFB7N3 | IO | DQ3B | | AR10 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQ3B | | AT10 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQ3B | | AW9 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQS3B | | AU10 | DQVLD1B | DQS0B | |
| B7 | VREFB7N2 | IO | | | AH16 | | | |
| B7 | VREFB7N2 | IO | | | AJ15 | | | |
| B7 | VREFB7N2 | IO | | | AM14 | | | |
| B7 | VREFB7N3 | IO | | | AK14 | | | |
| | | NC (Note 4) | | | AG16 | | | |
| B7 | VREFB7N3 | IO | DQ2B | | AW8 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQSn2B | | AV9 | DQSn1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQ2B | | AR9 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQ2B | | AT9 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQ2B | | AV8 | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N3 | IO | DQS2B | | AU9 | DQS1B | | |
| B7 | VREFB7N3 | VREFB7N3 | VREFB7N3 | | AP9 | | | |
| | | NC (Note 4) | | | AH15 | | | |
| B7 | VREFB7N3 | IO | | | AL13 | | | |
| B7 | VREFB7N3 | IO | | | AM13 | | | |
| | | NC (Note 4) | | | AK13 | | | |
| B7 | VREFB7N3 | IO | | | AJ14 | | | |
| B7 | VREFB7N3 | IO | | | AN14 | | | |
| B7 | VREFB7N3 | IO | | | AG15 | | | |
| B7 | VREFB7N3 | IO | | | AH14 | | | |
| B7 | VREFB7N3 | IO | DQ1B | | AW7 | DQ0B | | |
| B7 | VREFB7N3 | IO | DQSn1B | | AV7 | DQ0B | | |
| B7 | VREFB7N3 | IO | DQ1B | | AT8 | DQ0B | | |
| B7 | VREFB7N3 | IO | DQ1B | | AT7 | DQ0B | | |
| B7 | VREFB7N3 | IO | DQ1B | | AU8 | DQ0B | | |
| B7 | VREFB7N3 | IO | DQS1B | | AU7 | DQVLD0B | | |
| | | NC (Note 4) | | | AJ13 | | | |
| B7 | VREFB7N3 | IO | | | AM12 | | | |
| B7 | VREFB7N4 | IO | | | AN13 | | | |
| B7 | VREFB7N4 | IO | | | AG14 | | | |
| B7 | VREFB7N4 | IO | | | AL12 | | | |
| B7 | VREFB7N4 | IO | DQ0B | | AW6 | DQ0B | | |
| B7 | VREFB7N4 | IO | DQSn0B | | AV6 | DQSn0B | | |
| B7 | VREFB7N4 | IO | DQ0B | | AU5 | DQ0B | | |
| B7 | VREFB7N4 | IO | DQ0B | | AU6 | DQ0B | | |
| B7 | VREFB7N4 | IO | DQ0B | | AW5 | DQ0B | | |
| B7 | VREFB7N4 | IO | DQS0B | | AV5 | DQS0B | | |
| | | NC (Note 4) | | | AK12 | | | |
| B7 | VREFB7N4 | IO | | | AN12 | | | |
| B7 | VREFB7N4 | IO | | | AN11 | | | |
| B7 | VREFB7N4 | VREFB7N4 | VREFB7N4 | | AR7 | | | |
| B7 | VREFB7N4 | IO | | | AH13 | | | |
| | | NC (Note 4) | | | AM11 | | | |
| B7 | VREFB7N4 | IO | | | AP11 | | | |
| B7 | VREFB7N4 | IO | RDN7 | | AL11 | | | |
| B7 | VREFB7N4 | IO | RUP7 | | AN9 | | | |
| B7 | VREFB7N4 | IO | | | AP10 | | | |
| B7 | VREFB7N4 | IO | | | AJ12 | | | |
| B7 | VREFB7N4 | IO | | | AP8 | | | |
| B7 | VREFB7N4 | IO | | | AR8 | | | |
| B7 | VREFB7N4 | PORSEL | | PORSEL | AP7 | | | |
| B7 | VREFB7N4 | nIO_PULLUP | | nIO_PULLUP | AT5 | | | |
| B7 | VREFB7N4 | PLL_ENA | | PLL_ENA | AV4 | | | |
| | | GND | | | AW3 | | | |
| B7 | VREFB7N4 | nCEO | | nCEO | AT6 | | | |
| | | VCCD_PLL9 | | | AK11 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | VCCA_PLL9 | | | AJ11 | | | |
| | | GNDA_PLL9 | | | AK10 | | | |
| | | GNDA_PLL9 | | | AL10 | | | |
| B6 | | FPLL9CLKp | INPUT | | AU1 | | | |
| B6 | | FPLL9CLKn | INPUT | | AU2 | | | |
| | | NC (Note 4) | | | AM9 | | | |
| | | NC (Note 4) | | | AM8 | | | |
| | | NC (Note 4) | | | AL9 | | | |
| | | NC (Note 4) | | | AL8 | | | |
| | | NC (Note 4) | | | AP6 | | | |
| | | NC (Note 4) | | | AP5 | | | |
| | | NC (Note 4) | | | AK9 | | | |
| | | NC (Note 4) | | | AK8 | | | |
| | | NC (Note 4) | | | AT4 | | | |
| | | NC (Note 4) | | | AT3 | | | |
| | | NC (Note 3) | | | AT2 | | | |
| | | NC (Note 4) | | | AN7 | | | |
| | | NC (Note 4) | | | AN6 | | | |
| | | NC (Note 4) | | | AR4 | | | |
| | | NC (Note 4) | | | AR3 | | | |
| | | NC (Note 4) | | | AR6 | | | |
| | | NC (Note 4) | | | AR5 | | | |
| | | NC (Note 4) | | | AU4 | | | |
| | | NC (Note 4) | | | AU3 | | | |
| | | NC (Note 4) | | | AJ10 | | | |
| | | NC (Note 4) | | | AJ9 | | | |
| | | NC (Note 4) | | | AM6 | | | |
| | | NC (Note 4) | | | AM5 | | | |
| | | NC (Note 4) | | | AJ8 | | | |
| | | NC (Note 4) | | | AJ7 | | | |
| | | NC (Note 4) | | | AP4 | | | |
| | | NC (Note 4) | | | AP3 | | | |
| | | NC (Note 4) | | | AH8 | | | |
| | | NC (Note 4) | | | AH7 | | | |
| | | NC (Note 4) | | | AV3 | | | |
| | | NC (Note 4) | | | AV2 | | | |
| | | NC (Note 4) | | | AH10 | | | |
| | | NC (Note 4) | | | AH9 | | | |
| | | NC (Note 4) | | | AL6 | | | |
| | | NC (Note 4) | | | AL5 | | | |
| | | NC (Note 4) | | | AH12 | | | |
| | | NC (Note 4) | | | AH11 | | | |
| | | NC (Note 4) | | | AN4 | | | |
| | | NC (Note 4) | | | AN3 | | | |
| | | NC (Note 4) | | | AG13 | | | |
| | | NC (Note 4) | | | AG12 | | | |
| | | NC (Note 4) | | | AK6 | | | |
| | | NC (Note 4) | | | AK5 | | | |
| | | NC (Note 4) | | | AF13 | | | |
| | | NC (Note 4) | | | AF12 | | | |
| | | NC (Note 4) | | | AM4 | | | |
| | | NC (Note 4) | | | AM3 | | | |
| | | NC (Note 3) | | | AN5 | | | |
| B6 | | IO | DIFFIO_TX159n | | AG11 | | | |
| B6 | | IO | DIFFIO_TX159p | | AG10 | | | |
| | | NC (Note 4) | | | AR2 | | | |
| | | NC (Note 4) | | | AR1 | | | |
| B6 | | IO | DIFFIO_TX158n | | AG9 | | | |
| B6 | | IO | DIFFIO_TX158p | | AG8 | | | |
| B6 | | IO | DIFFIO_RX158n | | AJ6 | | | |
| B6 | | IO | DIFFIO_RX158p | | AJ5 | | | |
| B6 | | IO | DIFFIO_TX157n | | AE14 | | | |
| B6 | | IO | DIFFIO_TX157p | | AE13 | | | |
| B6 | | IO | DIFFIO_RX157n | | AP2 | | | |
| B6 | | IO | DIFFIO_RX157p | | AP1 | | | |
| B6 | | IO | DIFFIO_TX156n | | AD14 | | | |
| B6 | | IO | DIFFIO_TX156p | | AD13 | | | |
| B6 | | IO | DIFFIO_RX156n | | AN2 | | | |
| B6 | | IO | DIFFIO_RX156p | | AN1 | | | |
| B6 | | IO | DIFFIO_TX155n | | AF11 | | | |
| B6 | | IO | DIFFIO_TX155p | | AF10 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B6 | | IO | DIFFIO_RX155n | | AG7 | | | |
| B6 | | IO | DIFFIO_RX155p | | AG6 | | | |
| B6 | | IO | DIFFIO_TX154n | | AE12 | | | |
| B6 | | IO | DIFFIO_TX154p | | AE11 | | | |
| B6 | | IO | DIFFIO_RX154n | | AH6 | | | |
| B6 | | IO | DIFFIO_RX154p | | AH5 | | | |
| B6 | | IO | DIFFIO_TX153n | | AF6 | | | |
| B6 | | IO | DIFFIO_TX153p | | AF5 | | | |
| B6 | | IO | DIFFIO_RX153n | | AK4 | | | |
| B6 | | IO | DIFFIO_RX153p | | AK3 | | | |
| B6 | | IO | DIFFIO_TX152n | | AF8 | | | |
| B6 | | IO | DIFFIO_TX152p | | AF7 | | | |
| B6 | | IO | DIFFIO_RX152n | | AL4 | | | |
| B6 | | IO | DIFFIO_RX152p | | AL3 | | | |
| B6 | | IO | DIFFIO_TX151n | | AE6 | | | |
| B6 | | IO | DIFFIO_TX151p | | AE5 | | | |
| B6 | | IO | DIFFIO_RX151n | | AJ4 | | | |
| B6 | | IO | DIFFIO_RX151p | | AJ3 | | | |
| | | NC (Note 3) | | | AL7 | | | |
| B6 | | IO | DIFFIO_TX150n | | AE8 | | | |
| B6 | | IO | DIFFIO_TX150p | | AE7 | | | |
| B6 | | IO | DIFFIO_RX150n | | AM2 | | | |
| B6 | | IO | DIFFIO_RX150p | | AM1 | | | |
| B6 | | IO | DIFFIO_TX149n | | AE10 | | | |
| B6 | | IO | DIFFIO_TX149p | | AE9 | | | |
| B6 | | IO | DIFFIO_RX149n | | AH4 | | | |
| B6 | | IO | DIFFIO_RX149p | | AH3 | | | |
| B6 | | IO | DIFFIO_TX148n | | AD7 | | | |
| B6 | | IO | DIFFIO_TX148p | | AD6 | | | |
| B6 | | IO | DIFFIO_RX148n | | AL2 | | | |
| B6 | | IO | DIFFIO_RX148p | | AL1 | | | |
| B6 | | IO | DIFFIO_TX147n | | AD12 | | | |
| B6 | | IO | DIFFIO_TX147p | | AD11 | | | |
| B6 | | IO | DIFFIO_RX147n | | AG4 | | | |
| B6 | | IO | DIFFIO_RX147p | | AG3 | | | |
| B6 | | IO | DIFFIO_TX146n | | AD9 | | | |
| B6 | | IO | DIFFIO_TX146p | | AD8 | | | |
| B6 | | IO | DIFFIO_RX146n | | AK2 | | | |
| B6 | | IO | DIFFIO_RX146p | | AK1 | | | |
| B6 | | IO | DIFFIO_TX145n | | AC7 | | | |
| B6 | | IO | DIFFIO_TX145p | | AC6 | | | |
| B6 | | IO | DIFFIO_RX145n | | AJ2 | | | |
| B6 | | IO | DIFFIO_RX145p | | AJ1 | | | |
| B6 | | IO | DIFFIO_TX144n | | AC13 | | | |
| B6 | | IO | DIFFIO_TX144p | | AC12 | | | |
| B6 | | IO | DIFFIO_RX144n | | AF4 | | | |
| B6 | | IO | DIFFIO_RX144p | | AF3 | | | |
| B6 | | IO | DIFFIO_TX143n | | AC9 | | | |
| B6 | | IO | DIFFIO_TX143p | | AC8 | | | |
| B6 | | IO | DIFFIO_RX143n | | AH2 | | | |
| B6 | | IO | DIFFIO_RX143p | | AH1 | | | |
| B6 | | IO | DIFFIO_TX142n | | AC11 | | | |
| B6 | | IO | DIFFIO_TX142p | | AC10 | | | |
| B6 | | IO | DIFFIO_RX142n | | AG2 | | | |
| B6 | | IO | DIFFIO_RX142p | | AG1 | | | |
| | | NC (Note 3) | | | AG5 | | | |
| B6 | | IO | DIFFIO_TX141n | | AB13 | | | |
| B6 | | IO | DIFFIO_TX141p | | AB12 | | | |
| B6 | | IO | DIFFIO_RX141n | | AF2 | | | |
| B6 | | IO | DIFFIO_RX141p | | AF1 | | | |
| B6 | | IO | DIFFIO_TX140n | | AB7 | | | |
| B6 | | IO | DIFFIO_TX140p | | AB6 | | | |
| B6 | | IO | DIFFIO_RX140n | | AD5 | | | |
| B6 | | IO | DIFFIO_RX140p | | AD4 | | | |
| B6 | | IO | DIFFIO_TX139n | | AB9 | | | |
| B6 | | IO | DIFFIO_TX139p | | AB8 | | | |
| B6 | | IO | DIFFIO_RX139n | | AE4 | | | |
| B6 | | IO | DIFFIO_RX139p | | AE3 | | | |
| B6 | | IO | DIFFIO_TX138n | | AA8 | | | |
| B6 | | IO | DIFFIO_TX138p | | AA7 | | | |
| B6 | | IO | DIFFIO_RX138n | | AC4 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B6 | | IO | DIFFIO_RX138p | | AC3 | | | |
| B6 | | IO | DIFFIO_TX137n | | AB11 | | | |
| B6 | | IO | DIFFIO_TX137p | | AB10 | | | |
| B6 | | IO | DIFFIO_RX137n | | AD3 | | | |
| B6 | | IO | DIFFIO_RX137p | | AD2 | | | |
| B6 | | IO | DIFFIO_TX136n | | AA14 | | | |
| B6 | | IO | DIFFIO_TX136p | | AA13 | | | |
| B6 | | IO | DIFFIO_RX136n | | AE2 | | | |
| B6 | | IO | DIFFIO_RX136p | | AE1 | | | |
| B6 | | IO | DIFFIO_TX135n | | Y6 | | | |
| B6 | | IO | DIFFIO_TX135p | | Y5 | | | |
| B6 | | IO | DIFFIO_RX135n | | AB5 | | | |
| B6 | | IO | DIFFIO_RX135p | | AB4 | | | |
| B6 | | IO | DIFFIO_TX134n | | Y8 | | | |
| B6 | | IO | DIFFIO_TX134p | | Y7 | | | |
| B6 | | IO | DIFFIO_RX134n | | AC2 | | | |
| B6 | | IO | DIFFIO_RX134p | | AC1 | | | |
| | | NC (Note 3) | | | AA6 | | | |
| B6 | | IO | DIFFIO_TX133n | | AA10 | | | |
| B6 | | IO | DIFFIO_TX133p | | AA9 | | | |
| B6 | | IO | DIFFIO_RX133n | | AB3 | | | |
| B6 | | IO | DIFFIO_RX133p | | AB2 | | | |
| B6 | | IO | DIFFIO_TX132n | | AA12 | | | |
| B6 | | IO | DIFFIO_TX132p | | AA11 | | | |
| B6 | | IO | DIFFIO_RX132n | | AA4 | | | |
| B6 | | IO | DIFFIO_RX132p | | AA3 | | | |
| B6 | | IO | DIFFIO_TX131n | | Y14 | | | |
| B6 | | IO | DIFFIO_TX131p | | Y13 | | | |
| B6 | | IO | DIFFIO_RX131n | | AA2 | | | |
| B6 | | IO | DIFFIO_RX131p | | AA1 | | | |
| B6 | | CLK9n | INPUT | | Y4 | | | |
| B6 | | CLK9p | INPUT | | Y3 | | | |
| B6 | | IO | CLK8n/DIFFIO_RX_C2n | | Y2 | | | |
| B6 | | IO | CLK8p/DIFFIO_RX_C2p | | Y1 | | | |
| | | VCCD_PLL3 | | | Y10 | | | |
| | | VCCA_PLL3 | | | W11 | | | |
| | | GNDA_PLL3 | | | Y11 | | | |
| | | GNDA_PLL3 | | | Y12 | | | |
| | | GNDA_PLL4 | | | V10 | | | |
| | | GNDA_PLL4 | | | V11 | | | |
| | | VCCA_PLL4 | | | W9 | | | |
| | | VCCD_PLL4 | | | W10 | | | |
| B5 | | CLK11p | INPUT | | W3 | | | |
| B5 | | CLK11n | INPUT | | W4 | | | |
| B5 | | IO | CLK10p/DIFFIO_RX_C3p | | W1 | | | |
| B5 | | IO | CLK10n/DIFFIO_RX_C3n | | W2 | | | |
| B5 | | IO | DIFFIO_TX130n | | W8 | | | |
| B5 | | IO | DIFFIO_TX130p | | W7 | | | |
| B5 | | IO | DIFFIO_RX130n | | U2 | | | |
| B5 | | IO | DIFFIO_RX130p | | U1 | | | |
| B5 | | IO | DIFFIO_TX129n | | W13 | | | |
| B5 | | IO | DIFFIO_TX129p | | W12 | | | |
| B5 | | IO | DIFFIO_RX129n | | V3 | | | |
| B5 | | IO | DIFFIO_RX129p | | V2 | | | |
| B5 | | IO | DIFFIO_TX128n | | V7 | | | |
| B5 | | IO | DIFFIO_TX128p | | V6 | | | |
| B5 | | IO | DIFFIO_RX128n | | R2 | | | |
| B5 | | IO | DIFFIO_RX128p | | R1 | | | |
| B5 | | IO | DIFFIO_TX127n | | V9 | | | |
| B5 | | IO | DIFFIO_TX127p | | V8 | | | |
| B5 | | IO | DIFFIO_RX127n | | T3 | | | |
| B5 | | IO | DIFFIO_RX127p | | T2 | | | |
| | | NC (Note 3) | | | W6 | | | |
| B5 | | IO | DIFFIO_TX126n | | V13 | | | |
| B5 | | IO | DIFFIO_TX126p | | V12 | | | |
| B5 | | IO | DIFFIO_RX126n | | V5 | | | |
| B5 | | IO | DIFFIO_RX126p | | V4 | | | |
| B5 | | IO | DIFFIO_TX125n | | U13 | | | |
| B5 | | IO | DIFFIO_TX125p | | U12 | | | |
| B5 | | IO | DIFFIO_RX125n | | U4 | | | |
| B5 | | IO | DIFFIO_RX125p | | U3 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B5 | | IO | DIFFIO_TX124n | | U11 | | | |
| B5 | | IO | DIFFIO_TX124p | | U10 | | | |
| B5 | | IO | DIFFIO_RX124n | | P2 | | | |
| B5 | | IO | DIFFIO_RX124p | | P1 | | | |
| B5 | | IO | DIFFIO_TX123n | | U7 | | | |
| B5 | | IO | DIFFIO_TX123p | | U6 | | | |
| B5 | | IO | DIFFIO_RX123n | | P4 | | | |
| B5 | | IO | DIFFIO_RX123p | | P3 | | | |
| B5 | | IO | DIFFIO_TX122n | | U9 | | | |
| B5 | | IO | DIFFIO_TX122p | | U8 | | | |
| B5 | | IO | DIFFIO_RX122n | | R4 | | | |
| B5 | | IO | DIFFIO_RX122p | | R3 | | | |
| B5 | | IO | DIFFIO_TX121n | | T7 | | | |
| B5 | | IO | DIFFIO_TX121p | | T6 | | | |
| B5 | | IO | DIFFIO_RX121n | | T5 | | | |
| B5 | | IO | DIFFIO_RX121p | | T4 | | | |
| B5 | | IO | DIFFIO_TX120n | | T13 | | | |
| B5 | | IO | DIFFIO_TX120p | | T12 | | | |
| B5 | | IO | DIFFIO_RX120n | | N2 | | | |
| B5 | | IO | DIFFIO_RX120p | | N1 | | | |
| B5 | | IO | DIFFIO_TX119n | | T11 | | | |
| B5 | | IO | DIFFIO_TX119p | | T10 | | | |
| B5 | | IO | DIFFIO_RX119n | | M2 | | | |
| B5 | | IO | DIFFIO_RX119p | | M1 | | | |
| B5 | | IO | DIFFIO_TX118n | | T9 | | | |
| B5 | | IO | DIFFIO_TX118p | | T8 | | | |
| B5 | | IO | DIFFIO_RX118n | | L2 | | | |
| B5 | | IO | DIFFIO_RX118p | | L1 | | | |
| | | NC (Note 3) | | | R5 | | | |
| B5 | | IO | DIFFIO_TX117n | | R7 | | | |
| B5 | | IO | DIFFIO_TX117p | | R6 | | | |
| B5 | | IO | DIFFIO_RX117n | | K2 | | | |
| B5 | | IO | DIFFIO_RX117p | | K1 | | | |
| B5 | | IO | DIFFIO_TX116n | | P6 | | | |
| B5 | | IO | DIFFIO_TX116p | | P5 | | | |
| B5 | | IO | DIFFIO_RX116n | | N4 | | | |
| B5 | | IO | DIFFIO_RX116p | | N3 | | | |
| B5 | | IO | DIFFIO_TX115n | | R13 | | | |
| B5 | | IO | DIFFIO_TX115p | | R12 | | | |
| B5 | | IO | DIFFIO_RX115n | | J2 | | | |
| B5 | | IO | DIFFIO_RX115p | | J1 | | | |
| B5 | | IO | DIFFIO_TX114n | | R11 | | | |
| B5 | | IO | DIFFIO_TX114p | | R10 | | | |
| B5 | | IO | DIFFIO_RX114n | | H2 | | | |
| B5 | | IO | DIFFIO_RX114p | | H1 | | | |
| B5 | | IO | DIFFIO_TX113n | | R9 | | | |
| B5 | | IO | DIFFIO_TX113p | | R8 | | | |
| B5 | | IO | DIFFIO_RX113n | | M4 | | | |
| B5 | | IO | DIFFIO_RX113p | | M3 | | | |
| B5 | | IO | DIFFIO_TX112n | | N6 | | | |
| B5 | | IO | DIFFIO_TX112p | | N5 | | | |
| B5 | | IO | DIFFIO_RX112n | | K4 | | | |
| B5 | | IO | DIFFIO_RX112p | | K3 | | | |
| B5 | | IO | DIFFIO_TX111n | | P8 | | | |
| B5 | | IO | DIFFIO_TX111p | | P7 | | | |
| B5 | | IO | DIFFIO_RX111n | | L4 | | | |
| B5 | | IO | DIFFIO_RX111p | | L3 | | | |
| B5 | | IO | DIFFIO_TX110n | | P10 | | | |
| B5 | | IO | DIFFIO_TX110p | | P9 | | | |
| B5 | | IO | DIFFIO_RX110n | | G4 | | | |
| B5 | | IO | DIFFIO_RX110p | | G3 | | | |
| B5 | | IO | DIFFIO_TX109n | | M6 | | | |
| B5 | | IO | DIFFIO_TX109p | | M5 | | | |
| B5 | | IO | DIFFIO_RX109n | | H4 | | | |
| B5 | | IO | DIFFIO_RX109p | | H3 | | | |
| | | NC (Note 3) | | | J5 | | | |
| B5 | | IO | DIFFIO_TX108n | | N8 | | | |
| B5 | | IO | DIFFIO_TX108p | | N7 | | | |
| B5 | | IO | DIFFIO_RX108n | | J4 | | | |
| B5 | | IO | DIFFIO_RX108p | | J3 | | | |
| B5 | | IO | DIFFIO_TX107n | | P12 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B5 | | IO | DIFFIO_TX107p | | P11 | | | |
| B5 | | IO | DIFFIO_RX107n | | G2 | | | |
| B5 | | IO | DIFFIO_RX107p | | G1 | | | |
| B5 | | IO | DIFFIO_TX106n | | P14 | | | |
| B5 | | IO | DIFFIO_TX106p | | P13 | | | |
| B5 | | IO | DIFFIO_RX106n | | L6 | | | |
| B5 | | IO | DIFFIO_RX106p | | L5 | | | |
| B5 | | IO | DIFFIO_TX105n | | N12 | | | |
| B5 | | IO | DIFFIO_TX105p | | N11 | | | |
| B5 | | IO | DIFFIO_RX105n | | F2 | | | |
| B5 | | IO | DIFFIO_RX105p | | F1 | | | |
| B5 | | IO | DIFFIO_TX104n | | N10 | | | |
| B5 | | IO | DIFFIO_TX104p | | N9 | | | |
| B5 | | IO | DIFFIO_RX104n | | E2 | | | |
| B5 | | IO | DIFFIO_RX104p | | E1 | | | |
| B5 | | IO | DIFFIO_TX103n | | M8 | | | |
| B5 | | IO | DIFFIO_TX103p | | M7 | | | |
| B5 | | IO | DIFFIO_RX103n | | K6 | | | |
| B5 | | IO | DIFFIO_RX103p | | K5 | | | |
| B5 | | IO | DIFFIO_TX102n | | M12 | | | |
| B5 | | IO | DIFFIO_TX102p | | M11 | | | |
| | | NC (Note 4) | | | F4 | | | |
| | | NC (Note 4) | | | F3 | | | |
| | | NC (Note 4) | | | E6 | | | |
| | | NC (Note 4) | | | E5 | | | |
| | | NC (Note 4) | | | E4 | | | |
| | | NC (Note 4) | | | E3 | | | |
| | | NC (Note 4) | | | M10 | | | |
| | | NC (Note 4) | | | M9 | | | |
| | | NC (Note 4) | | | H6 | | | |
| | | NC (Note 4) | | | H5 | | | |
| | | NC (Note 3) | | | G7 | | | |
| | | NC (Note 4) | | | L8 | | | |
| | | NC (Note 4) | | | L7 | | | |
| | | NC (Note 4) | | | G6 | | | |
| | | NC (Note 4) | | | G5 | | | |
| | | NC (Note 4) | | | F6 | | | |
| | | NC (Note 4) | | | F5 | | | |
| | | NC (Note 4) | | | J7 | | | |
| | | NC (Note 4) | | | J6 | | | |
| | | NC (Note 4) | | | H9 | | | |
| | | NC (Note 4) | | | H8 | | | |
| | | NC (Note 4) | | | B3 | | | |
| | | NC (Note 4) | | | B2 | | | |
| | | NC (Note 4) | | | K9 | | | |
| | | NC (Note 4) | | | K8 | | | |
| | | NC (Note 4) | | | D4 | | | |
| | | NC (Note 4) | | | D3 | | | |
| | | NC (Note 4) | | | L10 | | | |
| | | NC (Note 4) | | | L9 | | | |
| | | NC (Note 4) | | | C4 | | | |
| | | NC (Note 4) | | | C3 | | | |
| | | NC (Note 4) | | | J9 | | | |
| | | NC (Note 4) | | | J8 | | | |
| | | NC (Note 3) | | | D2 | | | |
| B5 | | FPLL10CLKn | INPUT | | C2 | | | |
| B5 | | FPLL10CLKp | INPUT | | C1 | | | |
| | | GNDA_PLL10 | | | K10 | | | |
| | | GNDA_PLL10 | | | K11 | | | |
| | | VCCA_PLL10 | | | L11 | | | |
| | | VCCD_PLL10 | | | L12 | | | |
| | | TEMPDIODEp | | | B4 | | | |
| | | TEMPDIODEn | | | F7 | | | |
| B4 | VREFB4N0 | TDO | | TDO | F8 | | | |
| | | NC (Note 2) | | MSEL3 | A3 | | | |
| | | NC (Note 2) | | MSEL2 | E7 | | | |
| | | NC (Note 2) | | MSEL1 | G9 | | | |
| | | NC (Note 2) | | MSEL0 | H10 | | | |
| B4 | VREFB4N0 | IO | RUP4 | | E8 | | | |
| B4 | VREFB4N0 | IO | RDN4 | | J11 | | | |
| B4 | VREFB4N0 | IO | | | E9 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | NC (Note 4) | | | N13 | | | |
| B4 | VREFB4N0 | IO | | | F10 | | | |
| B4 | VREFB4N0 | IO | | | M13 | | | |
| | | NC (Note 4) | | | N14 | | | |
| B4 | VREFB4N0 | IO | | | F11 | | | |
| B4 | VREFB4N0 | IO | | | H11 | | | |
| B4 | VREFB4N0 | IO | | | P15 | | | |
| B4 | VREFB4N0 | VREFB4N0 | VREFB4N0 | | D5 | | | |
| B4 | VREFB4N0 | IO | | | G11 | | | |
| B4 | VREFB4N0 | IO | | | H12 | | | |
| | | NC (Note 4) | | | K12 | | | |
| B4 | VREFB4N0 | IO | DQS0T | | C6 | DQS0T | | |
| B4 | VREFB4N0 | IO | DQ0T | | B5 | DQ0T | | |
| B4 | VREFB4N0 | IO | DQ0T | | C5 | DQ0T | | |
| B4 | VREFB4N0 | IO | DQ0T | | D6 | DQ0T | | |
| B4 | VREFB4N0 | IO | DQSn0T | | B6 | DQSn0T | | |
| B4 | VREFB4N0 | IO | DQ0T | | A5 | DQ0T | | |
| B4 | VREFB4N0 | IO | | | N15 | | | |
| B4 | VREFB4N0 | IO | | | L13 | | | |
| B4 | VREFB4N0 | IO | | | G12 | | | |
| B4 | VREFB4N0 | IO | | | K13 | | | |
| | | NC (Note 4) | | | M14 | | | |
| B4 | VREFB4N0 | IO | DQS1T | | C7 | DQVLD0T | | |
| B4 | VREFB4N0 | IO | DQ1T | | A6 | DQ0T | | |
| B4 | VREFB4N0 | IO | DQ1T | | D7 | DQ0T | | |
| B4 | VREFB4N0 | IO | DQ1T | | D8 | DQ0T | | |
| B4 | VREFB4N1 | IO | DQSn1T | | B7 | DQ0T | | |
| B4 | VREFB4N1 | IO | DQ1T | | A7 | DQ0T | | |
| B4 | VREFB4N1 | IO | | | J12 | | | |
| B4 | VREFB4N1 | IO | | | L14 | | | |
| B4 | VREFB4N1 | IO | | | G13 | | | |
| B4 | VREFB4N1 | IO | | | H13 | | | |
| B4 | VREFB4N1 | IO | | | M15 | | | |
| | | NC (Note 4) | | | G14 | | | |
| B4 | VREFB4N1 | IO | | | H14 | | | |
| B4 | VREFB4N1 | IO | | | N16 | | | |
| B4 | VREFB4N1 | VREFB4N1 | VREFB4N1 | | F9 | | | |
| B4 | VREFB4N1 | IO | DQS2T | | B8 | DQS1T | | |
| B4 | VREFB4N1 | IO | DQ2T | | A8 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ2T | | C9 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ2T | | C8 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQSn2T | | B9 | DQSn1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ2T | | A9 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | | | J13 | | | |
| B4 | VREFB4N1 | IO | | | L15 | | | |
| | | NC (Note 4) | | | G15 | | | |
| B4 | VREFB4N1 | IO | | | K14 | | | |
| B4 | VREFB4N2 | IO | | | M16 | | | |
| B4 | VREFB4N1 | IO | DQS3T | | C10 | DQVLD1T | DQS0T | |
| B4 | VREFB4N1 | IO | DQ3T | | D10 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ3T | | E10 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ3T | | D9 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQSn3T | | B10 | DQ1T | DQSn0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ3T | | A10 | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | | | H15 | | | |
| | | NC (Note 4) | | | N17 | | | |
| B4 | VREFB4N2 | IO | | | M17 | | | |
| B4 | VREFB4N2 | IO | | | K15 | | | |
| B4 | VREFB4N2 | IO | | | J14 | | | |
| B4 | VREFB4N2 | IO | DQS4T | | C11 | DQS2T | DQVLD0T | DQVLD0T |
| B4 | VREFB4N2 | IO | DQ4T | | A11 | DQ2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ4T | | E11 | DQ2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ4T | | D11 | DQ2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQSn4T | | B11 | DQSn2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ4T | | E12 | DQ2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | | | L16 | | | |
| B4 | VREFB4N2 | VREFB4N2 | VREFB4N2 | | F12 | | | |
| | | NC (Note 4) | | | G17 | | | |
| B4 | VREFB4N2 | IO | | | G16 | | | |
| B4 | VREFB4N2 | IO | | | J15 | | | |
| B4 | VREFB4N2 | IO | | | N18 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B4 | VREFB4N2 | IO | DQS5T | | B12 | DQVLD2T | | DQS0T |
| B4 | VREFB4N2 | IO | DQ5T | | A12 | DQ2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ5T | | C12 | DQ2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ5T | | D12 | DQ2T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQSn5T | | B13 | DQ2T | DQ0T | DQSn0T |
| B4 | VREFB4N2 | IO | DQ5T | | A13 | DQ2T | | |
| B4 | VREFB4N2 | IO | | | K16 | | | |
| | | NC (Note 4) | | | G18 | | | |
| B4 | VREFB4N2 | IO | | | H16 | | | |
| B4 | VREFB4N2 | IO | | | M18 | | | |
| B4 | VREFB4N3 | IO | | | L17 | | | |
| B4 | VREFB4N3 | IO | DQS6T | | E13 | DQS3T | | |
| B4 | VREFB4N3 | IO | DQ6T | | F14 | DQ3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ6T | | E14 | DQ3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ6T | | F13 | DQ3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQSn6T | | D13 | DQSn3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ6T | | C13 | DQ3T | DQ1T | DQ0T |
| | | NC (Note 4) | | | J16 | | | |
| B4 | VREFB4N3 | IO | | | F18 | | | |
| B4 | VREFB4N3 | IO | | | H17 | | | |
| B4 | VREFB4N3 | IO | | | K17 | | | |
| B4 | VREFB4N3 | IO | DQS7T | | B14 | DQVLD3T | DQS1T | |
| B4 | VREFB4N3 | IO | DQ7T | | A14 | DQ3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ7T | | C14 | DQ3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ7T | | D14 | DQ3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | VREFB4N3 | VREFB4N3 | | F15 | | | |
| B4 | VREFB4N3 | IO | DQSn7T | | B15 | DQ3T | DQSn1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ7T | | A15 | DQ3T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | | | N19 | | | |
| | | NC (Note 4) | | | L18 | | | |
| B4 | VREFB4N3 | IO | | | G19 | | | |
| B4 | VREFB4N3 | IO | | | H18 | | | |
| B4 | VREFB4N3 | IO | | | J17 | | | |
| B4 | VREFB4N3 | IO | DQS8T | | E15 | DQS4T | DQVLD1T | |
| B4 | VREFB4N3 | IO | DQ8T | | C15 | DQ4T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ8T | | F16 | DQ4T | DQ1T | DQ0T |
| B4 | VREFB4N3 | IO | DQ8T | | D15 | DQ4T | DQ1T | DQ0T |
| B4 | VREFB4N4 | IO | DQSn8T | | E16 | DQSn4T | DQ1T | DQ0T |
| B4 | VREFB4N4 | IO | DQ8T | | D16 | DQ4T | DQ1T | DQ0T |
| | | NC (Note 4) | | | H19 | | | |
| B4 | VREFB4N4 | IO | | | P20 | | | |
| B4 | VREFB4N4 | IO | | | F19 | | | |
| B4 | VREFB4N4 | IO | | | M19 | | | |
| B4 | VREFB4N4 | IO | | | N20 | | | |
| B4 | VREFB4N4 | IO | DQS9T | | B16 | DQVLD4T | | |
| B4 | VREFB4N4 | IO | DQ9T | | C17 | DQ4T | DQ1T | DQ0T |
| B4 | VREFB4N4 | IO | DQ9T | | D17 | DQ4T | DQ1T | DQ0T |
| B4 | VREFB4N4 | IO | DQ9T | | C16 | DQ4T | DQ1T | |
| B4 | VREFB4N4 | VREFB4N4 | VREFB4N4 | | F17 | | | |
| B4 | VREFB4N4 | IO | DQSn9T | | B17 | DQ4T | DQ1T | DQ0T |
| B4 | VREFB4N4 | IO | DQ9T | | A17 | DQ4T | | |
| | | NC (Note 4) | | | H20 | | | |
| B4 | VREFB4N4 | IO | | | J18 | | | |
| B4 | VREFB4N4 | IO | | | G20 | | | |
| B9 | VREFB4N4 | IO | PLL5_FBn/OUT2n | | E18 | | | |
| B9 | VREFB4N4 | IO | PLL5_FBp/OUT2p | | D18 | | | |
| B9 | VREFB4N4 | IO | PLL5_OUT0n | | B19 | | | |
| B9 | VREFB4N4 | IO | PLL5_OUT0p | | A19 | | | |
| B9 | VREFB4N4 | IO | PLL5_OUT1n | | C18 | | | |
| B9 | VREFB4N4 | IO | PLL5_OUT1p | | B18 | | | |
| B4 | VREFB4N4 | IO | CLK12n | | B20 | | | |
| B4 | VREFB4N4 | IO | CLK12p | | A20 | | | |
| B4 | VREFB4N4 | IO | CLK13n | | D19 | | | |
| B4 | VREFB4N4 | IO | CLK13p | | C19 | | | |
| B9 | | VCC_PLL5_OUT | | | K18 | | | |
| | | VCCD_PLL5 | | | L19 | | | |
| | | VCCA_PLL5 | | | L20 | | | |
| | | GNDA_PLL5 | | | J19 | | | |
| | | GNDA_PLL5 | | | K19 | | | |
| | | GNDA_PLL11 | | | J21 | | | |
| | | GNDA_PLL11 | | | K21 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | VCCA_PLL11 | | | K20 | | | |
| | | VCCD_PLL11 | | | L21 | | | |
| B11 | | VCC_PLL11_OUT | | | K22 | | | |
| B3 | VREFB3N0 | IO | CLK14p | | C21 | | | |
| B3 | VREFB3N0 | IO | CLK14n | | D21 | | | |
| B3 | VREFB3N0 | IO | CLK15p | | C20 | | | |
| B3 | VREFB3N0 | IO | CLK15n | | D20 | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT0p | | A21 | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT0n | | B21 | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT1p | | B22 | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT1n | | C22 | | | |
| B3 | VREFB3N0 | IO | | | F23 | | | |
| B3 | VREFB3N0 | IO | | | M20 | | | |
| B11 | VREFB3N0 | IO | PLL11_FBp/OUT2p | | D22 | | | |
| B11 | VREFB3N0 | IO | PLL11_FBn/OUT2n | | E22 | | | |
| B3 | VREFB3N0 | IO | | PGM2 | E20 | | | |
| B3 | VREFB3N0 | IO | | PGM1 | F20 | | | |
| B3 | VREFB3N0 | IO | | PGM0 | G21 | | | |
| B3 | VREFB3N0 | IO | | ASDO | H21 | | | |
| B3 | VREFB3N0 | IO | | nCSO | F22 | | | |
| B3 | VREFB3N0 | IO | | CRC_ERROR | G22 | | | |
| B3 | VREFB3N0 | IO | | DATA0 | H22 | | | |
| B3 | VREFB3N0 | IO | | DATA1 | F21 | | | |
| B3 | VREFB3N0 | VREFB3N0 | VREFB3N0 | | D23 | | | |
| B3 | VREFB3N0 | IO | DQS10T | | B23 | DQS5T | | |
| B3 | VREFB3N0 | IO | DQ10T | | B24 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N0 | IO | DQ10T | | A23 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N0 | IO | DQ10T | | C24 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N0 | IO | DQSn10T | | C23 | DQSn5T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQ10T | | D24 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | | | J22 | | | |
| | | NC (Note 4) | | | M21 | | | |
| | | NC (Note 4) | | | G23 | | | |
| B3 | VREFB3N1 | IO | | | N21 | | | |
| B3 | VREFB3N1 | IO | | | L22 | | | |
| | | NC (Note 4) | | | E24 | | | |
| B3 | VREFB3N1 | IO | | | H23 | | | |
| B3 | VREFB3N1 | IO | | | M22 | | | |
| B3 | VREFB3N1 | IO | DQS11T | | B25 | DQVLD5T | DQS2T | |
| B3 | VREFB3N1 | IO | DQ11T | | D25 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQ11T | | A25 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQ11T | | A26 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQSn11T | | C25 | DQ5T | DQSn2T | DQ1T |
| B3 | VREFB3N1 | IO | DQ11T | | B26 | DQ5T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | | | J23 | | | |
| | | NC (Note 4) | | | N22 | | | |
| B3 | VREFB3N1 | IO | | | F24 | | | |
| B3 | VREFB3N1 | IO | | | G24 | | | |
| | | NC (Note 4) | | | K23 | | | |
| B3 | VREFB3N1 | VREFB3N1 | VREFB3N1 | | F25 | | | |
| | | NC (Note 4) | | | E25 | | | |
| B3 | VREFB3N1 | IO | | | M23 | | | |
| B3 | VREFB3N1 | IO | | | L23 | | | |
| B3 | VREFB3N1 | IO | | | N23 | | | |
| B3 | VREFB3N1 | IO | DQS12T | | C26 | DQS6T | DQVLD2T | DQVLD1T |
| B3 | VREFB3N1 | IO | DQ12T | | A27 | DQ6T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQ12T | | B27 | DQ6T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQ12T | | D26 | DQ6T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQSn12T | | C27 | DQSn6T | DQ2T | DQ1T |
| B3 | VREFB3N1 | IO | DQ12T | | D27 | DQ6T | DQ2T | DQ1T |
| B3 | VREFB3N2 | IO | | | J24 | | | |
| | | NC (Note 4) | | | E26 | | | |
| B3 | VREFB3N2 | IO | | | H24 | | | |
| | | NC (Note 4) | | | K24 | | | |
| B3 | VREFB3N2 | IO | | | L24 | | | |
| | | NC (Note 4) | | | G25 | | | |
| B3 | VREFB3N2 | IO | | | M24 | | | |
| B3 | VREFB3N2 | IO | | | N24 | | | |
| B3 | VREFB3N2 | IO | DQS13T | | B28 | DQVLD6T | | DQS1T |
| B3 | VREFB3N2 | IO | DQ13T | | A28 | DQ6T | DQ2T | DQ1T |
| B3 | VREFB3N2 | IO | DQ13T | | A29 | DQ6T | DQ2T | DQ1T |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B3 | VREFB3N2 | IO | DQ13T | | D28 | DQ6T | DQ2T | DQ1T |
| B3 | VREFB3N2 | IO | DQSn13T | | C28 | DQ6T | DQ2T | DQSn1T |
| B3 | VREFB3N2 | IO | DQ13T | | B29 | DQ6T | | |
| B3 | VREFB3N2 | IO | | | J25 | | | |
| | | NC (Note 4) | | | K25 | | | |
| B3 | VREFB3N2 | IO | | | F26 | | | |
| B3 | VREFB3N2 | IO | | | H25 | | | |
| B3 | VREFB3N2 | IO | | | L25 | | | |
| B3 | VREFB3N2 | VREFB3N2 | VREFB3N2 | | F28 | | | |
| B3 | VREFB3N2 | IO | | | G26 | | | |
| B3 | VREFB3N2 | IO | | | H26 | | | |
| B3 | VREFB3N2 | IO | | | M25 | | | |
| | | NC (Note 4) | | | N25 | | | |
| B3 | VREFB3N2 | IO | DQS14T | | C29 | DQS7T | | |
| B3 | VREFB3N2 | IO | DQ14T | | A30 | DQ7T | DQ3T | DQ1T |
| B3 | VREFB3N2 | IO | DQ14T | | B30 | DQ7T | DQ3T | DQ1T |
| B3 | VREFB3N2 | IO | DQ14T | | D29 | DQ7T | DQ3T | DQ1T |
| B3 | VREFB3N2 | IO | DQSn14T | | C30 | DQSn7T | DQ3T | DQ1T |
| B3 | VREFB3N2 | IO | DQ14T | | D30 | DQ7T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | | | J26 | | | |
| | | NC (Note 4) | | | E27 | | | |
| B3 | VREFB3N3 | IO | | | E28 | | | |
| | | NC (Note 4) | | | K26 | | | |
| B3 | VREFB3N3 | IO | | | L26 | | | |
| B3 | VREFB3N3 | IO | | | F27 | | | |
| B3 | VREFB3N3 | IO | | | H27 | | | |
| B3 | VREFB3N3 | IO | | | M26 | | | |
| B3 | VREFB3N3 | IO | DQS15T | | B31 | DQVLD7T | DQS3T | |
| B3 | VREFB3N3 | IO | DQ15T | | A32 | DQ7T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | DQ15T | | A31 | DQ7T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | DQ15T | | D31 | DQ7T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | DQSn15T | | C31 | DQ7T | DQSn3T | DQ1T |
| B3 | VREFB3N3 | IO | DQ15T | | B32 | DQ7T | DQ3T | DQ1T |
| | | NC (Note 4) | | | N26 | | | |
| B3 | VREFB3N3 | IO | | | J27 | | | |
| B3 | VREFB3N3 | IO | | | G27 | | | |
| B3 | VREFB3N3 | IO | | | K27 | | | |
| B3 | VREFB3N3 | IO | | | L27 | | | |
| B3 | VREFB3N3 | VREFB3N3 | VREFB3N3 | | F31 | | | |
| B3 | VREFB3N3 | IO | | | E29 | | | |
| B3 | VREFB3N3 | IO | | | G28 | | | |
| | | NC (Note 4) | | | M27 | | | |
| B3 | VREFB3N3 | IO | DQS16T | | C32 | DQS8T | DQVLD3T | |
| B3 | VREFB3N3 | IO | DQ16T | | B33 | DQ8T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | DQ16T | | A33 | DQ8T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | DQ16T | | D32 | DQ8T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | DQSn16T | | C33 | DQSn8T | DQ3T | DQ1T |
| B3 | VREFB3N3 | IO | DQ16T | | D33 | DQ8T | DQ3T | DQ1T |
| | | NC (Note 4) | | | N27 | | | |
| B3 | VREFB3N4 | IO | | | K28 | | | |
| B3 | VREFB3N4 | IO | | | F29 | | | |
| | | NC (Note 4) | | | E30 | | | |
| B3 | VREFB3N4 | IO | | | H28 | | | |
| B3 | VREFB3N4 | IO | | | F30 | | | |
| B3 | VREFB3N4 | IO | | | G29 | | | |
| | | NC (Note 4) | | | J28 | | | |
| B3 | VREFB3N4 | IO | | | L28 | | | |
| B3 | VREFB3N4 | IO | DQS17T | | B34 | DQVLD8T | | |
| B3 | VREFB3N4 | IO | DQ17T | | A34 | DQ8T | DQ3T | DQ1T |
| B3 | VREFB3N4 | IO | DQ17T | | A35 | DQ8T | DQ3T | DQ1T |
| B3 | VREFB3N4 | IO | DQ17T | | C35 | DQ8T | DQ3T | |
| B3 | VREFB3N4 | VREFB3N4 | VREFB3N4 | | D35 | | | |
| B3 | VREFB3N4 | IO | DQSn17T | | B35 | DQ8T | DQ3T | DQ1T |
| B3 | VREFB3N4 | IO | DQ17T | | C34 | DQ8T | | |
| B3 | VREFB3N4 | IO | | | M28 | | | |
| B3 | VREFB3N4 | IO | | DATA2 | E31 | | | |
| B3 | VREFB3N4 | IO | | DATA3 | E33 | | | |
| B3 | VREFB3N4 | IO | | DATA4 | H29 | | | |
| B3 | VREFB3N4 | IO | | DATA5 | J29 | | | |
| B3 | VREFB3N4 | IO | | DATA6 | E32 | | | |
| B3 | VREFB3N4 | IO | | DATA7 | F32 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| B3 | VREFB3N4 | IO | | RDYnBSY | G31 | | | |
| B3 | VREFB3N4 | IO | INIT_DONE | INIT_DONE | H30 | | | |
| B3 | VREFB3N4 | nSTATUS | | nSTATUS | A37 | | | |
| B3 | VREFB3N4 | nCE | | nCE | B36 | | | |
| B3 | VREFB3N4 | DCLK | | DCLK | D34 | | | |
| B3 | VREFB3N4 | CONF_DONE | | CONF_DONE | F33 | | | |
| | | VCCIO2 | | | D39 | | | |
| | | VCCIO2 | | | H33 | | | |
| | | VCCIO2 | | | U26 | | | |
| | | VCCIO2 | | | V39 | | | |
| | | VCCIO2 | | | W35 | | | |
| | | VCCIO1 | | | AA35 | | | |
| | | VCCIO1 | | | AB39 | | | |
| | | VCCIO1 | | | AC26 | | | |
| | | VCCIO1 | | | AF31 | | | |
| | | VCCIO1 | | | AM33 | | | |
| | | VCCIO1 | | | AT39 | | | |
| | | VCCIO8 | | | AF23 | | | |
| | | VCCIO8 | | | AN32 | | | |
| | | VCCIO8 | | | AR21 | | | |
| | | VCCIO8 | | | AW22 | | | |
| | | VCCIO8 | | | AW36 | | | |
| | | VCCIO7 | | | AF17 | | | |
| | | VCCIO7 | | | AN8 | | | |
| | | VCCIO7 | | | AR19 | | | |
| | | VCCIO7 | | | AW4 | | | |
| | | VCCIO7 | | | AW18 | | | |
| | | VCCIO6 | | | AA5 | | | |
| | | VCCIO6 | | | AB1 | | | |
| | | VCCIO6 | | | AC14 | | | |
| | | VCCIO6 | | | AF9 | | | |
| | | VCCIO6 | | | AM7 | | | |
| | | VCCIO6 | | | AT1 | | | |
| | | VCCIO5 | | | D1 | | | |
| | | VCCIO5 | | | H7 | | | |
| | | VCCIO5 | | | U14 | | | |
| | | VCCIO5 | | | V1 | | | |
| | | VCCIO5 | | | W5 | | | |
| | | VCCIO4 | | | A4 | | | |
| | | VCCIO4 | | | A18 | | | |
| | | VCCIO4 | | | E19 | | | |
| | | VCCIO4 | | | G8 | | | |
| | | VCCIO4 | | | P17 | | | |
| | | VCCIO3 | | | A22 | | | |
| | | VCCIO3 | | | A36 | | | |
| | | VCCIO3 | | | E21 | | | |
| | | VCCIO3 | | | G32 | | | |
| | | VCCIO3 | | | P23 | | | |
| | | VCCINT | | | AA16 | | | |
| | | VCCINT | | | AA18 | | | |
| | | VCCINT | | | AA22 | | | |
| | | VCCINT | | | AA24 | | | |
| | | VCCINT | | | AB15 | | | |
| | | VCCINT | | | AB17 | | | |
| | | VCCINT | | | AB19 | | | |
| | | VCCINT | | | AB21 | | | |
| | | VCCINT | | | AB23 | | | |
| | | VCCINT | | | AB25 | | | |
| | | VCCINT | | | AC16 | | | |
| | | VCCINT | | | AC18 | | | |
| | | VCCINT | | | AC20 | | | |
| | | VCCINT | | | AC22 | | | |
| | | VCCINT | | | AC24 | | | |
| | | VCCINT | | | AD17 | | | |
| | | VCCINT | | | AD19 | | | |
| | | VCCINT | | | AD21 | | | |
| | | VCCINT | | | AD23 | | | |
| | | VCCINT | | | AE16 | | | |
| | | VCCINT | | | AE18 | | | |
| | | VCCINT | | | AE20 | | | |
| | | VCCINT | | | AE22 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | VCCINT | | | AE24 | | | |
| | | VCCINT | | | R16 | | | |
| | | VCCINT | | | R18 | | | |
| | | VCCINT | | | R20 | | | |
| | | VCCINT | | | R22 | | | |
| | | VCCINT | | | R24 | | | |
| | | VCCINT | | | T15 | | | |
| | | VCCINT | | | T17 | | | |
| | | VCCINT | | | T19 | | | |
| | | VCCINT | | | T21 | | | |
| | | VCCINT | | | T23 | | | |
| | | VCCINT | | | T25 | | | |
| | | VCCINT | | | U16 | | | |
| | | VCCINT | | | U18 | | | |
| | | VCCINT | | | U20 | | | |
| | | VCCINT | | | U22 | | | |
| | | VCCINT | | | U24 | | | |
| | | VCCINT | | | V15 | | | |
| | | VCCINT | | | V17 | | | |
| | | VCCINT | | | V19 | | | |
| | | VCCINT | | | V21 | | | |
| | | VCCINT | | | V23 | | | |
| | | VCCINT | | | V25 | | | |
| | | VCCINT | | | W16 | | | |
| | | VCCINT | | | W18 | | | |
| | | VCCINT | | | W22 | | | |
| | | VCCINT | | | W24 | | | |
| | | VCCINT | | | Y15 | | | |
| | | VCCINT | | | Y17 | | | |
| | | VCCINT | | | Y23 | | | |
| | | VCCINT | | | Y25 | | | |
| | | GND | | | A2 | | | |
| | | GND | | | A16 | | | |
| | | GND | | | A24 | | | |
| | | GND | | | A38 | | | |
| | | GND | | | AA15 | | | |
| | | GND | | | AA17 | | | |
| | | GND | | | AA23 | | | |
| | | GND | | | AA25 | | | |
| | | GND | | | AB16 | | | |
| | | GND | | | AB18 | | | |
| | | GND | | | AB20 | | | |
| | | GND | | | AB22 | | | |
| | | GND | | | AB24 | | | |
| | | GND | | | AC5 | | | |
| | | GND | | | AC15 | | | |
| | | GND | | | AC17 | | | |
| | | GND | | | AC19 | | | |
| | | GND | | | AC21 | | | |
| | | GND | | | AC23 | | | |
| | | GND | | | AC25 | | | |
| | | GND | | | AC35 | | | |
| | | GND | | | AD1 | | | |
| | | GND | | | AD10 | | | |
| | | GND | | | AD16 | | | |
| | | GND | | | AD18 | | | |
| | | GND | | | AD20 | | | |
| | | GND | | | AD22 | | | |
| | | GND | | | AD24 | | | |
| | | GND | | | AD30 | | | |
| | | GND | | | AD39 | | | |
| | | GND | | | AE15 | | | |
| | | GND | | | AE17 | | | |
| | | GND | | | AE19 | | | |
| | | GND | | | AE21 | | | |
| | | GND | | | AE23 | | | |
| | | GND | | | AE25 | | | |
| | | GND | | | AF15 | | | |
| | | GND | | | AF20 | | | |
| | | GND | | | AF25 | | | |
| | | GND | | | AK7 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | GND | | | AK33 | | | |
| | | GND | | | AL20 | | | |
| | | GND | | | AL30 | | | |
| | | GND | | | AM10 | | | |
| | | GND | | | AN10 | | | |
| | | GND | | | AN30 | | | |
| | | GND | | | AR17 | | | |
| | | GND | | | AR23 | | | |
| | | GND | | | AV1 | | | |
| | | GND | | | AV39 | | | |
| | | GND | | | AW2 | | | |
| | | GND | | | AW16 | | | |
| | | GND | | | AW24 | | | |
| | | GND | | | AW38 | | | |
| | | GND | | | B1 | | | |
| | | GND | | | B39 | | | |
| | | GND | | | E17 | | | |
| | | GND | | | E23 | | | |
| | | GND | | | G10 | | | |
| | | GND | | | G30 | | | |
| | | GND | | | J10 | | | |
| | | GND | | | J20 | | | |
| | | GND | | | J30 | | | |
| | | GND | | | K7 | | | |
| | | GND | | | K33 | | | |
| | | GND | | | P24 | | | |
| | | GND | | | R15 | | | |
| | | GND | | | R17 | | | |
| | | GND | | | R19 | | | |
| | | GND | | | R21 | | | |
| | | GND | | | R23 | | | |
| | | GND | | | R25 | | | |
| | | GND | | | T1 | | | |
| | | GND | | | T14 | | | |
| | | GND | | | T16 | | | |
| | | GND | | | T18 | | | |
| | | GND | | | T20 | | | |
| | | GND | | | T22 | | | |
| | | GND | | | T24 | | | |
| | | GND | | | T26 | | | |
| | | GND | | | T39 | | | |
| | | GND | | | U5 | | | |
| | | GND | | | U15 | | | |
| | | GND | | | U17 | | | |
| | | GND | | | U19 | | | |
| | | GND | | | U21 | | | |
| | | GND | | | U23 | | | |
| | | GND | | | U25 | | | |
| | | GND | | | U35 | | | |
| | | GND | | | V16 | | | |
| | | GND | | | V18 | | | |
| | | GND | | | V20 | | | |
| | | GND | | | V22 | | | |
| | | GND | | | V24 | | | |
| | | GND | | | W15 | | | |
| | | GND | | | W17 | | | |
| | | GND | | | W23 | | | |
| | | GND | | | W25 | | | |
| | | GND | | | Y9 | | | |
| | | GND | | | Y16 | | | |
| | | GND | | | Y18 | | | |
| | | GND | | | Y22 | | | |
| | | GND | | | Y24 | | | |
| | | GND | | | Y31 | | | |
| | | VCCPD2 | | | R26 | | | |
| | | VCCPD2 | | | V26 | | | |
| | | VCCPD2 | | | W26 | | | |
| | | VCCPD1 | | | AB26 | | | |
| | | VCCPD1 | | | AD25 | | | |
| | | VCCPD1 | | | AF26 | | | |
| | | VCCPD8 | | | AF21 | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s)/DQ Group for DQS x4 Mode | Configuration Function for Stratix II Only (Note 1) | F1508 | DQ Group for DQS x8/x9 Mode | DQ Group for DQS x16/x18 Mode | DQ Group for DQS x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|
| | | VCCPD8 | | | AF22 | | | |
| | | VCCPD8 | | | AF24 | | | |
| | | VCCPD7 | | | AF16 | | | |
| | | VCCPD7 | | | AF18 | | | |
| | | VCCPD7 | | | AF19 | | | |
| | | VCCPD6 | | | AB14 | | | |
| | | VCCPD6 | | | AD15 | | | |
| | | VCCPD6 | | | AF14 | | | |
| | | VCCPD5 | | | R14 | | | |
| | | VCCPD5 | | | V14 | | | |
| | | VCCPD5 | | | W14 | | | |
| | | VCCPD4 | | | P16 | | | |
| | | VCCPD4 | | | P18 | | | |
| | | VCCPD4 | | | P19 | | | |
| | | VCCPD3 | | | P21 | | | |
| | | VCCPD3 | | | P22 | | | |
| | | VCCPD3 | | | P25 | | | |

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix II device pin table for details.

(2) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix II device and should be connected on the board to configure the FPGA prototype.

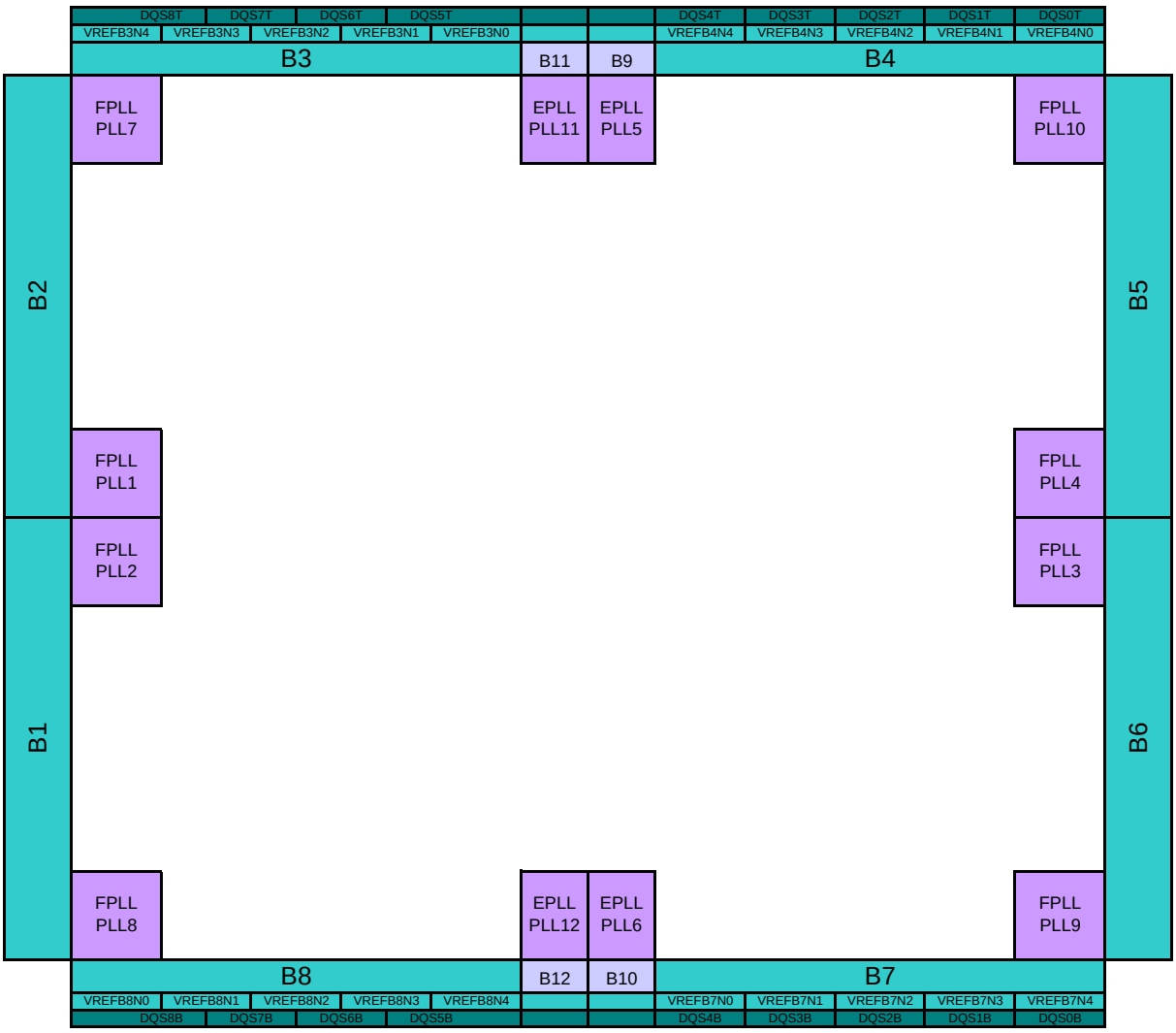
(3) This NC pin is a VREF pin in the Stratix II device and should be connected to the VREF input reference voltage for the FPGA prototype. If the VREF is not used, connect pin to VCC or GND.

(4) This NC pin is an IO pin in the Stratix II device and can be left unconnected.

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| | ***Supply and Reference Pins*** | |
| VCCINT | Power | These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HyperTransport™ technology, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards including TDO and nCEO. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards. |
| VCCPD[1..8] | Power | Dedicated power pins. This supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers all the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, and nCE. The VCCPD pins must be connected to 3.3 V and must ramp-up from 0 V to 3.3 V within 100 ms to ensure successful configuration. |
| GND | Ground | Device ground pins. All GND pins should be connected to the board GND plane. |
| VREFB[3,4,7,8]N[0..4] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All the VREF pins within a bank are shorted togetherIf VREF pins are not used, designers should connect them to either VCC or GND. |
| VCC_PLL5_OUT | Power | External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p & PLL5_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 9. |
| VCC_PLL6_OUT | Power | External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p & PLL6_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 10. |
| VCC_PLL11_OUT | Power | External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p & PLL11_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 11. |
| VCC_PLL12_OUT | Power | External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p & PLL12_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 12. |
| VCCA_PLL[1..12] | Power | Analog power for PLLs[1..12]. The designer must connect these pins to 1.2 V, even if the PLL is not used. |
| VCCD_PLL[1..12] | Power | Digital power for PLLs[1..12]. The designer must connect these pins to 1.2 V, even if the PLL is not used. |
| GNDA_PLL[1..12] | Ground | Analog ground for PLLs[1..12]. All analog GND pins should be connected to the board analog GND plane. |
| NC | No Connect | Do not drive signals into these pins. Exceptions are the configuration pins and the pins noted in this pin list. These pins should be properly connected on the board when prototyping with the Stratix II FPGA device. Make sure to check the pin out information for the Stratix II FPGA prototype compiled design when laying out the board to ensure compatibility between the HardCopy II device and the Stratix II FPGA prototype device. |
| RUP4 | I/O, Input | Reference pin for banks 3 & 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin. |
| RDN4 | I/O, Input | Reference pin for banks 3 & 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin. |
| RUP7 | I/O, Input | Reference pin for banks 7 & 8. The external precision resistor Rup must be connected to the designated RUP pin within bank 7. If not required, this pin is a regular I/O pin. |
| RDN7 | I/O, Input | Reference pin for banks 7 & 8. The external precision resistor Rdn must be connected to the designated RDN pin within bank 7. If not required, this pin is a regular I/O pin. |
| | ***Dedicated Configuration/JTAG Pins*** | |
| nIO_PULLUP | Input | Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during power up. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on. |
| VCCSEL | Input | Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input) and nCE. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD or ground. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory. |
| TEMPDIODEp | Input | Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND. |
| TEMPDIODEn | Input | Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND. |
| DCLK | Input | Dedicated configuration clock pin on Stratix II devices, but kept in HardCopy II for compatibility reasons. It's not required to clock this pin for HardCopy II. |
| nCE | Input | Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low. |
| nCONFIG | Input | Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy II to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin. |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Once the power up delays are done and the initialization cycle starts, CONF_DONE is released. It is not available as a user I/O pin. |
| nCEO | Output | Output that drives low when device initialization is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating. |

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| nSTATUS | Bidirectional (open-drain) | This is a dedicated power up block status pin. The HardCopy II drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, the device enters an error state when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin. |
| PORSEL | Input | Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms. This is in addition to the Instant On delay mode chosen (i.e. instant or additional 50 ms). |
| TCK | Input | Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND. |
| TMS | Input | Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC. |
| TDI | Input | Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC. |
| TDO | Output | Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected. |
| TRST | Input | Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. The JTAG circuitry can be disabled by connecting TRST to GND. |
| ***Clock and PLL Pins*** | | |
| CLK[1,3,9,11]p | Clock, Input | Dedicated clock input pins 1, 3, 9, & 11 that can also be used for data inputs. |
| CLK[1,3,9,11]n | Clock, Input | Dedicated negative terminal clock input pins for differential clock input that can also be used for data inputs. |
| CLK[0,2,8,10]p/DIFFIO_RX_C[0..3]p | I/O, Clock, RX channel | These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels. |
| CLK[0,2,8,10]n/DIFFIO_RX_C[0..3]n | I/O, Clock, RX channel | These pins can be used as I/O pins, the negative terminal clock input pins for differential clock input, or the negative terminal data pins of differential receiver channels. |
| CLK[4-7,12-15]p | I/O, Clock | These pins can be used as I/O pins or clock input pins. |
| CLK[4-7,12-15]n | I/O, Clock | These pins can be used as I/O pins or negative terminal clock input pins for differential clock input. |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you mus drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs. |
| FPLL[7..10]CLKp | Clock, Input | Dedicated clock inputs for fast PLLs (PLLs 7 through 10) that can also be used for data inputs. |
| FPLL[7..10]CLKn | Clock, Input | Dedicated negative terminal associated with FPLL[7..10]CLKp pins that can also be used for data inputs. |
| PLL5_OUT[0..1]p | I/O, Output | Optional external clock outputs [0..1] from enhanced PLL 5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5). |
| PLL5_OUT[0..1]n | I/O, Output | Optional negative terminal for external clock outputs [0..1] from PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL6_OUT[0..1]p | I/O, Output | Optional external clock outputs [0..1] from enhanced PLL 6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6). |
| PLL6_OUT[0..1]n | I/O, Output | Optional negative terminal for external clock outputs [0..1] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. |
| PLL[5..6]_FBp/OUT2p | I/O, Input, Output | These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[5..6]. |
| PLL[5..6]_FBn/OUT2n | I/O, Input, Output | These pins can be used as I/O pins, negative terminal input for external feedback input PLL[5..6]_FBp or negative terminal clock output pins for differential clock output. |
| PLL11_OUT[0..1]p | I/O, Output | Optional external clock outputs [0..1] from enhanced PLL 11. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL11). |
| PLL11_OUT[0..1]n | I/O, Output | Optional negative terminal for external clock outputs [0..1] from PLL11. If the clock outputs are single ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in phase o 180 degrees out of phase. |
| PLL12_OUT[0..1]p | I/O, Output | Optional external clock outputs [0..1] from enhanced PLL 12. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL12). |
| PLL12_OUT[0..1]n | I/O, Output | Optional negative terminal for external clock outputs [0..1] from PLL12. If the clock outputs are single ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in phase o 180 degrees out of phase. |
| PLL[11..12]_FBp/OUT2p | I/O, Input, Output | These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[11..12]. |
| PLL[11..12]_FBn/OUT2n | I/O, Input, Output | These pins can be used as I/O pins, negative terminal input for external feedback input PLL[11..12]_FBp or negative terminal clock output pins for differential clock output. |
| ***Optional/Dual-Purpose Configuration Pins*** | | |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. |
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| INIT_DONE | I/O, Output (open-drain) | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| ***Dual-Purpose Differential & External Memory Interface Pins*** | | |
| DIFFIO_RX[15..70,103..158]p/n | I/O, RX channel | Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. |

| Pin Name | Pin Type (1st, 2nd, & 3rd Function) | Pin Description |
|---|---|---|
| DIFFIO_TX[14..71,102..159]p/n | I/O, TX channel | Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pin with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. |
| DQS[0..1][T,B] (x32/x36)<br>DQS[0..3][T,B] (x16/x18)<br>DQS[0..8][T,B] (x8/x9)<br>DQS[0..17][T,B] (x4) | I/O, DQS | Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic. |
| DQSn[0..1][T,B] (x32/x36)<br>DQSn[0..3][T,B] (x16/x18)<br>DQSn[0..8][T,B] (x8/x9)<br>DQSn[0..17][T,B] (x4) | I/O, DQSn | Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry. |
| DQ[0..1][T,B] (x32/x36)<br>DQ[0..3][T,B] (x16/x18)<br>DQ[0..8][T,B] (x8/x9)<br>DQ[0..17][T,B] (x4) | I/O, DQ | Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list. |
| DQVLD[0..1][T,B] (x32/x36)<br>DQVLD[0..3][T,B] (x16/x18)<br>DQVLD[0..8][T,B] (x8/x9) | I/O, DQVLD | Optional data valid signal for use in external memory interfacing. |




**Notes:**

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
3. The DQ/DQS groups depicted above are in x8/x9 mode. DQ/DQS support differs across the package offerings.

| Version Number | Date | Changes Made |
|---|---|---|
| Preliminary | 2/10/2005 | |
| 1.0 | 9/21/2005 | Pintable updated to match latest Engineering pintable released 7/20/05. This pintable is compatible with Quartus II Version 5.1 |
| 1.1 | 3/27/2007 | Pintable updated to match latest Engineering pintable released 3/31/06. |
| | | Added configuration function column for FPGA prototyping in the pin list. |
| | | Added "DQ Group for DQS x4 Mode" description to the "Optional Function(s)" header in the pin list. |
| | | Added footnotes in the pin list to describe the HardCopy II pins that have functions which differ from the Stratix II. |
| | | Updated VREF bank numbers in the pin definition. |
| | | Added more NC pin definition details for the configuration and noted pins. |
| | | Updated DQS, DQSn, DQ, and DQLVD pin numbers in the pin definition. |