Pin Information for HardCopy® II HC210W / Stratix® II EP2S30 F484 Companion Devices Version 1.0

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
		NC (Note 3)			F18	
B2		IO	DIFFIO_RX22p		C22	
B2		IO	DIFFIO_RX22n		C21	
B2		IO	DIFFIO_TX22p		E20	
B2		IO	DIFFIO_TX22n		E19	
		NC (Note 7)			D22	
B2		IO			D21	
B2		IO	DIFFIO_TX21p		F20	
B2		IO	DIFFIO_TX21n		F19	
		NC (Note 7)			E22	
B2		IO			E21	
B2		IO	DIFFIO_TX20p		G20	
B2		IO	DIFFIO_TX20n		G19	
B2		IO	DIFFIO_RX19p		F22	
B2		IO	DIFFIO_RX19n		F21	
B2		IO	DIFFIO_TX19p		G18	
B2		IO	DIFFIO_TX19n		G17	
B2		IO	DIFFIO_RX18p		H20	
B2		IO	DIFFIO_RX18n		H19	
B2		IO	DIFFIO_TX18p		H18	
B2		IO	DIFFIO_TX18n		H17	
B2		IO	DIFFIO_RX17p		G22	
B2		IO	DIFFIO_RX17n		G21	
B2		IO	DIFFIO_TX17p		J17	
B2		IO	DIFFIO_TX17n		J16	
		NC (Note 3)			L19	
B2		IO	DIFFIO_RX16p		H22	
B2		IO	DIFFIO_RX16n		H21	
B2		IO			J19	
		NC (Note 7)			J18	
B2		IO	DIFFIO_RX15p		J21	
B2		IO	DIFFIO_RX15n		J20	
B2		IO	DIFFIO_TX15p		K18	
B2		IO	DIFFIO_TX15n		K17	
B2		IO	DIFFIO_RX14p		K20	
B2		IO	DIFFIO_RX14n		K19	
B2		IO			K16	
		NC (Note 7)			K15	
B2		IO	DIFFIO_RX13p		K22	
B2		IO	DIFFIO_RX13n		K21	
B2		IO	DIFFIO_TX13p		L16	
B2		IO	DIFFIO_TX13n		L15	
B2		IO	CLK0n/DIFFIO_RX_C0n		L20	
B2		IO	CLK0p/DIFFIO_RX_C0p		L21	
B2		CLK1n	INPUT		M20	
B2		CLK1p	INPUT		M21	
		VCCD_PLL1			M16	
		VCCA_PLL1			M17	
		GNDA_PLL1			L17	
		GNDA_PLL1			L18	
		GNDA_PLL2			N17	
		GNDA_PLL2			N18	
		VCCA_PLL2			M19	
		VCCD_PLL2			M18	
B1		IO	CLK2p/DIFFIO_RX_C1p		N22	
B1		IO	CLK2n/DIFFIO_RX_C1n		N21	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
B1		CLK3p	INPUT		N20	
B1		CLK3n	INPUT		N19	
		NC (Note 7)			P21	
B1		IO			P20	
B1		IO	DIFFIO_TX12p		N16	
B1		IO	DIFFIO_TX12n		N15	
B1		IO	DIFFIO_RX11p		R22	
B1		IO	DIFFIO_RX11n		R21	
		NC (Note 7)			P17	
B1		IO			P16	
		NC (Note 3)			R20	
B1		IO	DIFFIO_RX10p		T22	
B1		IO	DIFFIO_RX10n		T21	
B1		IO			P19	
		NC (Note 7)			P18	
		NC (Note 7)			U22	
B1		IO			U21	
B1		IO	DIFFIO_TX9p		R19	
B1		IO	DIFFIO_TX9n		R18	
B1		IO	DIFFIO_RX8p		T20	
B1		IO	DIFFIO_RX8n		T19	
B1		IO			R17	
		NC (Note 7)			R16	
B1		IO	DIFFIO_RX7p		U20	
B1		IO	DIFFIO_RX7n		U19	
B1		IO	DIFFIO_TX7p		T18	
B1		IO	DIFFIO_TX7n		T17	
B1		IO	DIFFIO_RX6p		V22	
B1		IO	DIFFIO_RX6n		V21	
B1		IO			U18	
		NC (Note 7)			U17	
B1		IO	DIFFIO_RX5p		Y22	
B1		IO	DIFFIO_RX5n		Y21	
B1		IO	DIFFIO_TX5p		V19	
B1		IO	DIFFIO_TX5n		V18	
B1		IO	DIFFIO_RX4p		W22	
B1		IO	DIFFIO_RX4n		W21	
B1		IO	DIFFIO_TX4p		W20	
B1		IO	DIFFIO_TX4n		W19	
		NC (Note 3)			V20	
B8		TDI		TDI	AB21	
B8		TMS		TMS	AA20	
B8		TCK		TCK	AA19	
B8		TRST		TRST	AB19	
B8		nCONFIG		nCONFIG	W18	
B8		VCCSEL		VCCSEL	V17	
		NC (Note 7)			Y20	
B8		IO		CS	T16	
B8		IO		CLKUSR	U16	
B8		IO		nWS	V16	
B8		IO		nRS	W17	
		NC (Note 7)			W16	
B8		IO			W15	
B8		IO			T15	
B8		IO			V15	
		NC (Note 3)			Y19	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
B8		IO			R15	
B8		IO			U15	
B8		IO			Y14	
B8		IO			W14	
B8		IO			V14	
B8		IO			R14	
B8		IO			Y13	
		NC (Note 7)			U14	
B8		IO			T14	
B8		IO			Y18	
B8		IO			AA18	
B8		IO			Y17	
B8		IO			AB18	
B8		IO			AB17	
B8		IO			AA17	
B8		IO			U13	
B8		IO			AB16	
B8		IO			AA16	
B8		IO			Y16	
B8		IO			Y15	
B8		IO			AB15	
B8		IO			AA15	
		NC (Note 3)			AA14	
B8		IO			T13	
B8		IO			V13	
B8		IO			W13	
B8		IO			U12	
B8		IO		RUnLU	V11	
B8		IO	DEV_OE	DEV_OE	V12	
B8		IO	DEV_CLRn	DEV_CLRn	W11	
B8		IO		nCS	W12	
B8		IO	CLK5n		Y12	
B8		IO	CLK5p		AA12	
B8		IO	CLK4n		AA13	
B8		IO	CLK4p		AB13	
		GNDA_PLL6			T11	
		GNDA_PLL6			T12	
		VCCA_PLL6			R12	
		VCCD_PLL6			U11	
B10		VCC_PLL6_OUT			R11	
B7		IO	CLK7p		Y10	
B7		IO	CLK7n		W10	
B7		IO	CLK6p		AA11	
B7		IO	CLK6n		Y11	
B10		IO	PLL6_OUT1p		AA9	
B10		IO	PLL6_OUT1n		Y9	
B10		IO	PLL6_OUT0p		AB10	
B10		IO	PLL6_OUT0n		AA10	
B10		IO	PLL6_FBp/OUT2p		W9	
B10		IO	PLL6_FBn/OUT2n		V9	
B7		IO			T10	
B7		IO			AB8	
B7		IO			AA8	
		NC (Note 3)			W8	
B7		IO			Y7	
B7		IO			Y8	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
B7		IO			AB7	
B7		IO			AA7	
B7		IO			U10	
B7		IO			V10	
B7		IO			AB6	
B7		IO			AA6	
B7		IO			Y6	
B7		IO			Y5	
B7		IO			AB5	
B7		IO			AA5	
B7		IO			T9	
B7		IO			R9	
B7		IO			U9	
B7		IO			T8	
B7		IO			U8	
B7		IO			V8	
B7		IO			W7	
B7		IO			V7	
		NC (Note 7)			AA4	
		NC (Note 3)			W6	
B7		IO			T7	
B7		IO			V6	
B7		IO			U6	
		NC (Note 7)			Y3	
B7		IO			U7	
B7		IO			W5	
B7		PORSEL		PORSEL	V5	
B7		nIO_PULLUP		nIO_PULLUP	AB2	
B7		PLL_ENA		PLL_ENA	Y4	
		GND			AB4	
B7		nCEO		nCEO	AA3	
		NC (Note 3)			U3	
B6		IO			W4	
B6		IO			W3	
B6		IO			W2	
B6		IO			W1	
B6		IO			V4	
B6		IO			V3	
B6		IO			Y2	
B6		IO			Y1	
B6		IO			U5	
		NC (Note 7)			U4	
B6		IO			V2	
B6		IO			V1	
B6		IO			T6	
B6		IO			T5	
B6		IO			T4	
B6		IO			T3	
B6		IO			R8	
		NC (Note 7)			R7	
B6		IO			U2	
B6		IO			U1	
B6		IO			R6	
		NC (Note 7)			R5	
B6		IO			R4	
B6		IO			R3	

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Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
B6		IO			P6	
B6		IO			P5	
B6		IO			T2	
B6		IO			T1	
		NC (Note 3)			P4	
B6		IO			P8	
B6		IO			P7	
		NC (Note 7)			R2	
B6		IO			R1	
B6		IO			N8	
B6		IO			N7	
B6		IO			P3	
B6		IO			P2	
B6		CLK9n	INPUT		N4	
B6		CLK9p	INPUT		N3	
B6		IO	CLK8n		N2	
B6		IO	CLK8p		N1	
		NC (Note 4)			M5	
		NC (Note 5)			M4	
		NC (Note 6)			N5	
		NC (Note 6)			N6	
		NC (Note 6)			L4	
		NC (Note 6)			L5	
		NC (Note 5)			M6	
		NC (Note 4)			L6	
B5		CLK11p	INPUT		M2	
B5		CLK11n	INPUT		M3	
B5		IO	CLK10p		L2	
B5		IO	CLK10n		L3	
B5		IO			L8	
B5		IO			L7	
B5		IO			K2	
B5		IO			K1	
B5		IO			K8	
		NC (Note 7)			K7	
B5		IO			K4	
B5		IO			K3	
B5		IO			K6	
B5		IO			K5	
B5		IO			J3	
B5		IO			J2	
B5		IO			J6	
B5		IO			J5	
B5		IO			H2	
B5		IO			H1	
		NC (Note 3)			F3	
B5		IO			J8	
		NC (Note 7)			J7	
B5		IO			G2	
B5		IO			G1	
		NC (Note 7)			H6	
B5		IO			H5	
		NC (Note 7)			H4	
B5		IO			H3	
B5		IO			G6	
B5		IO			G5	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
B5		IO			F2	
B5		IO			F1	
B5		IO			G4	
B5		IO			G3	
B5		IO			E2	
B5		IO			E1	
B5		IO			F5	
		NC (Note 7)			F4	
B5		IO			D2	
B5		IO			D1	
B5		IO			E4	
B5		IO			E3	
B5		IO			C2	
B5		IO			C1	
		NC (Note 3)			J4	
		TEMPDIODEp			A2	
		TEMPDIODEn			C3	
B4	VREFB4N0	TDO		TDO	B3	
		NC (Note 2)		MSEL3	A4	
		NC (Note 2)		MSEL2	B4	
		NC (Note 2)		MSEL1	D4	
		NC (Note 2)		MSEL0	E5	
B4	VREFB4N0	IO	RUP4		G7	
B4	VREFB4N0	IO	RDN4		F6	
B4	VREFB4N0	VREFB4N0 (Note 8)	VREFB4N0		C4	
		NC (Note 7)			D3	
B4	VREFB4N0	IO			D5	
B4	VREFB4N0	IO			E6	
B4	VREFB4N1	VREFB4N1	VREFB4N1		D7	
B4	VREFB4N1	IO			F7	
B4	VREFB4N0	IO			D6	
B4	VREFB4N0	IO			E7	
B4	VREFB4N2	IO			E8	
		NC (Note 7)			H7	
B4	VREFB4N0	IO			G8	
B4	VREFB4N1	IO			H9	
B4	VREFB4N0	IO			F8	
B4	VREFB4N0	IO			D8	
B4	VREFB4N0	IO			E9	
B4	VREFB4N1	IO	DQS7T		B5	DQS1T
B4	VREFB4N1	IO	DQ7T		A5	DQ1T
B4	VREFB4N1	IO	DQ7T		C5	DQ1T
B4	VREFB4N1	IO	DQ7T		C6	DQ1T
B4	VREFB4N1	IO	DQSn7T		B6	DQSn1T
B4	VREFB4N1	IO	DQ7T		A6	DQ1T
		NC (Note 7)			F9	
B4	VREFB4N1	IO			G9	
B4	VREFB4N1	IO	DQS9T		B7	DQVLD1T
B4	VREFB4N1	IO	DQ9T		A7	DQ1T
B4	VREFB4N2	IO	DQ9T		C8	DQ1T
B4	VREFB4N2	IO	DQ9T		C7	DQ1T
B4	VREFB4N2	VREFB4N2	VREFB4N2		D9	
B4	VREFB4N2	IO	DQSn9T		B8	DQ1T
B4	VREFB4N2	IO	DQ9T		A8	DQ1T
B4	VREFB4N2	IO			E10	
B9	VREFB4N2	IO	PLL5_FBn/OUT2n		C9	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
B9	VREFB4N2	IO	PLL5_FBp/OUT2p		B9	
B9	VREFB4N2	IO	PLL5_OUT0n		B10	
B9	VREFB4N2	IO	PLL5_OUT0p		A10	
B9	VREFB4N2	IO	PLL5_OUT1n		D10	
B9	VREFB4N2	IO	PLL5_OUT1p		C10	
B4	VREFB4N2	IO	CLK12n		C11	
B4	VREFB4N2	IO	CLK12p		B11	
B4	VREFB4N2	IO	CLK13n		C12	
B4	VREFB4N2	IO	CLK13p		B12	
B9		VCC_PLL5_OUT			G10	
		VCCD_PLL5			G11	
		VCCA_PLL5			F12	
		GNDA_PLL5			F10	
		GNDA_PLL5			F11	
B3	VREFB3N0	IO	CLK14p		A13	
B3	VREFB3N0	IO	CLK14n		B13	
B3	VREFB3N0	IO	CLK15p		C13	
B3	VREFB3N0	IO	CLK15n		D13	
B3	VREFB3N0	IO		PGM2	D12	
B3	VREFB3N0	IO		PGM1	E11	
B3	VREFB3N0	IO		PGM0	H11	
B3	VREFB3N0	IO		ASDO	G12	
B3	VREFB3N0	IO		nCSO	D11	
B3	VREFB3N0	IO		CRC_ERROR	E12	
B3	VREFB3N0	IO		DATA0	E13	
B3	VREFB3N0	IO		DATA1	H12	
B3	VREFB3N0	IO			C14	
B3	VREFB3N0	IO			F13	
B3	VREFB3N0	IO			G13	
B3	VREFB3N0	VREFB3N0	VREFB3N0		B14	
B3	VREFB3N0	IO	DQS11T		B15	DQS2T
B3	VREFB3N1	IO	DQ11T		A15	DQ2T
B3	VREFB3N0	IO	DQ11T		C15	DQ2T
B3	VREFB3N1	IO	DQ11T		C16	DQ2T
B3	VREFB3N1	IO	DQSn11T		B16	DQSn2T
B3	VREFB3N1	IO	DQ11T		A16	DQ2T
B3	VREFB3N0	IO			D14	
B3	VREFB3N1	IO			H14	
B3	VREFB3N1	IO	DQS13T		B17	DQVLD2T
B3	VREFB3N1	IO	DQ13T		A17	DQ2T
B3	VREFB3N1	IO	DQ13T		A18	DQ2T
B3	VREFB3N1	IO	DQ13T		C17	DQ2T
B3	VREFB3N1	IO	DQSn13T		B18	DQ2T
B3	VREFB3N1	IO	DQ13T		C18	DQ2T
		NC (Note 7)			F14	
B3	VREFB3N1	IO			E14	
B3	VREFB3N1	IO			G14	
		NC (Note 7)			D15	
B3	VREFB3N2	IO			E15	
B3	VREFB3N1	IO			J15	
B3	VREFB3N2	IO			F15	
B3	VREFB3N2	VREFB3N2 (Note 8)	VREFB3N2		C19	
		NC (Note 7)			G15	
		NC (Note 7)			D20	
B3	VREFB3N1	VREFB3N1	VREFB3N1		D16	
B3	VREFB3N2	IO			F16	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
		NC (Note 7)			H16	
B3	VREFB3N2	IO			G16	
B3	VREFB3N2	IO		DATA2	D17	
B3	VREFB3N2	IO		DATA3	A19	
B3	VREFB3N2	IO		DATA4	E16	
B3	VREFB3N2	IO		DATA5	E17	
B3	VREFB3N2	IO		DATA6	B19	
B3	VREFB3N2	IO		DATA7	D18	
B3	VREFB3N2	IO		RDYnBSY	F17	
B3	VREFB3N2	IO	INIT_DONE	INIT_DONE	E18	
B3	VREFB3N2	nSTATUS		nSTATUS	B20	
B3	VREFB3N2	nCE		nCE	A21	
B3	VREFB3N2	DCLK		DCLK	D19	
B3	VREFB3N2	CONF_DONE		CONF_DONE	C20	
		VCCIO2			B22	
		VCCIO2			L22	
		VCCIO1			AA22	
		VCCIO1			M22	
		VCCIO8			AB12	
		VCCIO8			AB20	
		VCCIO7			AB3	
		VCCIO7			AB11	
		VCCIO6			AA1	
		VCCIO6			M1	
		VCCIO5			B1	
		VCCIO5			L1	
		VCCIO4			A3	
		VCCIO4			A11	
		VCCIO3			A12	
		VCCIO3			A20	
		VCCINT			H8	
		VCCINT			J9	
		VCCINT			J11	
		VCCINT			J13	
		VCCINT			K10	
		VCCINT			K12	
		VCCINT			L11	
		VCCINT			L13	
		VCCINT			M8	
		VCCINT			M10	
		VCCINT			M12	
		VCCINT			M14	
		VCCINT			N11	
		VCCINT			N13	
		VCCINT			P9	
		VCCINT			P12	
		VCCINT			P14	
		GND			A1	
		GND			A9	
		GND			A14	
		GND			A22	
		GND			AA2	
		GND			AA21	
		GND			AB1	
		GND			AB9	
		GND			AB14	

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F484	DQ Group for DQS x8/x9 Mode
		GND			AB22	
		GND			B2	
		GND			B21	
		GND			H15	
		GND			J1	
		GND			J10	
		GND			J12	
		GND			J14	
		GND			J22	
		GND			K9	
		GND			K11	
		GND			K13	
		GND			L10	
		GND			L12	
		GND			L14	
		GND			M7	
		GND			M9	
		GND			M11	
		GND			M13	
		GND			M15	
		GND			N10	
		GND			N12	
		GND			N14	
		GND			P1	
		GND			P11	
		GND			P13	
		GND			P22	
		GND			R10	
		VCCPD2			K14	
		VCCPD1			P15	
		VCCPD8			R13	
		VCCPD7			P10	
		VCCPD6			N9	
		VCCPD5			L9	
		VCCPD4			H10	
		VCCPD3			H13	

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix II device pin table for details.

(2) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix II device and should be connected on the board to configure the FPGA prototype.

(3) This NC pin is a VREF pin in the Stratix II device and should be connected to the VREF input reference voltage for the FPGA prototype. If the VREF is not used, connect pin to VCC or GND.

(4) This NC pin is a VCCD_PLL pin in the Stratix II device and should be connected to the VCCD_PLL power for the FPGA prototype.

(5) This NC pin is a VCCA_PLL pin in the Stratix II device and should be connected to the VCCA_PLL power for the FPGA prototype.

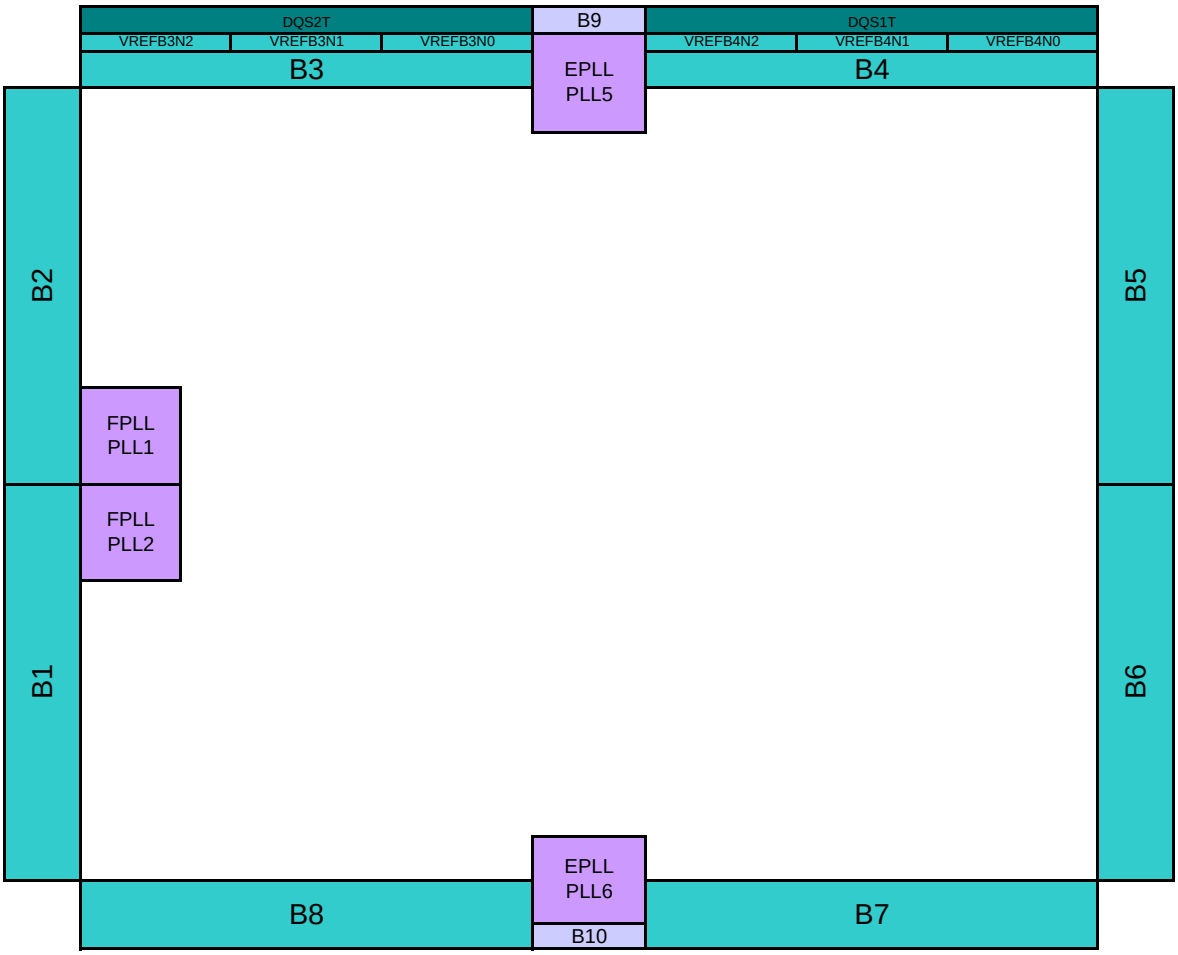
(6) This NC pin is a GNDA_PLL pin in the Stratix II device and should be connected to the GNDA_PLL ground for the FPGA prototype.

(7) This NC pin is an IO pin in the Stratix II device and can be left unconnected.

(8) This VREF pin is an IO pin in the Stratix II device and should be connected to the VREF input reference voltage for the FPGA prototype. If the VREF is not used, connect pin to VCC or GND.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HyperTransport™ technology, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards including TDO and nCEO. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCPD[1..8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers all the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, and nCE. The VCCPD pins must be connected to 3.3 V and must ramp-up from 0 V to 3.3 V within 100 ms to ensure successful configuration.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[3..4]N[0..2]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All the VREF pins within a bank are shorted together. If VREF pins are not used, designers should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p & PLL5_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 9.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p & PLL6_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 10.
VCCA_PLL[1,2,5,6]	Power	Analog power for PLLs[1,2,5,6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
VCCD_PLL[1,2,5,6]	Power	Digital power for PLLs[1,2,5,6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1,2,5,6]	Ground	Analog ground for PLLs[1,2,5,6]. All analog GND pins should be connected to the board analog GND plane.
NC	No Connect	Do not drive signals into these pins. Exceptions are the configuration pins and the pins noted in this pin list. These pins should be properly connected on the board when prototyping with the Stratix II FPGA device. Make sure to check the pin out information for the Stratix II FPGA prototype compiled design when laying out the board to ensure compatibility between the HardCopy II device and the Stratix II FPGA prototype device.
RUP4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.
RDN4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during power up. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input) and nCE. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD or ground. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
DCLK	Input	Dedicated configuration clock pin on Stratix II devices, but kept in HardCopy II for compatibility reasons. It's not required to clock this pin for HardCopy II.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy II to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Once the power up delays are done and the initialization cycle starts, CONF_DONE is released. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device initialization is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy II drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, the device enters an error state when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms. This is in addition to the Instant On delay mode chosen (i.e. instant or additional 50 ms).
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. The JTAG circuitry can be disabled by connecting TRST to GND.
	Clock and PLL Pins	
CLK[1,3,9,11]p	Clock, Input	Dedicated clock input pins 1, 3, 9, & 11 that can also be used for data inputs.
CLK[1,3,9,11]n	Clock, Input	Dedicated negative terminal clock input pins for differential clock input that can also be used for data inputs.
CLK[0,2]p/DIFFIO_RX_C[0,1]p	I/O, Clock, RX channel	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[0,2]n/DIFFIO_RX_C[0,1]n	I/O, Clock, RX channel	These pins can be used as I/O pins, the negative terminal clock input pins for differential clock input, or the negative terminal data pins of differential receiver channels.
CLK[4-8,10,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-8,10,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative terminal clock input pins for differential clock input.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
PLL5_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5).
PLL5_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL6_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6).
PLL6_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[5..6]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[5..6].
PLL[5..6]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[5..6]_FBp or negative terminal clock output pins for differential clock output.
	Optional/Dual-Purpose Configuration Pins	
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
	Dual-Purpose Differential & External Memory Interface Pins	
DIFFIO_RX[4..8,10..11,13..19,22]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[4..5,7,9,12..13,15,17..22]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[1..2]T (x8/x9) DQS[7,9,11,13]T (x4)	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1..2]T (x8/x9) DQSn[7,9,11,13]T (x4)	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.
DQ[1..2]T (x8/x9) DQ[7,9,11,13]T (x4)	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DQVLD[1..2]T (x8/x9)	I/O, DQVLD	Optional data valid signal for use in external memory interfacing.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
3. The DQ/DQS groups depicted above are in x8/x9 mode. DQ/DQS support differs across the package offerings.

Version Number	Date	Changes Made
1.0	3/27/2007	Initial revision generated to match latest Engineering pintable released 4/24/06.