Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		TDI		TDI			J29			
		TMS		TMS			N27			
		TRST		TRST			A32			
		TCK		TCK			G30			
		TDO		TDO			F30			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	K29			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	L29			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C34			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D34			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J30	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	K30	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	C31	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D31	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	M28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	N28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	C35	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	D35	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	H32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	B32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	C32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M31	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	N31	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	C33	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D33	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	M30	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	N30	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	G31	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	H31	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	M29	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	N29	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	E31	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F31	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	K31	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L31	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	E32	DQSn5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	F32	DQS5L	DQ3L/CQn3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	R28	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	T28	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	E34	DQSn6L	DQSn3L/DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	F34	DQS6L	DQS3L/CQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	R27	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	T27	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	F35	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	G35	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	J33	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	K32	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	F33	DQSn7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	G33	DQS7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	P29	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	R29	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	H35			
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	H34			
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	L32	DQ8L	DQ8L	DQ8L

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	M32	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	J35	DQSn8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	J34	DQS8L	DQ8L/CQn8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	P32	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	P31	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	K35	DQSn9L	DQSn8L/DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	K34	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	T31	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	T30	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	N34	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	N33	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	R33	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	R32	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	M34	DQSn10L	DQ9L	DQSn8L/DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	M33	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	V28	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	W28	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	L35	DQSn11L	DQSn9L/DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	L34	DQS11L	DQS9L/CQ9L	DQ8L
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	R31	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R30	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	V31	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	U31	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	W30	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	W29	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	N35	DQSn12L	DQ10L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	P34	DQS12L	DQ10L/CQn10L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	V27	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	W26	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	R35	DQSn13L	DQSn10L/DQ10L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	R34	DQS13L	DQS10L/CQ10L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	V30	DQ13L	DQ10L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	V29	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	U35	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	V34	DQ13L	DQ10L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	W33			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	W32			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	W35			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	W34			
1C	VREFB1CN0	CLK1n	CLK1n				AA35			
1C	VREFB1CN0	CLK1p	CLK1p				AB34			
2C	VREFB2CN0	CLK3p	CLK3p				AC34			
2C	VREFB2CN0	CLK3n	CLK3n				AC35			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	AF34			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	AE35			
2C	VREFB2CN0	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	AG34			
2C	VREFB2CN0	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	AG35			
2C	VREFB2CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC31	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AC32	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AB30	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	AB31	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AJ34	DQS14L	DQS17L/CQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AJ35	DQSn14L	DQSn17L/DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AB27	DQ15L	DQ17L	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AB28	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AH34	DQS15L	DQ17L/CQn17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AH35	DQSn15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	AC28	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	AC29	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AK34	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AK35	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	AG31	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AG32	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	AL34	DQS16L	DQS18L/CQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	AL35	DQSn16L	DQSn18L/DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AD28	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AD29	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29p	DIFFOUT_L57p	AH32	DQS17L	DQ18L/CQn18L	DQS19L/CQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29n	DIFFOUT_L57n	AH33	DQSn17L	DQ18L	DQSn19L/DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L29p	DIFFOUT_L58p	AE28	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L29n	DIFFOUT_L58n	AE29	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AN34	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L30n	DIFFOUT_L59n	AN35	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	AD30	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L30n	DIFFOUT_L60n	AD31	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AM34	DQS18L	DQS19L/CQ19L	DQ19L/CQn19L
2C	VREFB2CN0	IO			DIFFIO_RX_L31n	DIFFOUT_L61n	AM35	DQSn18L	DQSn19L/DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AF29	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AG30	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	AJ32	DQS19L	DQ19L/CQn19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32n	DIFFOUT_L63n	AK33	DQSn19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AE30	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AE31	DQ19L	DQ19L	DQ19L
2A	VREFB2AN0	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AN32			
2A	VREFB2AN0	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	AP33			
2A	VREFB2AN0	IO			DIFFIO_TX_L33p	DIFFOUT_L66p	AC26	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L33n	DIFFOUT_L66n	AD26	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AN33	DQS20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34n	DIFFOUT_L67n	AP34	DQSn20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AD27	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AE27	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AT34	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AR34	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AJ31	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AH30	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AT33	DQS21L	DQS24L/CQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L36n	DIFFOUT_L71n	AU33	DQSn21L	DQSn24L/DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AK32	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36n	DIFFOUT_L72n	AL32	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AP35	DQS22L	DQ24L/CQn24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	AR35	DQSn22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AG29	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AH29	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AP32	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AR32	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AK31	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AL31	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	AN30	DQS23L	DQS25L/CQ25L	DQ26L

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	AP30	DQSn23L	DQSn25L/DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	AE26	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	AF26	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AM31	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AN31	DQSn24L	DQ25L	DQSn26L/DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AK30	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AL30	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AT31	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AU31	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AG28	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AH28	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AR31	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AT30	DQSn25L	DQSn26L/DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AG27	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	AH27	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AT32	DQS26L	DQ26L/CQn26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AU32	DQSn26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AL29	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AM29	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AU34			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AV34			
2A	VREFB2AN0	IO			DIFFIO_TX_L44p	DIFFOUT_L88p	AJ29			
2A	VREFB2AN0	IO			DIFFIO_TX_L44n	DIFFOUT_L88n	AK29			
		nCONFIG		nCONFIG			AW36			
		nSTATUS		nSTATUS			AW35			
		CONF_DONE		CONF_DONE			AV35			
		PORSEL		PORSEL			AP29			
		nCE		nCE			AN29			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AD25	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AE25	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AG25	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AF25	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AE24	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AK27	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AK26	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AJ26	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AH26	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AL27	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AK25	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AJ25	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AW34	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AW33	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AW32	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AV32	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AV31	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AW31	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AW30	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AV29	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AW28	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AW27	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AW29	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AV28	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AN27	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AP27	DQ5B	DQ3B	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AN26	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AM26	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AP26	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AL25	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AR28	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AP28	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AT29	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AU29	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AU28	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AT28	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AG24			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AH24			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AU27			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AT27			
3B	VREFB3BN0	IO				DIFFOUT_B21n	AM25	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B21p	AN25	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AP24	DQSn7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AN24	DQS7B	DQ7B/CQn7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B23n	AP25	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B23p	AR25	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AU26	DQSn8B	DQSn7B/DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AT26	DQS8B	DQS7B/CQ7B	DQ7B/CQn7B
3B	VREFB3BN0	IO				DIFFOUT_B25n	AT25	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B25p	AU25	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AW26	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AV26	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B27n	AH22	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B27p	AE23	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AG22	DQSn9B	DQ8B	DQSn7B/DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AF22	DQS9B	DQ8B/CQn8B	DQS7B/CQ7B
3B	VREFB3BN0	IO				DIFFOUT_B29n	AE22	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B29p	AF23	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AL23	DQSn10B	DQSn8B/DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AK23	DQS10B	DQS8B/CQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AK24	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AJ22	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AJ23	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AH23	DQ10B	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B33n	AN23	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B33p	AM23	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AN22	DQSn11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AM22	DQS11B	DQ11B/CQn11B	
3C	VREFB3CN0	IO				DIFFOUT_B35n	AL21	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B35p	AL22	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AU24	DQSn12B	DQSn11B/DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AT24	DQS12B	DQS11B/CQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37n	AR23	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37p	AP23	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AU23	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AT23	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B39n	AG20	DQ13B		
3C	VREFB3CN0	IO				DIFFOUT_B39p	AD21	DQ13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B40n	AF20	DQSn13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B40p	AE20	DQS13B		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
3C	VREFB3CN0	IO				DIFFOUT_B41n	AE21	DQ13B		
3C	VREFB3CN0	IO				DIFFOUT_B41p	AG21	DQ13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B42n	AW25			
3C	VREFB3CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B42p	AV25			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B43n	AJ20			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B43p	AH20			
3C	VREFB3CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AW23			
3C	VREFB3CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AV23			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B45n	AP21			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B45p	AN21			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B23n	DIFFOUT_B46n	AU22			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B23p	DIFFOUT_B46p	AT22			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B47n	AW22			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B47p	AV22			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B24n	DIFFOUT_B48n	AT21			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B24p	DIFFOUT_B48p	AR22			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B25p	DIFFOUT_B49p	AW20			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B25n	DIFFOUT_B49n	AW21			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B50p	AV19			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B50n	AW19			
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B26p	DIFFOUT_B51p	AR20			
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B26n	DIFFOUT_B51n	AT20			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B52p	AN20			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B52n	AP20			
4C	VREFB4CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AU20			
4C	VREFB4CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AV20			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B54p	AH18			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B54n	AH19			
4C	VREFB4CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AT19			
4C	VREFB4CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AU19			
4C	VREFB4CN0	IO				DIFFOUT_B56p	AD19	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B56n	AG19	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AE19	DQS14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AF19	DQSn14B		
4C	VREFB4CN0	IO				DIFFOUT_B58p	AG18	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B58n	AE18	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AT18	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AU18	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60p	AT17	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60n	AW18	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AU17	DQS15B	DQS16B/CQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AV17	DQSn15B	DQSn16B/DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62p	AN19	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62n	AM19	DQ16B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32p	DIFFOUT_B63p	AN18	DQS16B	DQ16B/CQn16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32n	DIFFOUT_B63n	AP18	DQSn16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64p	AR19	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64n	AP19	DQ16B	DQ16B	
4B	VREFB4BN0	IO			DIFFIO_RX_B33p	DIFFOUT_B65p	AK17	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B33n	DIFFOUT_B65n	AL17	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B66p	AJ16	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B66n	AM17	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B67p	AK16	DQS17B	DQS19B/CQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B67n	AL16	DQSn17B	DQSn19B/DQ19B	DQ20B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
4B	VREFB4BN0	IO				DIFFOUT_B68p	AH17	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B68n	AE17	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AF17	DQS18B	DQ19B/CQn19B	DQS20B/CQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AG17	DQSn18B	DQ19B	DQSn20B/DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B70p	AH16	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B70n	AG16	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AP17	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AR17	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B72p	AN16	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B72n	AN17	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AP16	DQS19B	DQS20B/CQ20B	DQ20B/CQn20B
4B	VREFB4BN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AR16	DQSn19B	DQSn20B/DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B74p	AW16	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B74n	AT16	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AU16	DQS20B	DQ20B/CQn20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AV16	DQSn20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B76p	AU15	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B76n	AT15	DQ20B	DQ20B	DQ20B
4A	VREFB4AN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AN15			
4A	VREFB4AN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AP15			
4A	VREFB4AN0	IO				DIFFOUT_B78p	AE16			
4A	VREFB4AN0	IO				DIFFOUT_B78n	AF16			
4A	VREFB4AN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AV14	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AW14	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80p	AT14	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80n	AU14	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AV13	DQS21B	DQS24B/CQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AW13	DQSn21B	DQSn24B/DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82p	AW12	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82n	AW11	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AU11	DQS22B	DQ24B/CQn24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AV11	DQSn22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84p	AT12	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84n	AU12	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AP14	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AR14	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86p	AP13	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86n	AN14	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AR13	DQS23B	DQS25B/CQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AT13	DQSn23B	DQSn25B/DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88p	AN13	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88n	AL15	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AL13	DQS24B	DQ25B/CQn25B	DQS26B/CQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AM13	DQSn24B	DQ25B	DQSn26B/DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90p	AL14	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90n	AM14	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AJ13	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AK13	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92p	AH13	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92n	AK14	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AH14	DQS25B	DQS26B/CQ26B	DQ26B/CQn26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AJ14	DQSn25B	DQSn26B/DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94p	AG14	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94n	AG15	DQ26B	DQ26B	DQ26B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B48p	DIFFOUT_B95p	AE14	DQS26B	DQ26B/CQn26B	DQ26B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B48n	DIFFOUT_B95n	AF14	DQSn26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96p	AD15	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96n	AE15	DQ26B	DQ26B	DQ26B
		nIO_PULLUP		nIO_PULLUP			AM11			
		nCEO		nCEO			AT11			
		DCLK		DCLK			AR11			
		nCSO		nCSO			AP11			
		ASDO		ASDO			AN11			
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AM10			
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AL10			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AW7			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AV7			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AP10	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AN10	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AW8	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AV8	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AJ11	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AH11	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AU10	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AT10	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AH12	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AG12	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AW10	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AV10	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AG13	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AF13	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AU9	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AT9	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AP9	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AN9	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AU8	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AT8	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AP7	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AN7	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AR8	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AP8	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AL9	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AK9	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AU7	DQSn5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AT7	DQS5R	DQ3R/CQn3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AM8	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AL8	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AU6	DQSn6R	DQSn3R/DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AT6	DQS6R	DQS3R/CQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AJ10	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AH10	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AW4	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AV5	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AE12	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AE13	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AT5	DQSn7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AR5	DQS7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AD12	DQ7R		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AD13	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AW5			
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AW6			
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AH8	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AH9	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	AP5	DQSn8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AP6	DQS8R	DQ8R/CQn8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AK7	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AK8	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R14n	DIFFOUT_R28n	AM5	DQSn9R	DQSn8R/DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AM6	DQS9R	DQS8R/CQ8R	DQ8R/CQn8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15n	DIFFOUT_R29n	AE10	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	AE11	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R15n	DIFFOUT_R30n	AN5	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AN6	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R31n	AF10	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	AF11	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R32n	AL5	DQSn10R	DQ9R	DQSn8R/DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AL6	DQS10R	DQ9R/CQn9R	DQS8R/CQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	AG9	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	AG10	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	AK5	DQSn11R	DQSn9R/DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	AK6	DQS11R	DQS9R/CQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	AD9	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	AD10	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	AJ5	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	AJ6	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	AG7	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	AG8	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	AC8	DQSn12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	AB9	DQS12R	DQ10R/CQn10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	AB10	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	AB11	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	AH5	DQSn13R	DQSn10R/DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	AH6	DQS13R	DQS10R/CQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	AB12	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	AB13	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	AG5	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	AG6	DQ13R	DQ10R	
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	AC10			
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	AC11			
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	AE5			
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	AF6			
5C	VREFB5CN0	CLK8n	CLK8n				AC5			
5C	VREFB5CN0	CLK8p	CLK8p				AC6			
6C	VREFB6CN0	CLK10p	CLK10p				AB6			
6C	VREFB6CN0	CLK10n	CLK10n				AA5			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	W6			
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	W5			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	W12			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	W11			
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	W8	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	W7	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	V12	DQ14R	DQ17R	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	V11	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	V6	DQS14R	DQS17R/CQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	U5	DQSn14R	DQSn17R/DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	U10	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	T9	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	R6	DQS15R	DQ17R/CQn17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	R5	DQSn15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	V10	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	V9	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	R7	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	P6	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	N9	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	P8	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	N6	DQS16R	DQS18R/CQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	N5	DQSn16R	DQSn18R/DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	T10	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	R10	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	M6	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	L5	DQSn17R	DQ18R	DQSn19R/DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	R9	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	R8	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	N8	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	N7	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	M8	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	M7	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	K6	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	K5	DQSn18R	DQSn19R/DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	L8	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	L7	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	J6	DQS19R	DQ19R/CQn19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	J5	DQSn19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	K7	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	J7	DQ19R	DQ19R	DQ19R
6A	VREFB6AN0	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	G8			
6A	VREFB6AN0	IO			DIFFIO_RX_R33n	DIFFOUT_R65n	F8			
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	T13	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	T12	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	F7	DQS20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	E7	DQSn20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	H7	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	G7	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	G5	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	F5	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	R13	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	P13	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	G6	DQS21R	DQS24R/CQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	F6	DQSn21R	DQSn24R/DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	R12	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	R11	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	G9	DQS22R	DQ24R/CQn24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	F9	DQSn22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	N11	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	N10	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	F10	DQ23R	DQ25R	DQ26R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	E10	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	M10	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	L10	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	D7	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	C7	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	K9	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	J9	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	D8	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	C8	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	K8	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J8	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	D9	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	C9	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	M11	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	L11	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	D5	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	C5	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	N12	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	M12	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D10	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	C10	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	K10	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	J10	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	D6			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	C6			
6A	VREFB6AN0	IO			DIFFIO_TX_R44p	DIFFOUT_R88p	H10			
6A	VREFB6AN0	IO			DIFFIO_TX_R44n	DIFFOUT_R88n	G10			
7A	VREFB7AN0	IO				DIFFOUT_T1n	M13	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	N13	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	N14	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	P14	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	N15	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	R14	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	K13	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	L13	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	K12	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	M14	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	K14	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	L14	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	J13	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	J12	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	G13	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	H13	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	G14	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	H14	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	E13	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	F13	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	D13	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	F12	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	E14	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	F14	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	C11	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	A10	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	A11	DQSn5T	DQ3T	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	B11	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	B10	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	D11	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	C14	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	D14	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	C13	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	C12	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A13	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B13	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	J15			
7A	VREFB7AN0	IO				DIFFOUT_T19p	K15			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	A14			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	B14			
7B	VREFB7BN0	IO				DIFFOUT_T21n	G15	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T21p	E16	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	F16	DQSn7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	G16	DQS7T	DQ7T/CQn7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T23n	G17	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T23p	F15	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	C15	DQSn8T	DQSn7T/DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	D15	DQS8T	DQS7T/CQ7T	DQ7T/CQn7T
7B	VREFB7BN0	IO				DIFFOUT_T25n	A16	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T25p	D16	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	B16	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	C16	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T27n	P16	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T27p	P17	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	M16	DQSn9T	DQ8T	DQSn7T/DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	N16	DQS9T	DQ8T/CQn8T	DQS7T/CQ7T
7B	VREFB7BN0	IO				DIFFOUT_T29n	N17	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T29p	M17	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	J16	DQSn10T	DQSn8T/DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	K16	DQS10T	DQS8T/CQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T31n	K17	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T31p	L16	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	H17	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	J17	DQ10T	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T33n	C17	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T33p	F17	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	D17	DQSn11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	E17	DQS11T	DQ11T/CQn11T	
7C	VREFB7CN0	IO				DIFFOUT_T35n	C18	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T35p	D18	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	F18	DQSn12T	DQSn11T/DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	G18	DQS12T	DQS11T/CQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37n	G20	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37p	F20	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	F19	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	G19	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T39n	R18	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T39p	J18	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	A17	DQSn13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	B17	DQS13T		
7C	VREFB7CN0	IO				DIFFOUT_T41n	H19	DQ13T		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
7C	VREFB7CN0	IO				DIFFOUT_T41p	P18	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	A18			
7C	VREFB7CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	B19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T43n	M19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T43p	L19			
7C	VREFB7CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T44n	C19			
7C	VREFB7CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T44p	D19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T45n	N19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T45p	P19			
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T23n	DIFFOUT_T46n	C20			
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T23p	DIFFOUT_T46p	D20			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T47n	A19			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T47p	B20			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T24n	DIFFOUT_T48n	A20			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T24p	DIFFOUT_T48p	A21			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T25p	DIFFOUT_T49p	B22			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T25n	DIFFOUT_T49n	A22			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T50p	B23			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T50n	A23			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T26p	DIFFOUT_T51p	G21			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T26n	DIFFOUT_T51n	F21			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T52p	M20			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T52n	L20			
8C	VREFB8CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	D21			
8C	VREFB8CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	C22			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T54p	N20			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T54n	P20			
8C	VREFB8CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	A25			
8C	VREFB8CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	A24			
8C	VREFB8CN0	IO				DIFFOUT_T56p	M21	DQ14T		
8C	VREFB8CN0	IO				DIFFOUT_T56n	R20	DQ14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	D24	DQS14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	C24	DQSn14T		
8C	VREFB8CN0	IO				DIFFOUT_T58p	N21	DQ14T		
8C	VREFB8CN0	IO				DIFFOUT_T58n	M22	DQ14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	J22	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	H22	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60p	G22	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60n	K22	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	J23	DQS15T	DQS16T/CQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	H23	DQSn15T	DQSn16T/DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62p	E22	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62n	D22	DQ16T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32p	DIFFOUT_T63p	E23	DQS16T	DQ16T/CQn16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32n	DIFFOUT_T63n	D23	DQSn16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64p	G23	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64n	F23	DQ16T	DQ16T	
8B	VREFB8BN0	IO			DIFFIO_RX_T33p	DIFFOUT_T65p	K24	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T33n	DIFFOUT_T65n	J24	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T66p	M24	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T66n	J25	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T34p	DIFFOUT_T67p	L23	DQS17T	DQS19T/CQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T34n	DIFFOUT_T67n	K23	DQSn17T	DQSn19T/DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T68p	N22	DQ18T	DQ19T	DQ20T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
8B	VREFB8BN0	IO				DIFFOUT_T68n	M23	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	P23	DQS18T	DQ19T/CQn19T	DQS20T/CQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	N23	DQSn18T	DQ19T	DQSn20T/DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T70p	R22	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T70n	P22	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	G24	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	F24	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T72p	G25	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T72n	D25	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	F25	DQS19T	DQS20T/CQ20T	DQ20T/CQn20T
8B	VREFB8BN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	E25	DQSn19T	DQSn20T/DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T74p	C25	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T74n	B25	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	C26	DQS20T	DQ20T/CQn20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	B26	DQSn20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T76p	A26	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T76n	D26	DQ20T	DQ20T	DQ20T
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	G26			
8A	VREFB8AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	F26			
8A	VREFB8AN0	IO				DIFFOUT_T78p	P24			
8A	VREFB8AN0	IO				DIFFOUT_T78n	R24			
8A	VREFB8AN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	A28	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	A27	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80p	C27	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80n	D27	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	C28	DQS21T	DQS24T/CQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	B28	DQSn21T	DQSn24T/DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82p	B31	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82n	A31	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	B29	DQS22T	DQ24T/CQn24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	A29	DQSn22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84p	C29	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84n	C30	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	F28	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	E28	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86p	D28	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86n	F27	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	E29	DQS23T	DQS25T/CQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	D29	DQSn23T	DQSn25T/DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88p	G27	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88n	H26	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	H28	DQS24T	DQ25T/CQn25T	DQS26T/CQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	G28	DQSn24T	DQ25T	DQSn26T/DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90p	J26	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90n	G29	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	L26	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	K26	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92p	L25	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92n	K28	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	K27	DQS25T	DQS26T/CQ26T	DQ26T/CQn26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	J27	DQSn25T	DQSn26T/DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94p	M25	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94n	N25	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T48p	DIFFOUT_T95p	P26	DQS26T	DQ26T/CQn26T	DQ26T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T48n	DIFFOUT_T95n	N26	DQSn26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96p	P25	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96n	M27	DQ26T	DQ26T	DQ26T
QL2		GXB_TX_L11p					B36			
QL2		GXB_TX_L11n					B37			
QL2		GXB_RX_L11p					C38			
QL2		GXB_RX_L11n					C39			
QL2		GXB_TX_L10p					D36			
QL2		GXB_TX_L10n					D37			
QL2		GXB_RX_L10p					E38			
QL2		GXB_RX_L10n					E39			
QL2		GXB_CMUTX_L5p					F36			
QL2		GXB_CMUTX_L5n					F37			
QL2		REFCLK_L5p, GXB_CMURX_L5p					G38			
QL2		REFCLK_L5n, GXB_CMURX_L5n					G39			
QL2		GXB_CMUTX_L4p					H36			
QL2		GXB_CMUTX_L4n					H37			
QL2		REFCLK_L4p, GXB_CMURX_L4p					J38			
QL2		REFCLK_L4n, GXB_CMURX_L4n					J39			
QL2		GXB_TX_L9p					K36			
QL2		GXB_TX_L9n					K37			
QL2		GXB_RX_L9p					L38			
QL2		GXB_RX_L9n					L39			
QL2		GXB_TX_L8p					M36			
QL2		GXB_TX_L8n					M37			
QL2		GXB_RX_L8p					N38			
QL2		GXB_RX_L8n					N39			
QL1		GXB_TX_L7p					P36			
QL1		GXB_TX_L7n					P37			
QL1		GXB_RX_L7p					R38			
QL1		GXB_RX_L7n					R39			
QL1		GXB_TX_L6p					T36			
QL1		GXB_TX_L6n					T37			
QL1		GXB_RX_L6p					U38			
QL1		GXB_RX_L6n					U39			
QL1		GXB_CMUTX_L3p					V36			
QL1		GXB_CMUTX_L3n					V37			
QL1		REFCLK_L3p, GXB_CMURX_L3p					W38			
QL1		REFCLK_L3n, GXB_CMURX_L3n					W39			
QL1		GXB_CMUTX_L2p					Y36			
QL1		GXB_CMUTX_L2n					Y37			
QL1		REFCLK_L2p, GXB_CMURX_L2p					AA38			
QL1		REFCLK_L2n, GXB_CMURX_L2n					AA39			
QL1		GXB_TX_L5p					AB36			
QL1		GXB_TX_L5n					AB37			
QL1		GXB_RX_L5p					AC38			
QL1		GXB_RX_L5n					AC39			
QL1		GXB_TX_L4p					AD36			
QL1		GXB_TX_L4n					AD37			
QL1		GXB_RX_L4p					AE38			
QL1		GXB_RX_L4n					AE39			
QL0		GXB_TX_L3p					AF36			
QL0		GXB_TX_L3n					AF37			
QL0		GXB_RX_L3p					AG38			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
QL0		GXB_RX_L3n					AG39			
QL0		GXB_TX_L2p					AH36			
QL0		GXB_TX_L2n					AH37			
QL0		GXB_RX_L2p					AJ38			
QL0		GXB_RX_L2n					AJ39			
QL0		GXB_CMUTX_L1p					AK36			
QL0		GXB_CMUTX_L1n					AK37			
QL0		REFCLK_L1p, GXB_CMURX_L1p					AL38			
QL0		REFCLK_L1n, GXB_CMURX_L1n					AL39			
QL0		GXB_CMUTX_L0p					AM36			
QL0		GXB_CMUTX_L0n					AM37			
QL0		REFCLK_L0p, GXB_CMURX_L0p					AN38			
QL0		REFCLK_L0n, GXB_CMURX_L0n					AN39			
QL0		GXB_TX_L1p					AP36			
QL0		GXB_TX_L1n					AP37			
QL0		GXB_RX_L1p					AR38			
QL0		GXB_RX_L1n					AR39			
QL0		GXB_TX_L0p					AT36			
QL0		GXB_TX_L0n					AT37			
QL0		GXB_RX_L0p					AU38			
QL0		GXB_RX_L0n					AU39			
QR0		GXB_RX_R0n					AU1			
QR0		GXB_RX_R0p					AU2			
QR0		GXB_TX_R0n					AT3			
QR0		GXB_TX_R0p					AT4			
QR0		GXB_RX_R1n					AR1			
QR0		GXB_RX_R1p					AR2			
QR0		GXB_TX_R1n					AP3			
QR0		GXB_TX_R1p					AP4			
QR0		REFCLK_R0n, GXB_CMURX_R0n					AN1			
QR0		REFCLK_R0p, GXB_CMURX_R0p					AN2			
QR0		GXB_CMUTX_R0n					AM3			
QR0		GXB_CMUTX_R0p					AM4			
QR0		REFCLK_R1n, GXB_CMURX_R1n					AL1			
QR0		REFCLK_R1p, GXB_CMURX_R1p					AL2			
QR0		GXB_CMUTX_R1n					AK3			
QR0		GXB_CMUTX_R1p					AK4			
QR0		GXB_RX_R2n					AJ1			
QR0		GXB_RX_R2p					AJ2			
QR0		GXB_TX_R2n					AH3			
QR0		GXB_TX_R2p					AH4			
QR0		GXB_RX_R3n					AG1			
QR0		GXB_RX_R3p					AG2			
QR0		GXB_TX_R3n					AF3			
QR0		GXB_TX_R3p					AF4			
QR1		GXB_RX_R4n					AE1			
QR1		GXB_RX_R4p					AE2			
QR1		GXB_TX_R4n					AD3			
QR1		GXB_TX_R4p					AD4			
QR1		GXB_RX_R5n					AC1			
QR1		GXB_RX_R5p					AC2			
QR1		GXB_TX_R5n					AB3			
QR1		GXB_TX_R5p					AB4			
QR1		REFCLK_R2n, GXB_CMURX_R2n					AA1			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
QR1		REFCLK_R2p, GXB_CMURX_R2p					AA2			
QR1		GXB_CMUTX_R2n					Y3			
QR1		GXB_CMUTX_R2p					Y4			
QR1		REFCLK_R3n, GXB_CMURX_R3n					W1			
QR1		REFCLK_R3p, GXB_CMURX_R3p					W2			
QR1		GXB_CMUTX_R3n					V3			
QR1		GXB_CMUTX_R3p					V4			
QR1		GXB_RX_R6n					U1			
QR1		GXB_RX_R6p					U2			
QR1		GXB_TX_R6n					T3			
QR1		GXB_TX_R6p					T4			
QR1		GXB_RX_R7n					R1			
QR1		GXB_RX_R7p					R2			
QR1		GXB_TX_R7n					P3			
QR1		GXB_TX_R7p					P4			
QR2		GXB_RX_R8n					N1			
QR2		GXB_RX_R8p					N2			
QR2		GXB_TX_R8n					M3			
QR2		GXB_TX_R8p					M4			
QR2		GXB_RX_R9n					L1			
QR2		GXB_RX_R9p					L2			
QR2		GXB_TX_R9n					K3			
QR2		GXB_TX_R9p					K4			
QR2		REFCLK_R4n, GXB_CMURX_R4n					J1			
QR2		REFCLK_R4p, GXB_CMURX_R4p					J2			
QR2		GXB_CMUTX_R4n					H3			
QR2		GXB_CMUTX_R4p					H4			
QR2		REFCLK_R5n, GXB_CMURX_R5n					G1			
QR2		REFCLK_R5p, GXB_CMURX_R5p					G2			
QR2		GXB_CMUTX_R5n					F3			
QR2		GXB_CMUTX_R5p					F4			
QR2		GXB_RX_R10n					E1			
QR2		GXB_RX_R10p					E2			
QR2		GXB_TX_R10n					D3			
QR2		GXB_TX_R10p					D4			
QR2		GXB_RX_R11n					C1			
QR2		GXB_RX_R11p					C2			
QR2		GXB_TX_R11n					B3			
QR2		GXB_TX_R11p					B4			
		GND					T25			
		GND					AL11			
		GND					Y21			
		GND					B27			
		GND					AV6			
		GND					AV9			
		GND					AV12			
		GND					AV15			
		GND					AV18			
		GND					AV21			
		GND					AV24			
		GND					AV27			
		GND					AV30			
		GND					AV33			
		GND					AR6			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		GND					AR9			
		GND					AR12			
		GND					AR15			
		GND					AR18			
		GND					AR21			
		GND					AR24			
		GND					AR27			
		GND					AR30			
		GND					AR33			
		GND					AM7			
		GND					AM9			
		GND					AM12			
		GND					AM15			
		GND					AM18			
		GND					AM21			
		GND					AM24			
		GND					AM27			
		GND					AM30			
		GND					AM33			
		GND					AJ7			
		GND					AJ9			
		GND					AJ12			
		GND					AJ15			
		GND					AJ18			
		GND					AJ21			
		GND					AJ24			
		GND					AJ27			
		GND					AJ30			
		GND					AJ33			
		GND					AF9			
		GND					AF12			
		GND					AF15			
		GND					AF18			
		GND					AF21			
		GND					AF24			
		GND					AF27			
		GND					AF30			
		GND					AD23			
		GND					AC7			
		GND					AC9			
		GND					AC12			
		GND					AC14			
		GND					AC16			
		GND					AC18			
		GND					AC20			
		GND					AC22			
		GND					AC24			
		GND					AC27			
		GND					AC30			
		GND					AC33			
		GND					AB15			
		GND					AB17			
		GND					AB19			
		GND					AB21			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		GND					AB23			
		GND					AB25			
		GND					AA14			
		GND					AA16			
		GND					AA18			
		GND					AA22			
		GND					AA24			
		GND					Y12			
		GND					Y15			
		GND					Y17			
		GND					Y19			
		GND					Y23			
		GND					Y25			
		GND					Y27			
		GND					Y30			
		GND					W10			
		GND					W14			
		GND					W16			
		GND					W18			
		GND					W20			
		GND					W22			
		GND					W24			
		GND					V15			
		GND					V17			
		GND					V19			
		GND					V21			
		GND					V23			
		GND					V25			
		GND					U9			
		GND					U12			
		GND					U14			
		GND					U16			
		GND					U18			
		GND					U20			
		GND					U22			
		GND					U24			
		GND					U26			
		GND					U28			
		GND					U30			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					T21			
		GND					T23			
		GND					P7			
		GND					P9			
		GND					P12			
		GND					P15			
		GND					P21			
		GND					P27			
		GND					P30			
		GND					P33			
		GND					N18			
		GND					N24			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		GND					L6			
		GND					L9			
		GND					L12			
		GND					L15			
		GND					L18			
		GND					L21			
		GND					L24			
		GND					L27			
		GND					L30			
		GND					L33			
		GND					H6			
		GND					H9			
		GND					H12			
		GND					H15			
		GND					H18			
		GND					H21			
		GND					H24			
		GND					H27			
		GND					H30			
		GND					H33			
		GND					E6			
		GND					E9			
		GND					E12			
		GND					E15			
		GND					E18			
		GND					E21			
		GND					E24			
		GND					E27			
		GND					E30			
		GND					E33			
		GND					B9			
		GND					B12			
		GND					B15			
		GND					B18			
		GND					B21			
		GND					B24			
		GND					B30			
		GND					A38			
		GND					A37			
		GND					A36			
		GND					A35			
		GND					A33			
		GND					B39			
		GND					B38			
		GND					B35			
		GND					B34			
		GND					B33			
		GND					C37			
		GND					C36			
		GND					D39			
		GND					D38			
		GND					E37			
		GND					E36			
		GND					F39			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		GND					T34			
		GND					AW37			
		GND					AV37			
		GND					AV38			
		GND					AV39			
		GND					AU36			
		GND					AU37			
		GND					AT38			
		GND					AT39			
		GND					AR36			
		GND					AR37			
		GND					AP38			
		GND					AP39			
		GND					AN36			
		GND					AN37			
		GND					AM38			
		GND					AM39			
		GND					AL36			
		GND					AL37			
		GND					AK38			
		GND					AK39			
		GND					AJ36			
		GND					AJ37			
		GND					AH38			
		GND					AH39			
		GND					AG36			
		GND					AG37			
		GND					AF33			
		GND					AF38			
		GND					AF39			
		GND					AE36			
		GND					AE37			
		GND					AD32			
		GND					AD34			
		GND					AD38			
		GND					AD39			
		GND					AC36			
		GND					AC37			
		GND					AB33			
		GND					AB38			
		GND					AB39			
		GND					AA36			
		GND					AA37			
		GND					Y32			
		GND					Y34			
		GND					Y38			
		GND					Y39			
		GND					W36			
		GND					W37			
		GND					V33			
		GND					V38			
		GND					V39			
		GND					U36			
		GND					U37			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					T32			
		GND					T38			
		GND					T39			
		GND					R36			
		GND					R37			
		GND					P38			
		GND					P39			
		GND					N36			
		GND					N37			
		GND					M38			
		GND					M39			
		GND					L36			
		GND					L37			
		GND					K38			
		GND					K39			
		GND					J36			
		GND					J37			
		GND					H38			
		GND					H39			
		GND					G36			
		GND					G37			
		GND					F38			
		GND					A7			
		GND					A5			
		GND					A4			
		GND					A3			
		GND					A2			
		GND					B7			
		GND					B6			
		GND					B5			
		GND					B2			
		GND					B1			
		GND					C4			
		GND					C3			
		GND					D2			
		GND					D1			
		GND					E4			
		GND					E3			
		GND					F2			
		GND					T8			
		GND					AW3			
		GND					AV1			
		GND					AV2			
		GND					AV3			
		GND					AU3			
		GND					AU4			
		GND					AT1			
		GND					AT2			
		GND					AR3			
		GND					AR4			
		GND					AP1			
		GND					AP2			
		GND					AN3			
		GND					AN4			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		GND					AM1			
		GND					AM2			
		GND					AL3			
		GND					AL4			
		GND					AK1			
		GND					AK2			
		GND					AJ3			
		GND					AJ4			
		GND					AH1			
		GND					AH2			
		GND					AG3			
		GND					AG4			
		GND					AF1			
		GND					AF2			
		GND					AF7			
		GND					AE3			
		GND					AE4			
		GND					AD1			
		GND					AD2			
		GND					AD6			
		GND					AD8			
		GND					AC3			
		GND					AC4			
		GND					AB1			
		GND					AB2			
		GND					AB7			
		GND					AA3			
		GND					AA4			
		GND					Y1			
		GND					Y2			
		GND					Y6			
		GND					Y8			
		GND					W3			
		GND					W4			
		GND					V1			
		GND					V2			
		GND					V7			
		GND					U3			
		GND					U4			
		GND					T1			
		GND					T2			
		GND					T6			
		GND					R3			
		GND					R4			
		GND					P1			
		GND					P2			
		GND					N3			
		GND					N4			
		GND					M1			
		GND					M2			
		GND					L3			
		GND					L4			
		GND					K1			
		GND					K2			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		GND					J3			
		GND					J4			
		GND					H1			
		GND					H2			
		GND					G3			
		GND					G4			
		GND					F1			
		VCC					Y20			
		VCC					AC15			
		VCC					AC17			
		VCC					AC19			
		VCC					AC21			
		VCC					AC23			
		VCC					AC25			
		VCC					AB14			
		VCC					AB16			
		VCC					AB18			
		VCC					AB20			
		VCC					AB22			
		VCC					AB24			
		VCC					AA15			
		VCC					AA17			
		VCC					AA19			
		VCC					AA21			
		VCC					AA23			
		VCC					AA25			
		VCC					Y14			
		VCC					Y16			
		VCC					Y18			
		VCC					Y22			
		VCC					Y24			
		VCC					W15			
		VCC					W17			
		VCC					W19			
		VCC					W21			
		VCC					W23			
		VCC					W25			
		VCC					V14			
		VCC					V16			
		VCC					V18			
		VCC					V20			
		VCC					V22			
		VCC					V24			
		VCC					V26			
		VCC					U15			
		VCC					U17			
		VCC					U19			
		VCC					U21			
		VCC					U23			
		VCC					U25			
		VCC					T14			
		VCC					T16			
		VCC					T18			
		VCC					T20			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		VCC					T22			
		VCC					T24			
		VCC					T26			
		VCC					AE32			
		VCC					AF32			
		VCC					AB32			
		VCC					AA32			
		VCC					V32			
		VCC					U32			
		VCC					AF8			
		VCC					AE8			
		VCC					AB8			
		VCC					AA8			
		VCC					V8			
		VCC					U8			
		VCCPGM					AK28			
		VCCPGM					AK12			
		TEMPDIODEn					E11			
		TEMPDIODEp					A9			
		VCC_CLKIN3C					AK21			
		VCC_CLKIN4C					AK18			
		VCC_CLKIN7C					K18			
		VCC_CLKIN8C					K21			
		VCCA_PLL_B1					AL20			
		VCCA_PLL_B2					AL19			
		VCCA_PLL_L2					Y29			
		VCCA_PLL_L3					AA29			
		VCCA_PLL_R2					Y10			
		VCCA_PLL_R3					AA10			
		VCCA_PLL_T1					J20			
		VCCA_PLL_T2					J19			
		VCCD_PLL_B1					AK20			
		VCCD_PLL_B2					AK19			
		VCCD_PLL_L2					Y28			
		VCCD_PLL_L3					AA28			
		VCCD_PLL_R2					Y11			
		VCCD_PLL_R3					AA11			
		VCCD_PLL_T1					K20			
		VCCD_PLL_T2					K19			
		VCCIO1A					E35			
		VCCIO1A					J31			
		VCCIO1A					G32			
		VCCIO1A					G34			
		VCCIO1A					D32			
		VCCIO1C					K33			
		VCCIO1C					AA30			
		VCCIO1C					T29			
		VCCIO1C					N32			
		VCCIO2A					AJ28			
		VCCIO2A					AT35			
		VCCIO2A					AP31			
		VCCIO2A					AM32			
		VCCIO2A					AG26			
		VCCIO2C					AF31			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		VCCIO2C					AL33			
		VCCIO2C					AH31			
		VCCIO2C					AG33			
		VCCIO3A					AH25			
		VCCIO3A					AU30			
		VCCIO3A					AR29			
		VCCIO3A					AL26			
		VCCIO3B					AG23			
		VCCIO3B					AR26			
		VCCIO3C					AH21			
		VCCIO3C					AW24			
		VCCIO3C					AK22			
		VCCIO4A					AH15			
		VCCIO4A					AU13			
		VCCIO4A					AP12			
		VCCIO4A					AK15			
		VCCIO4B					AJ17			
		VCCIO4B					AW15			
		VCCIO4C					AJ19			
		VCCIO4C					AW17			
		VCCIO4C					AU21			
		VCCIO5A					AK10			
		VCCIO5A					AW9			
		VCCIO5A					AR7			
		VCCIO5A					AR10			
		VCCIO5A					AN8			
		VCCIO5C					AE9			
		VCCIO5C					AL7			
		VCCIO5C					AJ8			
		VCCIO5C					AH7			
		VCCIO6A					B8			
		VCCIO6A					M9			
		VCCIO6A					H8			
		VCCIO6A					E5			
		VCCIO6A					E8			
		VCCIO6C					H5			
		VCCIO6C					V13			
		VCCIO6C					T11			
		VCCIO6C					P10			
		VCCIO7A					A12			
		VCCIO7A					M15			
		VCCIO7A					J14			
		VCCIO7A					D12			
		VCCIO7B					A15			
		VCCIO7B					L17			
		VCCIO7C					C21			
		VCCIO7C					M18			
		VCCIO7C					E19			
		VCCIO8A					A30			
		VCCIO8A					M26			
		VCCIO8A					J28			
		VCCIO8A					D30			
		VCCIO8B					E26			
		VCCIO8B					K25			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		VCCIO8C					C23			
		VCCIO8C					L22			
		VCCIO8C					F22			
		VCCPD1A					U27			
		VCCPD1C					W27			
		VCCPD2A					AB26			
		VCCPD2C					Y26			
		VCCPD3A					AD24			
		VCCPD3B					AD22			
		VCCPD3C					AD20			
		VCCPD4A					AD14			
		VCCPD4B					AD16			
		VCCPD4C					AD18			
		VCCPD5A					AC13			
		VCCPD5C					AA13			
		VCCPD6A					U13			
		VCCPD6C					W13			
		VCCPD7A					R15			
		VCCPD7B					R17			
		VCCPD7C					R19			
		VCCPD8A					R25			
		VCCPD8B					R23			
		VCCPD8C					R21			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				P28			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				U29			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AF28			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				AB29			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AN28			
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AL24			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AP22			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AN12			
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AM16			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AL18			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AG11			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AD11			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				P11			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				U11			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G12			
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H16			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				E20			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				F29			
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				H25			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				J21			
		NC					L28			
		NC					AM28			
		NC					AK11			
		NC					F11			
		NC					AV36			
		NC					AU35			
		NC					AU5			
		NC					AV4			
		NC					AD17			
		NC					R16			
		NC					R26			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		NC *(3)*		MSEL2			A8			
		NC *(3)*		MSEL1			H11			
		NC *(3)*		MSEL0			J11			
		NC *(4)*					K11			
		NC *(5)*					AA27			
		NC *(5)*					AA26			
		NC *(5)*					AM20			
		NC *(5)*					AA12			
		NC *(5)*					Y13			
		NC *(5)*					H20			
		NC *(6)*					AA20			
		VCCAUX					H29			
		VCCAUX					AL28			
		VCCAUX					AL12			
		VCCAUX					G11			
		VCCA_L					AF35			
		VCCA_L					M35			
		VCCA_R					AF5			
		VCCA_R					M5			
		VCCH_GXBL0					AE34			
		VCCH_GXBL1					AA34			
		VCCH_GXBL2					U34			
		VCCH_GXBR0					AE6			
		VCCH_GXBR1					AA6			
		VCCH_GXBR2					U6			
		VCCL_GXBL0					AE33			
		VCCL_GXBL0					AD33			
		VCCL_GXBL1					Y33			
		VCCL_GXBL1					AA33			
		VCCL_GXBL2					T33			
		VCCL_GXBL2					U33			
		VCCL_GXBR0					AD7			
		VCCL_GXBR0					AE7			
		VCCL_GXBR1					AA7			
		VCCL_GXBR1					Y7			
		VCCL_GXBR2					U7			
		VCCL_GXBR2					T7			
		VCCR_R					Y5			
		VCCR_R					AD5			
		VCCR_R					T5			
		VCCR_L					Y35			
		VCCR_L					AD35			
		VCCR_L					T35			
		VCCT_R					V5			
		VCCT_R					AB5			
		VCCT_R					P5			
		VCCT_L					V35			
		VCCT_L					AB35			
		VCCT_L					P35			
		VCCHIP_R					Y9			
		VCCHIP_R					AA9			
		VCCHIP_R					W9			
		VCCHIP_L					Y31			
		VCCHIP_L					AA31			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)
		VCCHIP_L					W31			
		RREF_L0					AW38			
		RREF_L1					A34			
		RREF_R0					AW2			
		RREF_R1					A6			

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Strati IV device pin table for details.
(2) The individual index number of the pin in this column may not be the same as its companion Stratix IV device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.
(6) This NC pin is a DNU pin in the Stratix IV device and must be left floating.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Clock and PLL Pins		
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, ,L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin fo HardCopy IV.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

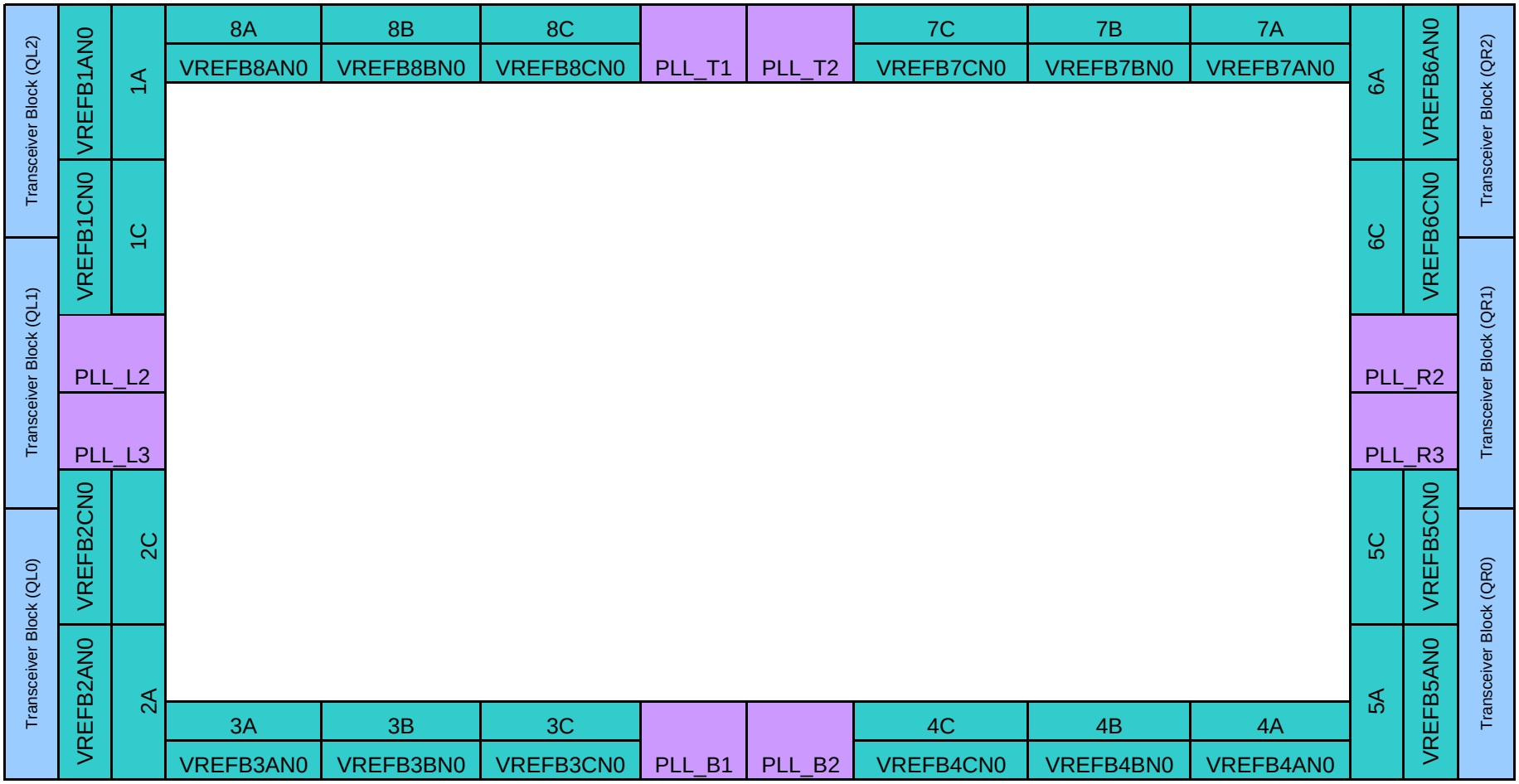
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), 3.0V PCI/PCI-X and LVTTL 3.3V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
VREFB[1:8][A,C]N0, VREFB[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
Transceiver (I/O Banks) Pins		
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p GXB_CMURX_[L,R][0:7]p	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n GXB_CMURX_[L,R][0:7]n	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC4GX35. Refer to the pin list for the availability of pins in each density.

(2) Refer to HardCopy IV Pin Connections Guidelines and Datasheet for the recommended operating voltage.



Notes:
1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	4/30/2010	Initial release.