Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		TDI		TDI			C29			
		TMS		TMS			A33			
		TRST		TRST			B34			
		TCK		TCK			B33			
		TDO		TDO			E29			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	K26			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	L26			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	F30			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	F29			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J27	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	J26	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	D30	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D29	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	G28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	G27	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	G30	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	G29	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	K28	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	K27	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	H30	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	H29	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M28	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	L27	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	J30	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	J29	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	M26	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	N26	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	K30	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	K29	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	M29	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	N28	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	L30	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	L29	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	P26	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	R26	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	M30	DQSn5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	N29	DQS5L	DQ3L/CQn3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	N25	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	N24	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	R25	DQSn6L	DQSn3L/DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	P24	DQS6L	DQS3L/CQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	U27	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	U26	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	T30	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	T29	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	U25	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	V24	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	U29	DQSn7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	U28	DQS7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	T24	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	U24	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	V28			
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	V27			
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	W24	DQ8L	DQ8L	DQ8L

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	Y24	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	V30	DQSn8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	V29	DQS8L	DQ8L/CQn8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	AA26	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	Y25	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	AB30	DQSn9L	DQSn8L/DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	AA29	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	AB26	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	AB25	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	AB29	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	AC29	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	AC25	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	AC24	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	AC28	DQSn10L	DQ9L	DQSn8L/DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	AB27	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	AF27	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	AE26	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	AH30	DQSn11L	DQSn9L/DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	AG29	DQS11L	DQS9L/CQ9L	DQ8L
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	AH28	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	AG27	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	AJ30	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	AH29	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	AC27	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	AC26	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	AG30	DQSn12L	DQ10L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	AF29	DQS12L	DQ10L/CQn10L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	AD27	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	AE27	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	AE30	DQSn13L	DQSn10L/DQ10L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	AE29	DQS13L	DQS10L/CQ10L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	AE28	DQ13L	DQ10L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	AF28	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	AD30	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	AD29	DQ13L	DQ10L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	AK30			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	AJ29			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	AL30			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	AK29			
1C	VREFB1CN0	CLK1n	CLK1n				AM34			
1C	VREFB1CN0	CLK1p	CLK1p				AM33			
		nCONFIG		nCONFIG			AL31			
		nSTATUS		nSTATUS			AL32			
		CONF_DONE		CONF_DONE			AK32			
		PORSEL		PORSEL			AP33			
		nCE		nCE			AN33			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AM31	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AP32	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AP31	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AP30	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AN32	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AN30	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AP29	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AN29	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
3A	VREFB3AN0	IO				DIFFOUT_B5n	AP28	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AP26	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AP27	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AN27	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AM29	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AM30	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AN26	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AM26	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AL28	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AM28	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AM25	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AL25	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AL27	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AL26	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AK27	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AJ27	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AF23	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AH25	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AK26	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AJ26	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AF24	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AF26	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AF25	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AE25	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AH24	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AG26	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AD24	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AC23	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AE23			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AD23			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AC22			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AB23			
3B	VREFB3BN0	IO				DIFFOUT_B21n	AP25	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B21p	AP24	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AN24	DQSn7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AN23	DQS7B	DQ7B/CQn7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B23n	AL24	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B23p	AM23	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AL23	DQSn8B	DQSn7B/DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AK23	DQS8B	DQS7B/CQ7B	DQ7B/CQn7B
3B	VREFB3BN0	IO				DIFFOUT_B25n	AJ23	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B25p	AJ22	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AK24	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AJ24	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B27n	AG24	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B27p	AG23	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AH22	DQSn9B	DQ8B	DQSn7B/DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AH21	DQS9B	DQ8B/CQn8B	DQS7B/CQ7B
3B	VREFB3BN0	IO				DIFFOUT_B29n	AE20	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B29p	AE22	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AF22	DQSn10B	DQSn8B/DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AF21	DQS10B	DQS8B/CQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AD21	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AC21	DQ10B	DQ8B	DQ7B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AD20	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AC20	DQ10B	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B33n	AP22	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B33p	AP23	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AM22	DQSn11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AL22	DQS11B	DQ11B/CQn11B	
3C	VREFB3CN0	IO				DIFFOUT_B35n	AM20	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B35p	AL20	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AM21	DQSn12B	DQSn11B/DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AL21	DQS12B	DQS11B/CQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37n	AM19	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37p	AL19	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AP21	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AN21	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B39n	AK21	DQ13B		
3C	VREFB3CN0	IO				DIFFOUT_B39p	AK20	DQ13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B40n	AJ19	DQSn13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B40p	AH19	DQS13B		
3C	VREFB3CN0	IO				DIFFOUT_B41n	AJ20	DQ13B		
3C	VREFB3CN0	IO				DIFFOUT_B41p	AK18	DQ13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B42n	AF20			
3C	VREFB3CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B42p	AF19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B43n	AE19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B43p	AC19			
3C	VREFB3CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AG21			
3C	VREFB3CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AG20			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B45n	AD18			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B45p	AC18			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B23n	DIFFOUT_B46n	AM18			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B23p	DIFFOUT_B46p	AL18			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B47n	AP20			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B47p	AN20			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B24n	DIFFOUT_B48n	AP18			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B24p	DIFFOUT_B48p	AN18			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B25p	DIFFOUT_B49p	AN17			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B25n	DIFFOUT_B49n	AP17			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B50p	AN15			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B50n	AP15			
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B26p	DIFFOUT_B51p	AL17			
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B26n	DIFFOUT_B51n	AM17			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B52p	AC17			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B52n	AD17			
4C	VREFB4CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AG15			
4C	VREFB4CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AH16			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B54p	AE16			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B54n	AC16			
4C	VREFB4CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AF15			
4C	VREFB4CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AF16			
4C	VREFB4CN0	IO				DIFFOUT_B56p	AJ15	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B56n	AK17	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AJ16	DQS14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AJ17	DQSn14B		
4C	VREFB4CN0	IO				DIFFOUT_B58p	AK14	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B58n	AK15	DQ14B		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
4C	VREFB4CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AN14	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AP14	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60p	AM16	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60n	AL16	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AL14	DQS15B	DQS16B/CQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AM14	DQSn15B	DQSn16B/DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62p	AM15	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62n	AL15	DQ16B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32p	DIFFOUT_B63p	AL13	DQS16B	DQ16B/CQn16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32n	DIFFOUT_B63n	AM13	DQSn16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64p	AP13	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64n	AP12	DQ16B	DQ16B	
4B	VREFB4BN0	IO			DIFFIO_RX_B33p	DIFFOUT_B65p	AC15	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B33n	DIFFOUT_B65n	AD15	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B66p	AD14	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B66n	AC14	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B67p	AF13	DQS17B	DQS19B/CQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B67n	AF14	DQSn17B	DQSn19B/DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B68p	AE15	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B68n	AE13	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AG14	DQS18B	DQ19B/CQn19B	DQS20B/CQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AH14	DQSn18B	DQ19B	DQSn20B/DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B70p	AG12	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B70n	AH13	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AJ11	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AK11	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B72p	AJ12	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B72n	AJ13	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AK12	DQS19B	DQS20B/CQ20B	DQ20B/CQn20B
4B	VREFB4BN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AL12	DQSn19B	DQSn20B/DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B74p	AL11	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B74n	AM12	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AN11	DQS20B	DQ20B/CQn20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AN12	DQSn20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B76p	AP10	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B76n	AP11	DQ20B	DQ20B	DQ20B
4A	VREFB4AN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AC12			
4A	VREFB4AN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AC13			
4A	VREFB4AN0	IO				DIFFOUT_B78p	AD11			
4A	VREFB4AN0	IO				DIFFOUT_B78n	AB12			
4A	VREFB4AN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AH10	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AH11	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80p	AE12	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80n	AD12	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AE10	DQS21B	DQS24B/CQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AF10	DQSn21B	DQSn24B/DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82p	AF11	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82n	AG9	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AJ9	DQS22B	DQ24B/CQn24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AK9	DQSn22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84p	AF12	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84n	AG11	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AJ8	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AK8	DQ23B	DQ25B	DQ26B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
4A	VREFB4AN0	IO				DIFFOUT_B86p	AL8	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86n	AL9	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AL10	DQS23B	DQS25B/CQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AM10	DQSn23B	DQSn25B/DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88p	AL7	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88n	AM7	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AM9	DQS24B	DQ25B/CQn25B	DQS26B/CQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AN9	DQSn24B	DQ25B	DQSn26B/DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90p	AM6	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90n	AM5	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AN8	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AP8	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92p	AP7	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92n	AP9	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AN6	DQS25B	DQS26B/CQ26B	DQ26B/CQn26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AP6	DQSn25B	DQSn26B/DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94p	AN3	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94n	AN5	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B48p	DIFFOUT_B95p	AP4	DQS26B	DQ26B/CQn26B	DQ26B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B48n	DIFFOUT_B95n	AP5	DQSn26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96p	AM4	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96n	AP3	DQ26B	DQ26B	DQ26B
		nIO_PULLUP		nIO_PULLUP			AP2			
		nCEO		nCEO			AK3			
		DCLK		DCLK			AL3			
		nCSO		nCSO			AL4			
		ASDO		ASDO			AN1			
6C	VREFB6CN0	CLK10p	CLK10p				AM2			
6C	VREFB6CN0	CLK10n	CLK10n				AM1			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	AK6			
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	AL5			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	AJ6			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	AK5			
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	AD6	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	AD5	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	AE7	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	AF7	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	AE6	DQS14R	DQS17R/CQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	AE5	DQSn14R	DQSn17R/DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	AD8	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	AE8	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	AF6	DQS15R	DQ17R/CQn17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	AG5	DQSn15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	AC9	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	AC8	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	AG6	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	AH5	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	AG8	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	AH7	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	AH6	DQS16R	DQS18R/CQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	AJ5	DQSn16R	DQSn18R/DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	AE9	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	AF8	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	AB8	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
6C	VREFB6CN0	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	AC7	DQSn17R	DQ18R	DQSn19R/DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	AC11	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	AC10	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	AB6	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	AC6	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	AB10	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	AB9	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	AA6	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	AB5	DQSn18R	DQSn19R/DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	Y10	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	AA9	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	V6	DQS19R	DQ19R/CQn19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	V5	DQSn19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	W11	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	Y11	DQ19R	DQ19R	DQ19R
6A	VREFB6AN0	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	V8			
6A	VREFB6AN0	IO			DIFFIO_RX_R33n	DIFFOUT_R65n	V7			
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	T11	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	U11	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	U7	DQS20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	U6	DQSn20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	V11	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	U10	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	T6	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	T5	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	U9	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	U8	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	P11	DQS21R	DQS24R/CQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	R10	DQSn21R	DQSn24R/DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	N11	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	N10	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	N6	DQS22R	DQ24R/CQn24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	M5	DQSn22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	P9	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	R9	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	L6	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	L5	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	N7	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	M6	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	K6	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	K5	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	M9	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	N9	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	J6	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	J5	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	L8	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	M7	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	H6	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	H5	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	K8	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	K7	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	G6	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	G5	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	G8	DQ26R	DQ26R	DQ26R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	G7	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D6	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	D5	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	J9	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	J8	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	F6			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	F5			
6A	VREFB6AN0	IO			DIFFIO_TX_R44p	DIFFOUT_R88p	K9			
6A	VREFB6AN0	IO			DIFFIO_TX_R44n	DIFFOUT_R88n	L9			
7A	VREFB7AN0	IO				DIFFOUT_T1n	A3	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C4	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A4	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	A5	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	B5	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B3	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	A6	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	B6	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	A9	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	A7	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	A8	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	B8	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	C7	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	D7	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	B9	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	C9	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	F8	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	E8	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	C10	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	D10	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	E9	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	F9	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	D8	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	D9	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	H11	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	J12	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	G10	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	G11	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	H9	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	J11	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	J10	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	K10	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	M12	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	K12	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	L11	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	M11	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	M13			
7A	VREFB7AN0	IO				DIFFOUT_T19p	L12			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	N12			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	P12			
7B	VREFB7BN0	IO				DIFFOUT_T21n	A11	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T21p	A10	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	B11	DQSn7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	B12	DQS7T	DQ7T/CQn7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T23n	C12	DQ7T	DQ7T	DQ7T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
7B	VREFB7BN0	IO				DIFFOUT_T23p	D11	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	D12	DQSn8T	DQSn7T/DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	E12	DQS8T	DQS7T/CQ7T	DQ7T/CQn7T
7B	VREFB7BN0	IO				DIFFOUT_T25n	F13	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T25p	F12	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	E11	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	F11	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T27n	G13	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T27p	H12	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	G14	DQSn9T	DQ8T	DQSn7T/DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	H14	DQS9T	DQ8T/CQn8T	DQS7T/CQ7T
7B	VREFB7BN0	IO				DIFFOUT_T29n	K13	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T29p	K15	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	J13	DQSn10T	DQSn8T/DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	J14	DQS10T	DQS8T/CQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T31n	M14	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T31p	L14	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	L15	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	M15	DQ10T	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T33n	A12	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T33p	A13	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	C13	DQSn11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	D13	DQS11T	DQ11T/CQn11T	
7C	VREFB7CN0	IO				DIFFOUT_T35n	D15	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T35p	C15	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	C14	DQSn12T	DQSn11T/DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	D14	DQS12T	DQS11T/CQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37n	D16	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37p	C16	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	A14	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	B14	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T39n	E15	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T39p	E14	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	F16	DQSn13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	F17	DQS13T		
7C	VREFB7CN0	IO				DIFFOUT_T41n	E17	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T41p	F15	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	J15			
7C	VREFB7CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	J16			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T43n	M16			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T43p	K16			
7C	VREFB7CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T44n	G16			
7C	VREFB7CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T44p	H15			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T45n	L17			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T45p	M17			
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T23n	DIFFOUT_T46n	C17			
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T23p	DIFFOUT_T46p	D17			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T47n	A15			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T47p	B15			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T24n	DIFFOUT_T48n	A17			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T24p	DIFFOUT_T48p	B17			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T25p	DIFFOUT_T49p	B18			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T25n	DIFFOUT_T49n	A18			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T50p	B20			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T50n	A20			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T26p	DIFFOUT_T51p	D18			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T26n	DIFFOUT_T51n	C18			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T52p	M18			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T52n	L18			
8C	VREFB8CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	H21			
8C	VREFB8CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	H20			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T54p	M19			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T54n	K19			
8C	VREFB8CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	J20			
8C	VREFB8CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	J19			
8C	VREFB8CN0	IO				DIFFOUT_T56p	E18	DQ14T		
8C	VREFB8CN0	IO				DIFFOUT_T56n	F20	DQ14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	G19	DQS14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	F19	DQSn14T		
8C	VREFB8CN0	IO				DIFFOUT_T58p	E20	DQ14T		
8C	VREFB8CN0	IO				DIFFOUT_T58n	E21	DQ14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	B21	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	A21	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60p	D19	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60n	C19	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	D21	DQS15T	DQS16T/CQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C21	DQSn15T	DQSn16T/DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62p	D20	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62n	C20	DQ16T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32p	DIFFOUT_T63p	D22	DQS16T	DQ16T/CQn16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32n	DIFFOUT_T63n	C22	DQSn16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64p	A23	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64n	A22	DQ16T	DQ16T	
8B	VREFB8BN0	IO			DIFFIO_RX_T33p	DIFFOUT_T65p	M20	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T33n	DIFFOUT_T65n	L20	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T66p	M21	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T66n	L21	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T34p	DIFFOUT_T67p	J22	DQS17T	DQS19T/CQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T34n	DIFFOUT_T67n	J21	DQSn17T	DQSn19T/DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T68p	K22	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T68n	K20	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	G22	DQS18T	DQ19T/CQn19T	DQS20T/CQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	G21	DQSn18T	DQ19T	DQSn20T/DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T70p	H23	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T70n	H24	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	F24	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	E24	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T72p	F22	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T72n	F23	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	E23	DQS19T	DQS20T/CQ20T	DQ20T/CQn20T
8B	VREFB8BN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	D23	DQSn19T	DQSn20T/DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T74p	C23	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T74n	D24	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	B24	DQS20T	DQ20T/CQn20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	B23	DQSn20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T76p	A24	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T76n	A25	DQ20T	DQ20T	DQ20T
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	P23			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8A	VREFB8AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	N23			
8A	VREFB8AN0	IO				DIFFOUT_T78p	M22			
8A	VREFB8AN0	IO				DIFFOUT_T78n	L23			
8A	VREFB8AN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	M24	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	L24	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80p	M23	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80n	K23	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	K25	DQS21T	DQS24T/CQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	J25	DQSn21T	DQSn24T/DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82p	H27	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82n	J24	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	G25	DQS22T	DQ24T/CQn24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	G24	DQSn22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84p	H26	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84n	J23	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	D27	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	D26	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86p	E26	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86n	F26	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	D25	DQS23T	DQS25T/CQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	C25	DQSn23T	DQSn25T/DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88p	F27	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88n	E27	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	C26	DQS24T	DQ25T/CQn25T	DQS26T/CQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	B26	DQSn24T	DQ25T	DQSn26T/DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90p	C28	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90n	D28	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	B27	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	A27	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92p	A26	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92n	A28	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	B29	DQS25T	DQS26T/CQ26T	DQ26T/CQn26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	A29	DQSn25T	DQSn26T/DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94p	B30	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94n	B32	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T48p	DIFFOUT_T95p	A31	DQS26T	DQ26T/CQn26T	DQ26T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T48n	DIFFOUT_T95n	A30	DQSn26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96p	A32	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96n	C31	DQ26T	DQ26T	DQ26T
QL1		GXB_TX_L7p					E31			
QL1		GXB_TX_L7n					E32			
QL1		GXB_RX_L7p					F33			
QL1		GXB_RX_L7n					F34			
QL1		GXB_TX_L6p					G31			
QL1		GXB_TX_L6n					G32			
QL1		GXB_RX_L6p					H33			
QL1		GXB_RX_L6n					H34			
QL1		GXB_CMUTX_L3p					J31			
QL1		GXB_CMUTX_L3n					J32			
QL1		REFCLK_L3p, GXB_CMURX_L3p					K33			
QL1		REFCLK_L3n, GXB_CMURX_L3n					K34			
QL1		GXB_CMUTX_L2p					L31			
QL1		GXB_CMUTX_L2n					L32			
QL1		REFCLK_L2p, GXB_CMURX_L2p					M33			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
QL1		REFCLK_L2n, GXB_CMURX_L2n					M34			
QL1		GXB_TX_L5p					N31			
QL1		GXB_TX_L5n					N32			
QL1		GXB_RX_L5p					P33			
QL1		GXB_RX_L5n					P34			
QL1		GXB_TX_L4p					R31			
QL1		GXB_TX_L4n					R32			
QL1		GXB_RX_L4p					T33			
QL1		GXB_RX_L4n					T34			
QL0		GXB_TX_L3p					U31			
QL0		GXB_TX_L3n					U32			
QL0		GXB_RX_L3p					V33			
QL0		GXB_RX_L3n					V34			
QL0		GXB_TX_L2p					W31			
QL0		GXB_TX_L2n					W32			
QL0		GXB_RX_L2p					Y33			
QL0		GXB_RX_L2n					Y34			
QL0		GXB_CMUTX_L1p					AA31			
QL0		GXB_CMUTX_L1n					AA32			
QL0		REFCLK_L1p, GXB_CMURX_L1p					AB33			
QL0		REFCLK_L1n, GXB_CMURX_L1n					AB34			
QL0		GXB_CMUTX_L0p					AC31			
QL0		GXB_CMUTX_L0n					AC32			
QL0		REFCLK_L0p, GXB_CMURX_L0p					AD33			
QL0		REFCLK_L0n, GXB_CMURX_L0n					AD34			
QL0		GXB_TX_L1p					AE31			
QL0		GXB_TX_L1n					AE32			
QL0		GXB_RX_L1p					AF33			
QL0		GXB_RX_L1n					AF34			
QL0		GXB_TX_L0p					AG31			
QL0		GXB_TX_L0n					AG32			
QL0		GXB_RX_L0p					AH33			
QL0		GXB_RX_L0n					AH34			
QR0		GXB_RX_R0n					AH1			
QR0		GXB_RX_R0p					AH2			
QR0		GXB_TX_R0n					AG3			
QR0		GXB_TX_R0p					AG4			
QR0		GXB_RX_R1n					AF1			
QR0		GXB_RX_R1p					AF2			
QR0		GXB_TX_R1n					AE3			
QR0		GXB_TX_R1p					AE4			
QR0		REFCLK_R0n, GXB_CMURX_R0n					AD1			
QR0		REFCLK_R0p, GXB_CMURX_R0p					AD2			
QR0		GXB_CMUTX_R0n					AC3			
QR0		GXB_CMUTX_R0p					AC4			
QR0		REFCLK_R1n, GXB_CMURX_R1n					AB1			
QR0		REFCLK_R1p, GXB_CMURX_R1p					AB2			
QR0		GXB_CMUTX_R1n					AA3			
QR0		GXB_CMUTX_R1p					AA4			
QR0		GXB_RX_R2n					Y1			
QR0		GXB_RX_R2p					Y2			
QR0		GXB_TX_R2n					W3			
QR0		GXB_TX_R2p					W4			
QR0		GXB_RX_R3n					V1			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
QR0		GXB_RX_R3p					V2			
QR0		GXB_TX_R3n					U3			
QR0		GXB_TX_R3p					U4			
QR1		GXB_RX_R4n					T1			
QR1		GXB_RX_R4p					T2			
QR1		GXB_TX_R4n					R3			
QR1		GXB_TX_R4p					R4			
QR1		GXB_RX_R5n					P1			
QR1		GXB_RX_R5p					P2			
QR1		GXB_TX_R5n					N3			
QR1		GXB_TX_R5p					N4			
QR1		REFCLK_R2n, GXB_CMURX_R2n					M1			
QR1		REFCLK_R2p, GXB_CMURX_R2p					M2			
QR1		GXB_CMUTX_R2n					L3			
QR1		GXB_CMUTX_R2p					L4			
QR1		REFCLK_R3n, GXB_CMURX_R3n					K1			
QR1		REFCLK_R3p, GXB_CMURX_R3p					K2			
QR1		GXB_CMUTX_R3n					J3			
QR1		GXB_CMUTX_R3p					J4			
QR1		GXB_RX_R6n					H1			
QR1		GXB_RX_R6p					H2			
QR1		GXB_TX_R6n					G3			
QR1		GXB_TX_R6p					G4			
QR1		GXB_RX_R7n					F1			
QR1		GXB_RX_R7p					F2			
QR1		GXB_TX_R7n					E3			
QR1		GXB_TX_R7p					E4			
		GND					P21			
		GND					AN2			
		GND					U18			
		GND					U22			
		GND					AN4			
		GND					AN7			
		GND					AN10			
		GND					AN13			
		GND					AN16			
		GND					AN19			
		GND					AN22			
		GND					AN25			
		GND					AN28			
		GND					AN31			
		GND					AK4			
		GND					AK7			
		GND					AK10			
		GND					AK13			
		GND					AK16			
		GND					AK19			
		GND					AK22			
		GND					AK25			
		GND					AK28			
		GND					AK31			
		GND					AG7			
		GND					AG10			
		GND					AG13			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					AG16			
		GND					AG19			
		GND					AG22			
		GND					AG25			
		GND					AG28			
		GND					AD7			
		GND					AD10			
		GND					AD13			
		GND					AD16			
		GND					AD19			
		GND					AD22			
		GND					AD25			
		GND					AD28			
		GND					AB7			
		GND					AB13			
		GND					AB15			
		GND					AB17			
		GND					AB19			
		GND					AB21			
		GND					AB28			
		GND					AA10			
		GND					AA14			
		GND					AA16			
		GND					AA18			
		GND					AA20			
		GND					AA22			
		GND					AA25			
		GND					Y13			
		GND					Y15			
		GND					Y17			
		GND					Y19			
		GND					Y21			
		GND					W10			
		GND					W14			
		GND					W16			
		GND					W18			
		GND					W20			
		GND					W22			
		GND					W25			
		GND					V13			
		GND					V15			
		GND					V19			
		GND					V21			
		GND					U14			
		GND					U16			
		GND					U20			
		GND					T10			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					T21			
		GND					T25			
		GND					R14			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					R16			
		GND					R18			
		GND					R20			
		GND					R22			
		GND					P10			
		GND					P13			
		GND					P15			
		GND					P17			
		GND					P19			
		GND					P25			
		GND					N14			
		GND					N16			
		GND					N18			
		GND					N20			
		GND					N22			
		GND					L7			
		GND					L10			
		GND					L13			
		GND					L16			
		GND					L19			
		GND					L22			
		GND					L25			
		GND					L28			
		GND					H7			
		GND					H10			
		GND					H13			
		GND					H16			
		GND					H19			
		GND					H22			
		GND					H25			
		GND					H28			
		GND					E7			
		GND					E10			
		GND					E13			
		GND					E16			
		GND					E19			
		GND					E22			
		GND					E25			
		GND					E28			
		GND					B4			
		GND					B7			
		GND					B10			
		GND					B13			
		GND					B16			
		GND					B19			
		GND					B22			
		GND					B25			
		GND					B28			
		GND					B31			
		GND					C34			
		GND					C33			
		GND					D33			
		GND					D32			
		GND					D31			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					E34			
		GND					E33			
		GND					F32			
		GND					F31			
		GND					G34			
		GND					G33			
		GND					H32			
		GND					H31			
		GND					J34			
		GND					J33			
		GND					K32			
		GND					K31			
		GND					L34			
		GND					L33			
		GND					M32			
		GND					M31			
		GND					N34			
		GND					N33			
		GND					P32			
		GND					P31			
		GND					P29			
		GND					P27			
		GND					R34			
		GND					R33			
		GND					T32			
		GND					T31			
		GND					T28			
		GND					U34			
		GND					U33			
		GND					V32			
		GND					V31			
		GND					W34			
		GND					W33			
		GND					W29			
		GND					W27			
		GND					Y32			
		GND					AA28			
		GND					AL33			
		GND					AL34			
		GND					AK33			
		GND					AJ33			
		GND					AJ34			
		GND					AH31			
		GND					AH32			
		GND					AG33			
		GND					AG34			
		GND					AF31			
		GND					AF32			
		GND					AE33			
		GND					AE34			
		GND					AD31			
		GND					AD32			
		GND					AC33			
		GND					AC34			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					AB31			
		GND					AB32			
		GND					AA33			
		GND					AA34			
		GND					Y31			
		GND					C2			
		GND					C1			
		GND					D4			
		GND					D3			
		GND					D2			
		GND					E2			
		GND					E1			
		GND					F4			
		GND					F3			
		GND					G2			
		GND					G1			
		GND					H4			
		GND					H3			
		GND					J2			
		GND					J1			
		GND					K4			
		GND					K3			
		GND					L2			
		GND					L1			
		GND					M4			
		GND					M3			
		GND					N2			
		GND					N1			
		GND					P8			
		GND					P6			
		GND					P4			
		GND					P3			
		GND					R2			
		GND					R1			
		GND					T7			
		GND					T4			
		GND					T3			
		GND					U2			
		GND					U1			
		GND					V4			
		GND					V3			
		GND					W8			
		GND					W6			
		GND					W2			
		GND					W1			
		GND					Y4			
		GND					Y3			
		GND					AA7			
		GND					AA2			
		GND					AA1			
		GND					AB4			
		GND					AB3			
		GND					AC2			
		GND					AC1			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					AD4			
		GND					AD3			
		GND					AE2			
		GND					AE1			
		GND					AF4			
		GND					AF3			
		GND					AG2			
		GND					AG1			
		GND					AH4			
		GND					AH3			
		GND					AJ2			
		GND					AJ1			
		GND					AK2			
		GND					AL2			
		GND					AL1			
		VCC					U17			
		VCC					P20			
		VCC					AA15			
		VCC					AA17			
		VCC					AA19			
		VCC					AA21			
		VCC					Y14			
		VCC					Y16			
		VCC					Y18			
		VCC					Y20			
		VCC					W15			
		VCC					W17			
		VCC					W19			
		VCC					W21			
		VCC					V14			
		VCC					V16			
		VCC					V18			
		VCC					V20			
		VCC					U15			
		VCC					U19			
		VCC					U21			
		VCC					T14			
		VCC					T16			
		VCC					T18			
		VCC					T20			
		VCC					R15			
		VCC					R17			
		VCC					R19			
		VCC					R21			
		VCC					P14			
		VCC					P16			
		VCC					P18			
		VCC					AA27			
		VCC					Y27			
		VCC					T27			
		VCC					R27			
		VCC					AA8			
		VCC					Y8			
		VCC					T8			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCC					R8			
		VCCPGM					AL29			
		VCCPGM					AL6			
		TEMPDIODEn					A2			
		TEMPDIODEp					B1			
		VCC_CLKIN3C					AH18			
		VCC_CLKIN4C					AH17			
		VCC_CLKIN7C					G17			
		VCC_CLKIN8C					G18			
		VCCA_PLL_B1					AF18			
		VCCA_PLL_B2					AF17			
		VCCA_PLL_L2					V23			
		VCCA_PLL_R2					V12			
		VCCA_PLL_T1					J18			
		VCCA_PLL_T2					J17			
		VCCD_PLL_B1					AG18			
		VCCD_PLL_B2					AG17			
		VCCD_PLL_L2					U23			
		VCCD_PLL_R2					U12			
		VCCD_PLL_T1					H18			
		VCCD_PLL_T2					H17			
		VCCIO1A					E30			
		VCCIO1A					T26			
		VCCIO1A					P30			
		VCCIO1A					M27			
		VCCIO1A					J28			
		VCCIO1C					Y30			
		VCCIO1C					AJ28			
		VCCIO1C					AF30			
		VCCIO1C					AD26			
		VCCIO3A					AE24			
		VCCIO3A					AM27			
		VCCIO3A					AM32			
		VCCIO3A					AJ25			
		VCCIO3B					AE21			
		VCCIO3B					AM24			
		VCCIO3C					AE18			
		VCCIO3C					AP19			
		VCCIO3C					AJ21			
		VCCIO4A					AE11			
		VCCIO4A					AM3			
		VCCIO4A					AM8			
		VCCIO4A					AJ10			
		VCCIO4B					AE14			
		VCCIO4B					AM11			
		VCCIO4C					AE17			
		VCCIO4C					AP16			
		VCCIO4C					AJ14			
		VCCIO6A					E5			
		VCCIO6A					T9			
		VCCIO6A					P5			
		VCCIO6A					M8			
		VCCIO6A					J7			
		VCCIO6C					Y5			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCIO6C					AJ7			
		VCCIO6C					AF5			
		VCCIO6C					AD9			
		VCCIO7A					C8			
		VCCIO7A					K11			
		VCCIO7A					F10			
		VCCIO7A					C3			
		VCCIO7B					C11			
		VCCIO7B					K14			
		VCCIO7C					A16			
		VCCIO7C					K17			
		VCCIO7C					F14			
		VCCIO8A					C32			
		VCCIO8A					K24			
		VCCIO8A					F25			
		VCCIO8A					C27			
		VCCIO8B					C24			
		VCCIO8B					K21			
		VCCIO8C					A19			
		VCCIO8C					K18			
		VCCIO8C					F21			
		VCCPD1A					M25			
		VCCPD1C					V22			
		VCCPD3A					AB22			
		VCCPD3B					AB20			
		VCCPD3C					AB18			
		VCCPD4A					AA13			
		VCCPD4B					AB14			
		VCCPD4C					AB16			
		VCCPD6A					M10			
		VCCPD6C					U13			
		VCCPD7A					N13			
		VCCPD7B					N15			
		VCCPD7C					N17			
		VCCPD8A					P22			
		VCCPD8B					N21			
		VCCPD8C					N19			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				N27			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				V25			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AH26			
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AH23			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AH20			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AH9			
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AH12			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AH15			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				N8			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				V10			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G9			
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				G12			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G15			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G26			
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				G23			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G20			
		NC					C30			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		NC					AN34			
		NC					AF9			
		NC					B2			
		NC					AJ32			
		NC					AJ31			
		NC					AJ4			
		NC					AJ3			
		NC					AB11			
		NC					AB24			
		NC					AA11			
		NC *(3)*		MSEL2			E6			
		NC *(3)*		MSEL1			C6			
		NC *(3)*		MSEL0			C5			
		NC					Y12			
		NC					Y23			
		NC					T12			
		NC					T22			
		NC					T23			
		NC					R11			
		NC					R12			
		NC					R13			
		NC					R23			
		NC					R24			
		NC					AA12			
		NC					AA23			
		NC					AA24			
		NC *(4)*					H8			
		NC *(5)*					Y22			
		NC *(5)*					W23			
		NC *(5)*					AJ18			
		NC *(5)*					W12			
		NC *(5)*					W13			
		NC *(5)*					F18			
		NC *(6)*					V17			
		VCCAUX					F28			
		VCCAUX					AH27			
		VCCAUX					AH8			
		VCCAUX					F7			
		VCCA_L					AC30			
		VCCA_L					U30			
		VCCA_R					AC5			
		VCCA_R					U5			
		VCCH_GXBL0					Y29			
		VCCH_GXBL1					R29			
		VCCH_GXBR0					Y6			
		VCCH_GXBR1					R6			
		VCCL_GXBL0					W28			
		VCCL_GXBL0					Y28			
		VCCL_GXBL1					P28			
		VCCL_GXBL1					R28			
		VCCL_GXBR0					Y7			
		VCCL_GXBR0					W7			
		VCCL_GXBR1					R7			
		VCCL_GXBR1					P7			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix® IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCR_R					W5			
		VCCR_R					N5			
		VCCR_L					N30			
		VCCR_L					W30			
		VCCT_R					AA5			
		VCCT_R					R5			
		VCCT_L					AA30			
		VCCT_L					R30			
		VCCHIP_R					W9			
		VCCHIP_R					Y9			
		VCCHIP_R					V9			
		VCCHIP_L					V26			
		VCCHIP_L					Y26			
		VCCHIP_L					W26			
		RREF_L0					AK34			
		RREF_L1					D34			
		RREF_R0					AK1			
		RREF_R1					D1			

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Strati IV device pin table for details.
(2) The individual index number of the pin in this column may not be the same as its companion Stratix IV device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.
(6) This NC pin is a DNU pin in the Stratix IV device and must be left floating.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Clock and PLL Pins		
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, ,L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin fo HardCopy IV.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

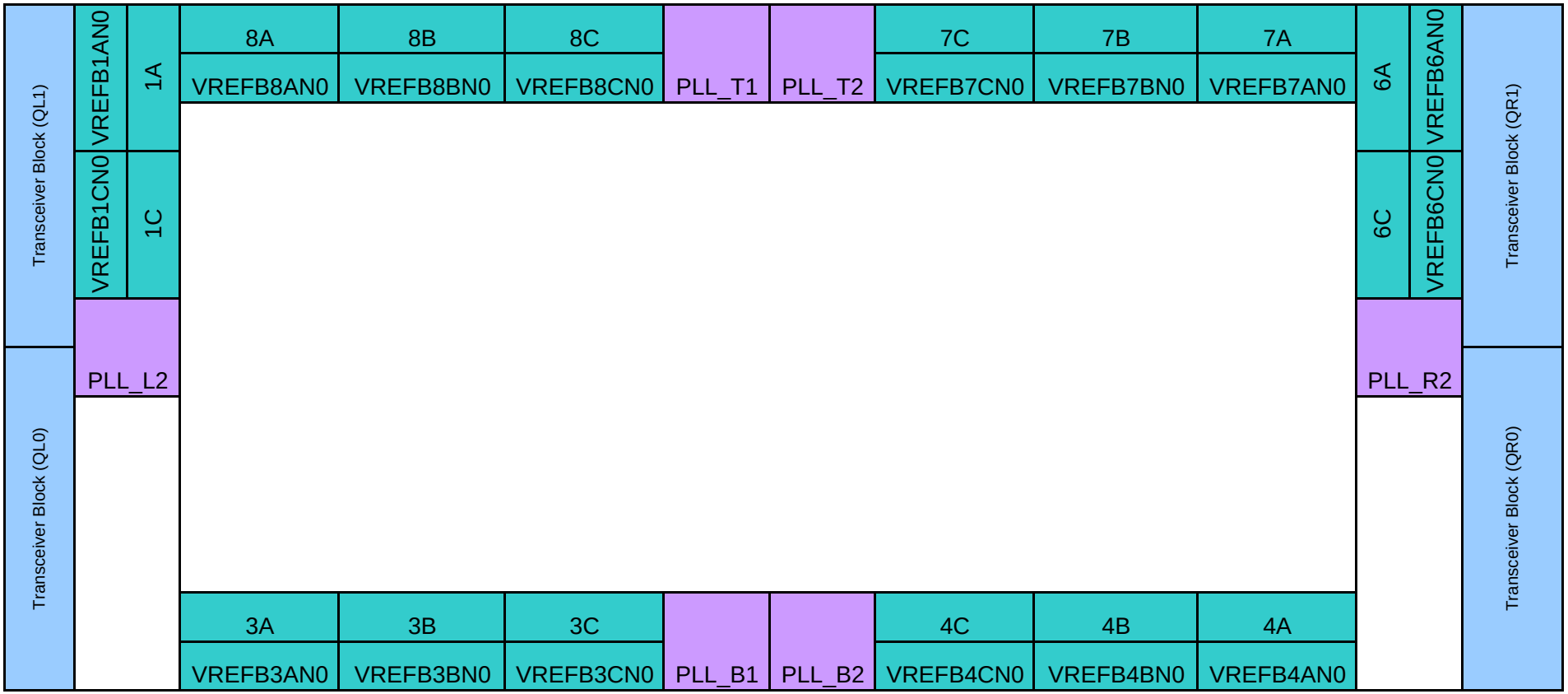
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), 3.0V PCI/PCI-X and LVTTL 3.3V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
VREFB[1:8][A,C]N0, VREFB[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
Transceiver (I/O Banks) Pins		
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p GXB_CMURX_[L,R][0:7]p	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n GXB_CMURX_[L,R][0:7]n	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC4GX35. Refer to the pin list for the availability of pins in each density.

(2) Refer to HardCopy IV Pin Connections Guidelines and Datasheet for the recommended operating voltage.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	4/30/2010	Initial release.