Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		TDI		TDI			G28			
		TMS		TMS			H28			
		TRST		TRST			K26			
		TCK		TCK			F29			
		TDO		TDO			G29			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	G30			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	H29			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	E31			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	E30			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J29	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	J28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	C32	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D32	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	K28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	L27	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	B34	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	A33	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	L26	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	M25	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	C34	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	B33	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	N25	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	N24	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	F32	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	F31	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K29	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	L28	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	D34	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	D33	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	H31	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	H30	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	G32	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	G31	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	K30	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L29	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	E34	DQSn5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	E33	DQS5L	DQ3L/CQn3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L9n	DIFFOUT_L17n	N27	DQ5L	DQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L9p	DIFFOUT_L17p	N26	DQ5L	DQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L9n	DIFFOUT_L18n	F34	DQSn6L	DQSn3L/DQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L9p	DIFFOUT_L18p	G33	DQS6L	DQS3L/CQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L10n	DIFFOUT_L19n	K31	DQ6L	DQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L10p	DIFFOUT_L19p	L30	DQ6L	DQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L10n	DIFFOUT_L20n	J32	DQ6L	DQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L10p	DIFFOUT_L20p	J31	DQ6L	DQ3L	
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L11n	DIFFOUT_L21n	M29	DQ7L		
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L11p	DIFFOUT_L21p	N28	DQ7L		
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L11n	DIFFOUT_L22n	G34	DQSn7L		
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L11p	DIFFOUT_L22p	H33	DQS7L		
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L12n	DIFFOUT_L23n	P24	DQ7L		
1A	VREFB1AN0	IO*(7)*			DIFFIO_TX_L12p	DIFFOUT_L23p	P23	DQ7L		
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L12n	DIFFOUT_L24n	H34			
1A	VREFB1AN0	IO*(7)*			DIFFIO_RX_L12p	DIFFOUT_L24p	J34			
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L13n	DIFFOUT_L25n	P26	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L13p	DIFFOUT_L25p	R25	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L13n	DIFFOUT_L26n	K32	DQSn8L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L13p	DIFFOUT_L26p	L31	DQS8L	DQ8L/CQn8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L14n	DIFFOUT_L27n	N30	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L14p	DIFFOUT_L27p	N29	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L14n	DIFFOUT_L28n	K34	DQSn9L	DQSn8L/DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L14p	DIFFOUT_L28p	K33	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L15n	DIFFOUT_L29n	P28	DQ9L	DQ8L	DQ8L

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L15p	DIFFOUT_L29p	P27	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L15n	DIFFOUT_L30n	L34	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L15p	DIFFOUT_L30p	L33	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L16n	DIFFOUT_L31n	T25	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_TX_L16p	DIFFOUT_L31p	T24	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L16n	DIFFOUT_L32n	M32	DQSn10L	DQ9L	DQSn8L/DQ8L
1C	VREFB1CN0	IO*(7)*			DIFFIO_RX_L16p	DIFFOUT_L32p	M31	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	T23	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	U23	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	N32	DQSn11L	DQSn9L/DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	N31	DQS11L	DQS9L/CQ9L	DQ8L
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	P29	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R29	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	M34	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	N33	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	T29	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	T28	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	P32	DQSn12L	DQ10L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	P31	DQS12L	DQ10L/CQn10L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	T27	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	T26	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	N34	DQSn13L	DQSn10L/DQ10L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	P33	DQS13L	DQS10L/CQ10L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	V25	DQ13L	DQ10L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	U24	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	R32	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	R31	DQ13L	DQ10L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	V23			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	W23			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	T31			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	T30			
1C	VREFB1CN0	CLK1n	CLK1n				P34			
1C	VREFB1CN0	CLK1p	CLK1p				R34			
		nCONFIG		nCONFIG			AC27			
		nSTATUS		nSTATUS			AM30			
		CONF_DONE		CONF_DONE			AN30			
		PORSEL		PORSEL			AL28			
		nCE		nCE			AM29			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AA25	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AB25	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AC26	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AC25	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AB24	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AC24	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE25	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD26	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AD23	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AE24	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AE27	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AE26	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AG26	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AF24	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH27	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AH26	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AJ27	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AG25	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH25	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH24	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AJ25	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AK26	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AG23	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AF23	DQ4B	DQ2B	DQ1B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
3A	VREFB3AN0	IO				DIFFOUT_B13n	AL27	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AM27	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AM26	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AL26	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AK25	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AN28	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AP32	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AP31	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AP28	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AP27	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AP30	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AP29	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AB23			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AA23			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AD22			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AC22			
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B21n	AC20	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B21p	AD20	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B11n	DIFFOUT_B22n	AF21	DQSn7B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B11p	DIFFOUT_B22p	AE22	DQS7B	DQ7B/CQn7B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B23n	AE20	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B23p	AE21	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B12n	DIFFOUT_B24n	AJ24	DQSn8B	DQSn7B/DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B12p	DIFFOUT_B24p	AH23	DQS8B	DQS7B/CQ7B	DQ7B/CQn7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B25n	AG22	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B25p	AH21	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B13n	DIFFOUT_B26n	AJ22	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B13p	DIFFOUT_B26p	AH22	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B27n	AL23	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B27p	AM23	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B14n	DIFFOUT_B28n	AM24	DQSn9B	DQ8B	DQSn7B/DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B14p	DIFFOUT_B28p	AL24	DQS9B	DQ8B/CQn8B	DQS7B/CQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B29n	AK22	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B29p	AK23	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B15n	DIFFOUT_B30n	AP26	DQSn10B	DQSn8B/DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B15p	DIFFOUT_B30p	AN26	DQS10B	DQS8B/CQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B31n	AM25	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*				DIFFOUT_B31p	AP24	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B16n	DIFFOUT_B32n	AP25	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO*(7)*			DIFFIO_RX_B16p	DIFFOUT_B32p	AN25	DQ10B	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B33n	AM22	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B33p	AP22	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AP23	DQSn11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AN23	DQS11B	DQ11B/CQn11B	
3C	VREFB3CN0	IO				DIFFOUT_B35n	AP21	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B35p	AN22	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AM21	DQSn12B	DQSn11B/DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AL21	DQS12B	DQS11B/CQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37n	AJ21	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37p	AK20	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AM20	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AL20	DQ12B	DQ11B	
3C	VREFB3CN0	IO*(7)*				DIFFOUT_B39n	AN20	DQ13B		
3C	VREFB3CN0	IO*(7)*				DIFFOUT_B39p	AJ20	DQ13B		
3C	VREFB3CN0	IO*(7)*			DIFFIO_RX_B20n	DIFFOUT_B40n	AM19	DQSn13B		
3C	VREFB3CN0	IO*(7)*			DIFFIO_RX_B20p	DIFFOUT_B40p	AL19	DQS13B		
3C	VREFB3CN0	IO*(7)*				DIFFOUT_B41n	AK19	DQ13B		
3C	VREFB3CN0	IO*(7)*				DIFFOUT_B41p	AJ19	DQ13B		
3C	VREFB3CN0	IO*(7)*			DIFFIO_RX_B21n	DIFFOUT_B42n	AH19			
3C	VREFB3CN0	IO*(7)*			DIFFIO_RX_B21p	DIFFOUT_B42p	AG19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B43n	AD19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B43p	AC18			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
3C	VREFB3CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AG20			
3C	VREFB3CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AF19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B45n	AE19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B45p	AE18			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B23n	DIFFOUT_B46n	AM18			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B23p	DIFFOUT_B46p	AL18			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B47n	AP20			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B47p	AP19			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B24n	DIFFOUT_B48n	AP18			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B24p	DIFFOUT_B48p	AP17			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B25p	DIFFOUT_B49p	AP15			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B25n	DIFFOUT_B49n	AP16			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B50p	AM17			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B50n	AN17			
4C	VREFB4CN0	IO***(7)***	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B26p	DIFFOUT_B51p	AK17			
4C	VREFB4CN0	IO***(7)***	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B26n	DIFFOUT_B51n	AL17			
4C	VREFB4CN0	IO***(7)***	PLL_B2_CLKOUT0p			DIFFOUT_B52p	AC16			
4C	VREFB4CN0	IO***(7)***	PLL_B2_CLKOUT0n			DIFFOUT_B52n	AD17			
4C	VREFB4CN0	IO***(7)***			DIFFIO_RX_B27p	DIFFOUT_B53p	AE16			
4C	VREFB4CN0	IO***(7)***			DIFFIO_RX_B27n	DIFFOUT_B53n	AF16			
4C	VREFB4CN0	IO***(7)***	PLL_B2_CLKOUT3			DIFFOUT_B54p	AE15			
4C	VREFB4CN0	IO***(7)***	PLL_B2_CLKOUT4			DIFFOUT_B54n	AD16			
4C	VREFB4CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AG16			
4C	VREFB4CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AH16			
4C	VREFB4CN0	IO				DIFFOUT_B56p	AJ16	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B56n	AK16	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AM15	DQS14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AM16	DQSn14B		
4C	VREFB4CN0	IO				DIFFOUT_B58p	AL16	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B58n	AH15	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AP13	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AP14	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60p	AP12	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60n	AN14	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AM13	DQS15B	DQS16B/CQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AN13	DQSn15B	DQSn16B/DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62p	AL15	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62n	AJ15	DQ16B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32p	DIFFOUT_B63p	AK14	DQS16B	DQ16B/CQn16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32n	DIFFOUT_B63n	AL14	DQSn16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64p	AJ14	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64n	AM14	DQ16B	DQ16B	
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B33p	DIFFOUT_B65p	AJ13	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B33n	DIFFOUT_B65n	AK13	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B66p	AG13	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B66n	AH13	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B34p	DIFFOUT_B67p	AH12	DQS17B	DQS19B/CQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B34n	DIFFOUT_B67n	AJ12	DQSn17B	DQSn19B/DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B68p	AC14	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B68n	AD14	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B35p	DIFFOUT_B69p	AF14	DQS18B	DQ19B/CQn19B	DQS20B/CQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B35n	DIFFOUT_B69n	AG14	DQSn18B	DQ19B	DQSn20B/DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B70p	AE14	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B70n	AE13	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B36p	DIFFOUT_B71p	AM11	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B36n	DIFFOUT_B71n	AN11	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B72p	AL12	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B72n	AM12	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B37p	DIFFOUT_B73p	AK11	DQS19B	DQS20B/CQ20B	DQ20B/CQn20B
4B	VREFB4BN0	IO***(7)***			DIFFIO_RX_B37n	DIFFOUT_B73n	AL11	DQSn19B	DQSn20B/DQ20B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B74p	AP11	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO***(7)***				DIFFOUT_B74n	AM10	DQ20B	DQ20B	DQ20B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
4B	VREFB4BN0	IO*(7)*			DIFFIO_RX_B38p	DIFFOUT_B75p	AN10	DQS20B	DQ20B/CQn20B	DQ20B
4B	VREFB4BN0	IO*(7)*			DIFFIO_RX_B38n	DIFFOUT_B75n	AP10	DQSn20B	DQ20B	DQ20B
4B	VREFB4BN0	IO*(7)*				DIFFOUT_B76p	AP9	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO*(7)*				DIFFOUT_B76n	AM9	DQ20B	DQ20B	DQ20B
4A	VREFB4AN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	Y12			
4A	VREFB4AN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AA12			
4A	VREFB4AN0	IO				DIFFOUT_B78p	AC12			
4A	VREFB4AN0	IO				DIFFOUT_B78n	AD13			
4A	VREFB4AN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AP5	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AP6	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80p	AN7	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80n	AP7	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AP3	DQS21B	DQS24B/CQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AP4	DQSn21B	DQSn24B/DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82p	AP8	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82n	AL9	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AM8	DQS22B	DQ24B/CQn24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AN8	DQSn22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84p	AL7	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84n	AL8	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AJ10	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AK10	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86p	AH11	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86n	AJ11	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AF12	DQS23B	DQS25B/CQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AG11	DQSn23B	DQSn25B/DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88p	AJ9	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88n	AG10	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AJ8	DQS24B	DQ25B/CQn25B	DQS26B/CQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AK8	DQSn24B	DQ25B	DQSn26B/DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90p	AH8	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90n	AH9	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AD9	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AE9	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92p	AE11	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92n	AE12	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AD11	DQS25B	DQS26B/CQ26B	DQ26B/CQn26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AE10	DQSn25B	DQSn26B/DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94p	AB11	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94n	AB12	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B48p	DIFFOUT_B95p	AB10	DQS26B	DQ26B/CQn26B	DQ26B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B48n	DIFFOUT_B95n	AC10	DQSn26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96p	AA10	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96n	AA11	DQ26B	DQ26B	DQ26B
		nIO_PULLUP		nIO_PULLUP			AM6			
		nCEO		nCEO			AE8			
		DCLK		DCLK			AM5			
		nCSO		nCSO			AD8			
		ASDO		ASDO			AN5			
6C	VREFB6CN0	CLK10p	CLK10p				P1			
6C	VREFB6CN0	CLK10n	CLK10n				R1			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	R3			
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	R2			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	U12			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	V12			
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	T5	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	T4	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	V11	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	U10	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	P4	DQS14R	DQS17R/CQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	P3	DQSn14R	DQSn17R/DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	T9	DQ15R	DQ17R	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	T8	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	N2	DQS15R	DQ17R/CQn17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	N1	DQSn15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	T11	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	T10	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	M2	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	M1	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	T7	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	T6	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	N4	DQS16R	DQS18R/CQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	N3	DQSn16R	DQSn18R/DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	R6	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	R5	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R29p	DIFFOUT_R57p	K1	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R29n	DIFFOUT_R57n	L1	DQSn17R	DQ18R	DQSn19R/DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R29p	DIFFOUT_R58p	R12	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R29n	DIFFOUT_R58n	R11	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R30p	DIFFOUT_R59p	K3	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R30n	DIFFOUT_R59n	K2	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R30p	DIFFOUT_R60p	R8	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R30n	DIFFOUT_R60n	R7	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R31p	DIFFOUT_R61p	L4	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R31n	DIFFOUT_R61n	L3	DQSn18R	DQSn19R/DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R31p	DIFFOUT_R62p	P7	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R31n	DIFFOUT_R62n	P6	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R32p	DIFFOUT_R63p	M5	DQS19R	DQ19R/CQn19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_RX_R32n	DIFFOUT_R63n	M4	DQSn19R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R32p	DIFFOUT_R64p	N6	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO*(7)*			DIFFIO_TX_R32n	DIFFOUT_R64n	N5	DQ19R	DQ19R	DQ19R
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R33p	DIFFOUT_R65p	J2			
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R33n	DIFFOUT_R65n	J1			
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R33p	DIFFOUT_R66p	M7	DQ20R		
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R33n	DIFFOUT_R66n	M6	DQ20R		
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R34p	DIFFOUT_R67p	J4	DQS20R		
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R34n	DIFFOUT_R67n	J3	DQSn20R		
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R34p	DIFFOUT_R68p	P10	DQ20R		
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R34n	DIFFOUT_R68n	P9	DQ20R		
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R35p	DIFFOUT_R69p	G1	DQ21R	DQ24R	
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R35n	DIFFOUT_R69n	H1	DQ21R	DQ24R	
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R35p	DIFFOUT_R70p	N9	DQ21R	DQ24R	
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R35n	DIFFOUT_R70n	N8	DQ21R	DQ24R	
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R36p	DIFFOUT_R71p	G2	DQS21R	DQS24R/CQ24R	
6A	VREFB6AN0	IO*(7)*			DIFFIO_RX_R36n	DIFFOUT_R71n	F1	DQSn21R	DQSn24R/DQ24R	
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R36p	DIFFOUT_R72p	L7	DQ22R	DQ24R	
6A	VREFB6AN0	IO*(7)*			DIFFIO_TX_R36n	DIFFOUT_R72n	L6	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	H4	DQS22R	DQ24R/CQn24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	H3	DQSn22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	K6	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	K5	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	F2	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	E1	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	N11	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	N10	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	G4	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	G3	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	N12	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	M11	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	D2	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	D1	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	J6	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J5	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	C2	DQ25R	DQ26R	DQ26R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	C1	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	M9	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	M8	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	E4	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	E3	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	K8	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	K7	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D4	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	D3	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	F5	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	F4	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	A2			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	B1			
6A	VREFB6AN0	IO			DIFFIO_TX_R44p	DIFFOUT_R88p	H7			
6A	VREFB6AN0	IO			DIFFIO_TX_R44n	DIFFOUT_R88n	H6			
7A	VREFB7AN0	IO				DIFFOUT_T1n	J11	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	K11	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	H12	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	J12	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	K12	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	L12	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	F8	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	G8	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	H9	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	G9	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	G10	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	H10	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	F7	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	F6	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	D6	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	E6	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	E7	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	D7	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	B4	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	C5	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A5	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	A4	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A3	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B3	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	G11	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	E10	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	E9	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	F10	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	A6	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	B6	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	A7	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	C6	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A8	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B7	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	L13			
7A	VREFB7AN0	IO				DIFFOUT_T19p	M13			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	C9			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	D9			
7B	VREFB7BN0	IO*(7)*				DIFFOUT_T21n	M15	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO*(7)*				DIFFOUT_T21p	K13	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO*(7)*			DIFFIO_RX_T11n	DIFFOUT_T22n	J14	DQSn7T	DQ7T	DQ7T
7B	VREFB7BN0	IO*(7)*			DIFFIO_RX_T11p	DIFFOUT_T22p	K14	DQS7T	DQ7T/CQn7T	DQ7T
7B	VREFB7BN0	IO*(7)*				DIFFOUT_T23n	K15	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO*(7)*				DIFFOUT_T23p	L15	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO*(7)*			DIFFIO_RX_T12n	DIFFOUT_T24n	F13	DQSn8T	DQSn7T/DQ7T	DQ7T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T12p	DIFFOUT_T24p	G13	DQS8T	DQS7T/CQ7T	DQ7T/CQn7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T25n	G12	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T25p	H13	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T13n	DIFFOUT_T26n	F14	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T13p	DIFFOUT_T26p	G14	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T27n	D11	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T27p	C11	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T14n	DIFFOUT_T28n	D12	DQSn9T	DQ8T	DQSn7T/DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T14p	DIFFOUT_T28p	E12	DQS9T	DQ8T/CQn8T	DQS7T/CQ7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T29n	F11	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T29p	E13	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T15n	DIFFOUT_T30n	A9	DQSn10T	DQSn8T/DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T15p	DIFFOUT_T30p	B9	DQS10T	DQS8T/CQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T31n	A11	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***				DIFFOUT_T31p	C10	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T16n	DIFFOUT_T32n	A10	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO***(7)***			DIFFIO_RX_T16p	DIFFOUT_T32p	B10	DQ10T	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T33n	A13	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T33p	A12	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	B13	DQSn11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	C13	DQS11T	DQ11T/CQn11T	
7C	VREFB7CN0	IO				DIFFOUT_T35n	C12	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T35p	B12	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	C14	DQSn12T	DQSn11T/DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	D14	DQS12T	DQS11T/CQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37n	C15	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37p	A14	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	A15	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	B15	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T39n	C16	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T39p	D15	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	E15	DQSn13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	F15	DQS13T		
7C	VREFB7CN0	IO				DIFFOUT_T41n	F16	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T41p	E16	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	G16			
7C	VREFB7CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	H15			
7C	VREFB7CN0	IO***(7)***	PLL_T2_CLKOUT4			DIFFOUT_T43n	M17			
7C	VREFB7CN0	IO***(7)***	PLL_T2_CLKOUT3			DIFFOUT_T43p	L16			
7C	VREFB7CN0	IO***(7)***			DIFFIO_RX_T22n	DIFFOUT_T44n	H16			
7C	VREFB7CN0	IO***(7)***			DIFFIO_RX_T22p	DIFFOUT_T44p	J16			
7C	VREFB7CN0	IO***(7)***	PLL_T2_CLKOUT0n			DIFFOUT_T45n	K16			
7C	VREFB7CN0	IO***(7)***	PLL_T2_CLKOUT0p			DIFFOUT_T45p	K17			
7C	VREFB7CN0	IO***(7)***	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T23n	DIFFOUT_T46n	C17			
7C	VREFB7CN0	IO***(7)***	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T23p	DIFFOUT_T46p	D17			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T47n	A16			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T47p	B16			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T24n	DIFFOUT_T48n	A17			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T24p	DIFFOUT_T48p	A18			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T25p	DIFFOUT_T49p	C18			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T25n	DIFFOUT_T49n	B18			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T50p	A20			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T50n	A19			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T26p	DIFFOUT_T51p	E18			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T26n	DIFFOUT_T51n	D18			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T52p	M19			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T52n	L18			
8C	VREFB8CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	H19			
8C	VREFB8CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	G19			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T54p	L19			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T54n	K20			
8C	VREFB8CN0	IO***(7)***			DIFFIO_RX_T28p	DIFFOUT_T55p	K19			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8C	VREFB8CN0	IO*(7)*			DIFFIO_RX_T28n	DIFFOUT_T55n	J19			
8C	VREFB8CN0	IO*(7)*				DIFFOUT_T56p	F20	DQ14T		
8C	VREFB8CN0	IO*(7)*				DIFFOUT_T56n	G20	DQ14T		
8C	VREFB8CN0	IO*(7)*			DIFFIO_RX_T29p	DIFFOUT_T57p	E19	DQS14T		
8C	VREFB8CN0	IO*(7)*			DIFFIO_RX_T29n	DIFFOUT_T57n	D19	DQSn14T		
8C	VREFB8CN0	IO*(7)*				DIFFOUT_T58p	F19	DQ14T		
8C	VREFB8CN0	IO*(7)*				DIFFOUT_T58n	C19	DQ14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	A23	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	A22	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60p	B21	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60n	A21	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	C22	DQS15T	DQS16T/CQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	B22	DQSn15T	DQSn16T/DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62p	F21	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62n	C20	DQ16T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32p	DIFFOUT_T63p	E21	DQS16T	DQ16T/CQn16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32n	DIFFOUT_T63n	D21	DQSn16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64p	D20	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64n	C21	DQ16T	DQ16T	
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T33p	DIFFOUT_T65p	A26	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T33n	DIFFOUT_T65n	A25	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T66p	A24	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T66n	B24	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T34p	DIFFOUT_T67p	C26	DQS17T	DQS19T/CQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T34n	DIFFOUT_T67n	B25	DQSn17T	DQSn19T/DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T68p	E24	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T68n	C25	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T35p	DIFFOUT_T69p	D24	DQS18T	DQ19T/CQn19T	DQS20T/CQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T35n	DIFFOUT_T69n	C24	DQSn18T	DQ19T	DQSn20T/DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T70p	D23	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T70n	C23	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T36p	DIFFOUT_T71p	J21	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T36n	DIFFOUT_T71n	H21	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T72p	L21	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T72n	M21	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T37p	DIFFOUT_T73p	K22	DQS19T	DQS20T/CQ20T	DQ20T/CQn20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T37n	DIFFOUT_T73n	K21	DQSn19T	DQSn20T/DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T74p	E22	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T74n	F22	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T38p	DIFFOUT_T75p	H22	DQS20T	DQ20T/CQn20T	DQ20T
8B	VREFB8BN0	IO*(7)*			DIFFIO_RX_T38n	DIFFOUT_T75n	G22	DQSn20T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T76p	F23	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO*(7)*				DIFFOUT_T76n	G23	DQ20T	DQ20T	DQ20T
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	M23			
8A	VREFB8AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	L22			
8A	VREFB8AN0	IO				DIFFOUT_T78p	L24			
8A	VREFB8AN0	IO				DIFFOUT_T78n	K25			
8A	VREFB8AN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	B28	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	A29	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80p	A27	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80n	A28	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	C27	DQS21T	DQS24T/CQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	B27	DQSn21T	DQSn24T/DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82p	E25	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82n	F24	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	D26	DQS22T	DQ24T/CQn24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	D27	DQSn22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84p	F25	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84n	E27	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	A31	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	A32	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86p	A30	DQ23T	DQ25T	DQ26T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8A	VREFB8AN0	IO				DIFFOUT_T86n	B30	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	C31	DQS23T	DQS25T/CQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	B31	DQSn23T	DQSn25T/DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88p	E28	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88n	D28	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	D29	DQS24T	DQ25T/CQn25T	DQS26T/CQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	C29	DQSn24T	DQ25T	DQSn26T/DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90p	D30	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90n	C30	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	G26	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	F26	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92p	G25	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92n	H25	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	G27	DQS25T	DQS26T/CQ26T	DQ26T/CQn26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	F27	DQSn25T	DQSn26T/DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94p	J23	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94n	K23	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T48p	DIFFOUT_T95p	J24	DQS26T	DQ26T/CQn26T	DQ26T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T48n	DIFFOUT_T95n	H24	DQSn26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96p	J25	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96n	K24	DQ26T	DQ26T	DQ26T
QL1		GXB_TX_L7p					V31			
QL1		GXB_TX_L7n					V32			
QL1		GXB_RX_L7p					U33			
QL1		GXB_RX_L7n					U34			
QL1		GXB_TX_L6p					Y31			
QL1		GXB_TX_L6n					Y32			
QL1		GXB_RX_L6p					W33			
QL1		GXB_RX_L6n					W34			
QL1		REFCLK_L3p, GXB_CMURX_L3p					AC29			
QL1		REFCLK_L3n, GXB_CMURX_L3n					AC30			
QL1		REFCLK_L2p, GXB_CMURX_L2p					AE29			
QL1		REFCLK_L2n, GXB_CMURX_L2n					AE30			
QL1		GXB_TX_L5p					AB31			
QL1		GXB_TX_L5n					AB32			
QL1		GXB_RX_L5p					AA33			
QL1		GXB_RX_L5n					AA34			
QL1		GXB_TX_L4p					AD31			
QL1		GXB_TX_L4n					AD32			
QL1		GXB_RX_L4p					AC33			
QL1		GXB_RX_L4n					AC34			
QL0		GXB_TX_L3p					AF31			
QL0		GXB_TX_L3n					AF32			
QL0		GXB_RX_L3p					AE33			
QL0		GXB_RX_L3n					AE34			
QL0		GXB_TX_L2p					AH31			
QL0		GXB_TX_L2n					AH32			
QL0		GXB_RX_L2p					AG33			
QL0		GXB_RX_L2n					AG34			
QL0		REFCLK_L1p, GXB_CMURX_L1p					AG29			
QL0		REFCLK_L1n, GXB_CMURX_L1n					AG30			
QL0		REFCLK_L0p, GXB_CMURX_L0p					AJ29			
QL0		REFCLK_L0n, GXB_CMURX_L0n					AJ30			
QL0		GXB_TX_L1p					AK31			
QL0		GXB_TX_L1n					AK32			
QL0		GXB_RX_L1p					AJ33			
QL0		GXB_RX_L1n					AJ34			
QL0		GXB_TX_L0p					AM31			
QL0		GXB_TX_L0n					AM32			
QL0		GXB_RX_L0p					AL33			
QL0		GXB_RX_L0n					AL34			
QR0		GXB_RX_R0n					AL1			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
QR0		GXB_RX_R0p					AL2			
QR0		GXB_TX_R0n					AM3			
QR0		GXB_TX_R0p					AM4			
QR0		GXB_RX_R1n					AJ1			
QR0		GXB_RX_R1p					AJ2			
QR0		GXB_TX_R1n					AK3			
QR0		GXB_TX_R1p					AK4			
QR0		REFCLK_R0n, GXB_CMURX_R0n					AJ5			
QR0		REFCLK_R0p, GXB_CMURX_R0p					AJ6			
QR0		REFCLK_R1n, GXB_CMURX_R1n					AG5			
QR0		REFCLK_R1p, GXB_CMURX_R1p					AG6			
QR0		GXB_RX_R2n					AG1			
QR0		GXB_RX_R2p					AG2			
QR0		GXB_TX_R2n					AH3			
QR0		GXB_TX_R2p					AH4			
QR0		GXB_RX_R3n					AE1			
QR0		GXB_RX_R3p					AE2			
QR0		GXB_TX_R3n					AF3			
QR0		GXB_TX_R3p					AF4			
QR1		GXB_RX_R4n					AC1			
QR1		GXB_RX_R4p					AC2			
QR1		GXB_TX_R4n					AD3			
QR1		GXB_TX_R4p					AD4			
QR1		GXB_RX_R5n					AA1			
QR1		GXB_RX_R5p					AA2			
QR1		GXB_TX_R5n					AB3			
QR1		GXB_TX_R5p					AB4			
QR1		REFCLK_R2n, GXB_CMURX_R2n					AE5			
QR1		REFCLK_R2p, GXB_CMURX_R2p					AE6			
QR1		REFCLK_R3n, GXB_CMURX_R3n					AC5			
QR1		REFCLK_R3p, GXB_CMURX_R3p					AC6			
QR1		GXB_RX_R6n					W1			
QR1		GXB_RX_R6p					W2			
QR1		GXB_TX_R6n					Y3			
QR1		GXB_TX_R6p					Y4			
QR1		GXB_RX_R7n					U1			
QR1		GXB_RX_R7p					U2			
QR1		GXB_TX_R7n					V3			
QR1		GXB_TX_R7p					V4			
		GND					P21			
		GND					AC8			
		GND					U18			
		GND					B32			
		GND					AN6			
		GND					AN9			
		GND					AN12			
		GND					AN15			
		GND					AN18			
		GND					AN21			
		GND					AN24			
		GND					AN27			
		GND					AN29			
		GND					AK9			
		GND					AK12			
		GND					AK15			
		GND					AK18			
		GND					AK21			
		GND					AK24			
		GND					AK27			
		GND					AG9			
		GND					AG12			
		GND					AG15			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					AG18			
		GND					AG21			
		GND					AG24			
		GND					AG27			
		GND					AF8			
		GND					AD12			
		GND					AD15			
		GND					AD18			
		GND					AD21			
		GND					AD24			
		GND					AD27			
		GND					AC9			
		GND					AC11			
		GND					AB13			
		GND					AB15			
		GND					AB17			
		GND					AB19			
		GND					AB21			
		GND					AA14			
		GND					AA16			
		GND					AA18			
		GND					AA20			
		GND					AA22			
		GND					AA24			
		GND					Y11			
		GND					Y13			
		GND					Y15			
		GND					Y17			
		GND					Y19			
		GND					Y21			
		GND					W14			
		GND					W16			
		GND					W18			
		GND					W20			
		GND					W22			
		GND					V13			
		GND					V15			
		GND					V19			
		GND					V21			
		GND					V24			
		GND					U11			
		GND					U14			
		GND					U16			
		GND					U20			
		GND					U22			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					T21			
		GND					R14			
		GND					R16			
		GND					R18			
		GND					R20			
		GND					R22			
		GND					R24			
		GND					R27			
		GND					R30			
		GND					R33			
		GND					P2			
		GND					P5			
		GND					P8			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					P11			
		GND					P13			
		GND					P15			
		GND					P17			
		GND					P19			
		GND					N14			
		GND					N16			
		GND					N18			
		GND					N20			
		GND					N22			
		GND					M24			
		GND					M27			
		GND					M30			
		GND					M33			
		GND					L2			
		GND					L5			
		GND					L8			
		GND					L11			
		GND					L14			
		GND					L17			
		GND					L20			
		GND					L23			
		GND					J27			
		GND					J30			
		GND					J33			
		GND					H2			
		GND					H5			
		GND					H8			
		GND					H11			
		GND					H14			
		GND					H17			
		GND					H20			
		GND					H23			
		GND					H26			
		GND					F30			
		GND					F33			
		GND					E2			
		GND					E5			
		GND					E8			
		GND					E11			
		GND					E14			
		GND					E17			
		GND					E20			
		GND					E23			
		GND					E26			
		GND					E29			
		GND					C33			
		GND					B2			
		GND					B5			
		GND					B8			
		GND					B11			
		GND					B14			
		GND					B17			
		GND					B20			
		GND					B23			
		GND					B26			
		GND					B29			
		GND					T34			
		GND					T33			
		GND					T32			
		GND					U32			
		GND					U31			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					U29			
		GND					U27			
		GND					V34			
		GND					V33			
		GND					V30			
		GND					V28			
		GND					W32			
		GND					W31			
		GND					W29			
		GND					W27			
		GND					Y34			
		GND					Y33			
		GND					Y30			
		GND					Y28			
		GND					AA32			
		GND					AA31			
		GND					AA29			
		GND					AA27			
		GND					AB34			
		GND					AB33			
		GND					AB30			
		GND					AB28			
		GND					AC32			
		GND					AC31			
		GND					AD34			
		GND					AD33			
		GND					AD30			
		GND					AD29			
		GND					AE32			
		GND					AE31			
		GND					AF34			
		GND					AF33			
		GND					AF30			
		GND					AF29			
		GND					AG32			
		GND					AG31			
		GND					AP33			
		GND					AN31			
		GND					AN32			
		GND					AN33			
		GND					AM33			
		GND					AM34			
		GND					AL31			
		GND					AL32			
		GND					AK29			
		GND					AK30			
		GND					AK33			
		GND					AK34			
		GND					AJ31			
		GND					AJ32			
		GND					AH29			
		GND					AH30			
		GND					AH33			
		GND					AH34			
		GND					T3			
		GND					T2			
		GND					T1			
		GND					U8			
		GND					U6			
		GND					U4			
		GND					U3			
		GND					V7			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					V5			
		GND					V2			
		GND					V1			
		GND					W8			
		GND					W6			
		GND					W4			
		GND					W3			
		GND					Y7			
		GND					Y5			
		GND					Y2			
		GND					Y1			
		GND					AA8			
		GND					AA6			
		GND					AA4			
		GND					AA3			
		GND					AB7			
		GND					AB5			
		GND					AB2			
		GND					AB1			
		GND					AC4			
		GND					AC3			
		GND					AD6			
		GND					AD5			
		GND					AD2			
		GND					AD1			
		GND					AE4			
		GND					AE3			
		GND					AF6			
		GND					AF5			
		GND					AF2			
		GND					AF1			
		GND					AG4			
		GND					AG3			
		GND					AH6			
		GND					AH5			
		GND					AH2			
		GND					AH1			
		GND					AJ4			
		GND					AJ3			
		GND					AK6			
		GND					AK5			
		GND					AK2			
		GND					AK1			
		GND					AL4			
		GND					AL3			
		GND					AM2			
		GND					AM1			
		GND					AN4			
		GND					AN3			
		GND					AN2			
		GND					AP2			
		VCC					U17			
		VCC					N19			
		VCC					AB14			
		VCC					AB16			
		VCC					AB18			
		VCC					AB20			
		VCC					AB22			
		VCC					AA13			
		VCC					AA15			
		VCC					AA17			
		VCC					AA19			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCC					AA21			
		VCC					Y14			
		VCC					Y16			
		VCC					Y18			
		VCC					Y20			
		VCC					Y22			
		VCC					W13			
		VCC					W15			
		VCC					W17			
		VCC					W19			
		VCC					W21			
		VCC					V14			
		VCC					V16			
		VCC					V18			
		VCC					V20			
		VCC					V22			
		VCC					U13			
		VCC					U15			
		VCC					U19			
		VCC					U21			
		VCC					T14			
		VCC					T16			
		VCC					T18			
		VCC					T20			
		VCC					T22			
		VCC					R13			
		VCC					R15			
		VCC					R17			
		VCC					R19			
		VCC					R21			
		VCC					P14			
		VCC					P16			
		VCC					P18			
		VCC					P20			
		VCC					P22			
		VCC					N13			
		VCC					N15			
		VCC					N17			
		VCC					N21			
		VCC					AB26			
		VCC					AB27			
		VCC					V26			
		VCC					U26			
		VCC					AB8			
		VCC					AB9			
		VCC					V9			
		VCC					U9			
		VCCPGM					AD25			
		VCCPGM					AD10			
		TEMPDIODEn					C3			
		TEMPDIODEp					D5			
		VCC_CLKIN3C					AF18			
		VCC_CLKIN4C					AE17			
		VCC_CLKIN7C					J17			
		VCC_CLKIN8C					K18			
		VCCA_PLL_B1					AJ18			
		VCCA_PLL_B2***(7)***					AH17			
		VCCA_PLL_L2					W25			
		VCCA_PLL_R2					W10			
		VCCA_PLL_T1					G18			
		VCCA_PLL_T2***(7)***					F17			
		VCCD_PLL_B1					AH18			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCD_PLL_B2***(7)***					AG17			
		VCCD_PLL_L2					W24			
		VCCD_PLL_R2					V10			
		VCCD_PLL_T1					H18			
		VCCD_PLL_T2***(7)***					G17			
		VCCIO1A					P25			
		VCCIO1A					M28			
		VCCIO1A					K27			
		VCCIO1A***(7)***					H32			
		VCCIO1A***(7)***					E32			
		VCCIO1C					L32			
		VCCIO1C					U25			
		VCCIO1C***(7)***					R28			
		VCCIO1C***(7)***					P30			
		VCCIO3A					AF25			
		VCCIO3A					AM28			
		VCCIO3A					AJ26			
		VCCIO3A					AE23			
		VCCIO3B***(7)***					AJ23			
		VCCIO3B***(7)***					AL25			
		VCCIO3C					AH20			
		VCCIO3C					AN19			
		VCCIO3C***(7)***					AL22			
		VCCIO4A					AF9			
		VCCIO4A					AM7			
		VCCIO4A					AH10			
		VCCIO4A					AF11			
		VCCIO4B***(7)***					AL13			
		VCCIO4B***(7)***					AL10			
		VCCIO4C					AJ17			
		VCCIO4C					AN16			
		VCCIO4C***(7)***					AH14			
		VCCIO6A					F3			
		VCCIO6A					L9			
		VCCIO6A					K4			
		VCCIO6A***(7)***					J7			
		VCCIO6A***(7)***					G5			
		VCCIO6C					N7			
		VCCIO6C					R4			
		VCCIO6C***(7)***					R9			
		VCCIO6C***(7)***					M3			
		VCCIO7A					C7			
		VCCIO7A					K10			
		VCCIO7A					F9			
		VCCIO7A					C4			
		VCCIO7B***(7)***					F12			
		VCCIO7B***(7)***					D10			
		VCCIO7C					D16			
		VCCIO7C					G15			
		VCCIO7C***(7)***					D13			
		VCCIO8A					C28			
		VCCIO8A					L25			
		VCCIO8A					G24			
		VCCIO8A					F28			
		VCCIO8B***(7)***					D25			
		VCCIO8B***(7)***					D22			
		VCCIO8C					B19			
		VCCIO8C					G21			
		VCCIO8C***(7)***					F18			
		VCCPD1A					N23			
		VCCPD1C					R23			
		VCCPD3A					AC23			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCPD3B***(7)***					AC21			
		VCCPD3C					AC19			
		VCCPD4A					AC13			
		VCCPD4B***(7)***					AC15			
		VCCPD4C					AC17			
		VCCPD6A					P12			
		VCCPD6C					T12			
		VCCPD7A					M12			
		VCCPD7B***(7)***					M14			
		VCCPD7C					M16			
		VCCPD8A					M22			
		VCCPD8B***(7)***					M20			
		VCCPD8C					M18			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				M26			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				R26			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AF26			
3B	VREFB3BN0	VREFB3BN0***(7)***	VREFB3BN0				AF22			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AF20			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AF10			
4B	VREFB4BN0	VREFB4BN0***(7)***	VREFB4BN0				AF13			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AF15			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				M10			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				R10			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				J10			
7B	VREFB7BN0	VREFB7BN0***(7)***	VREFB7BN0				J13			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				J15			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				J26			
8B	VREFB8BN0	VREFB8BN0***(7)***	VREFB8BN0				J22			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				J20			
		NC					D31			
		NC					AK28			
		NC					AK7			
		NC					G7			
		NC					AL29			
		NC					AL30			
		NC					AL5			
		NC					AL6			
		NC					AJ7			
		NC					AJ28			
		NC					AH7			
		NC					AH28			
		NC					AG7			
		NC					AG28			
		NC					AF7			
		NC					AF28			
		NC					AE7			
		NC					AE28			
		NC					AD7			
		NC					AD28			
		NC					AC7			
		NC					AC28			
		NC***(6)***					V17			
		NC***(4)***					G6			
		NC***(3)***		MSEL2			K9			
		NC***(3)***		MSEL1			L10			
		NC***(3)***		MSEL0			J9			
		NC***(5)***					Y23			
		NC***(5)***					Y24			
		NC***(5)***					AF17			
		NC***(5)***					W11			
		NC***(5)***					W12			
		NC***(5)***					J18			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCAUX					H27			
		VCCAUX					AF27			
		VCCAUX					AG8			
		VCCAUX					J8			
		VCCA_L					Y29			
		VCCA_L					V29			
		VCCA_R					Y6			
		VCCA_R					V6			
		VCCH_GXBL0					AA28			
		VCCH_GXBL1					U28			
		VCCH_GXBR0					AA7			
		VCCH_GXBR1					U7			
		VCCL_GXBL0					AA26			
		VCCL_GXBL0					Y27			
		VCCL_GXBL1					W28			
		VCCL_GXBL1					V27			
		VCCL_GXBR0					Y8			
		VCCL_GXBR0					AA9			
		VCCL_GXBR1					W7			
		VCCL_GXBR1					V8			
		VCCR_R					U5			
		VCCR_R					AA5			
		VCCR_L					U30			
		VCCR_L					AA30			
		VCCT_R					AB6			
		VCCT_R					W5			
		VCCT_L					AB29			
		VCCT_L					W30			
		VCCHIP_R					W9			
		VCCHIP_R					Y10			
		VCCHIP_R					Y9			
		VCCHIP_L					W26			
		VCCHIP_L					Y26			
		VCCHIP_L					Y25			
		RREF_L0					AN34			
		RREF_R0					AN1			

Notes on Pin Table:
(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix IV device pin table for details.
(2) The individual index number of the pin in this column may not be the same as its companion Stratix IV device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.
(6) This NC pin is a DNU pin in the Stratix IV device and must be left floating.
(7) These pins are NC in FPGA companion device EP4SGX110FF35 only.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Clock and PLL Pins		
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, ,L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin for HardCopy IV.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.

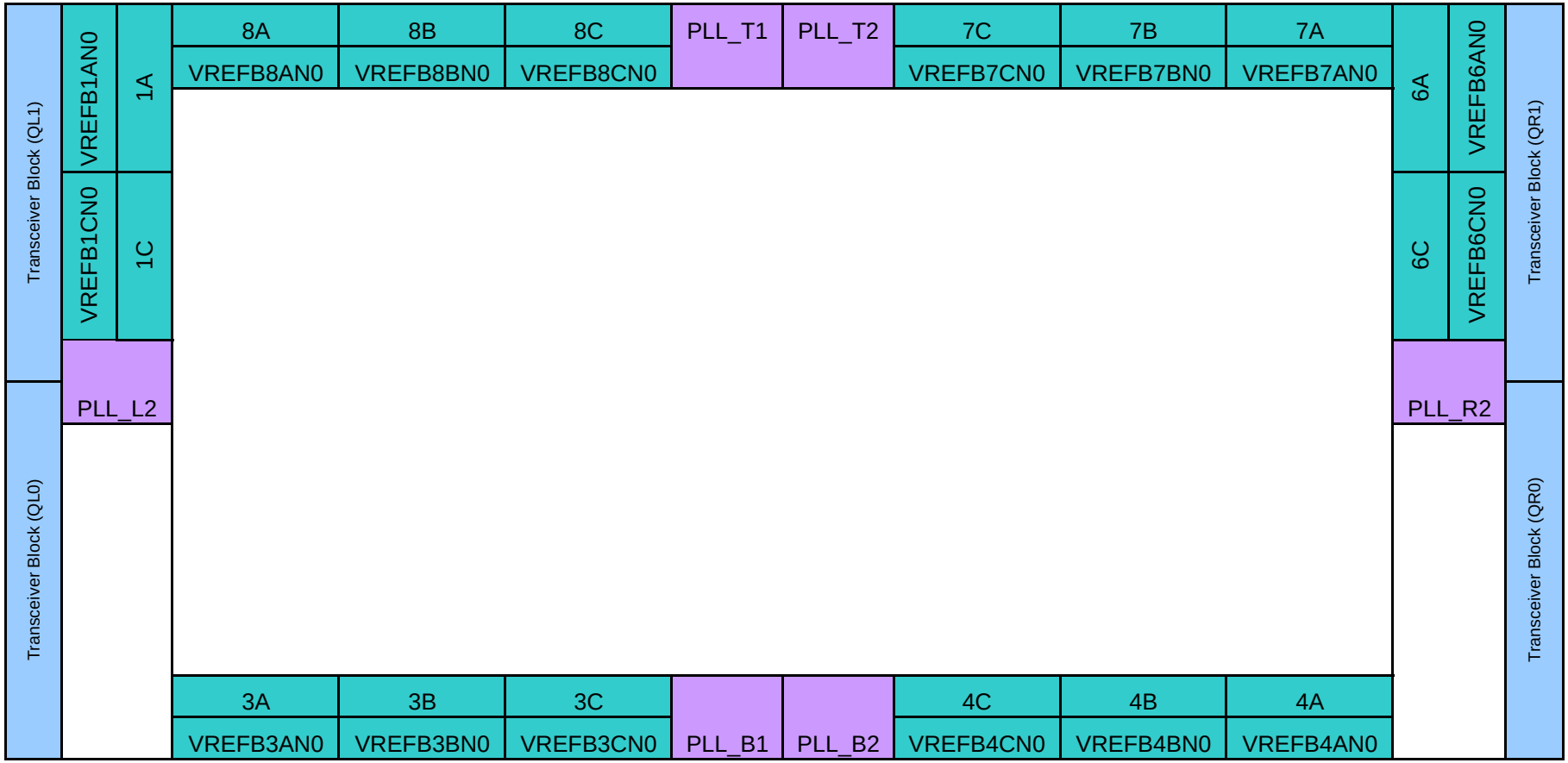
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), 3.0V PCI/PCI-X and LVTTL 3.3V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
GND	Ground	Device ground pins.
VREFB[1:8][A,C]N0, VREFB[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
Transceiver (I/O Banks) Pins		
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p GXB_CMURX_[L,R][0:7]p	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n GXB_CMURX_[L,R][0:7]n	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC4GX35. Refer to the pin list for the availability of pins in each density.

(2) Refer to HardCopy IV Pin Connections Guidelines and Datasheet for the recommended operating voltage.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	02/05/2010	Initial release.