Pin Information for HardCopy® IV HC4GX15LF780
Version 1.1

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		TDI		TDI			H23			
		TMS		TMS			J21			
		TRST		TRST			G24			
		TCK		TCK			F24			
		TDO		TDO			H24			
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	M21*			
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	N20*			
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	M20*			
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	L18*			
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	K20*			
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	M18*			
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	M19*			
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	L20*			
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	N21*			
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	N18*			
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	N19*			
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	P20*			
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	P19*			
1C	VREFB1CN0	CLK1p	CLK1p				R20			
		nCONFIG		nCONFIG			U20			
		nSTATUS		nSTATUS			U21			
		CONF_DONE		CONF_DONE			V22			
		PORSEL		PORSEL			V19			
		nCE		nCE			V20			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AD23	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AD24	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AF23	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AE23	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AE24	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AF24	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AG26	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AF26	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AH26	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AH25	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AH24	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AG24	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AH22	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AH21	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH23	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG23	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AG21	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AF21	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AF22	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AE22	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AC22	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AC21	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AE21	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AD21	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AB22	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	Y22	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AB23	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AA23	DQS5B	DQ3B/CQn3B	

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3A	VREFB3AN0	IO				DIFFOUT_B15n	W22	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	Y21	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AA20	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	Y20	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AA21	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AB21	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AC20	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AB20	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	W20			
3A	VREFB3AN0	IO				DIFFOUT_B19p	W19			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y19			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y18			
3C	VREFB3CN0	IO				DIFFOUT_B21n	AB18	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B21p	AB17	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AC19	DQSn7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AC18	DQS7B	DQ7B/CQn7B	
3C	VREFB3CN0	IO				DIFFOUT_B23n	AC17	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B23p	AA17	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AE18	DQSn8B	DQSn7B/DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AD18	DQS8B	DQS7B/CQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25n	AE20	DQ8B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25p	AD17	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF19	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE19	DQ8B	DQ7B	
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	Y17			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	Y16			
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AF16			
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AE16			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AA15			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	Y15			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AF15			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AE15			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AH17			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AH16			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AH15			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AG15			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AG14			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AH14			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AH12			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AH13			
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AF12			
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AG12			
4C	VREFB4CN0	IO				DIFFOUT_B36p	AH11	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B36n	AG11	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AG9	DQS9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AH9	DQSn9B		
4C	VREFB4CN0	IO				DIFFOUT_B38p	AF11	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B38n	AH10	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AD12	DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AE12	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40p	AE9	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40n	AE11	DQ10B	DQ11B	

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4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AE10	DQS10B	DQS11B/CQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AF10	DQSn10B	DQSn11B/DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42p	AC12	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42n	AB12	DQ11B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AC11	DQS11B	DQ11B/CQn11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AD11	DQSn11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44p	AB11	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44n	AA11	DQ11B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B45p	W11			
4A	VREFB4AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B45n	W12			
4A	VREFB4AN0	IO				DIFFOUT_B46p	Y10			
4A	VREFB4AN0	IO				DIFFOUT_B46n	Y11			
4A	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AB10	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AC10	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48p	Y9	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48n	AA9	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AB9	DQS12B	DQS15B/CQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AC9	DQSn12B	DQSn15B/DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50p	Y8	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50n	AA8	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AB6	DQS13B	DQ15B/CQn15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AB7	DQSn13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52p	Y7	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52n	W8	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AD8	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AE8	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54p	AC7	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54n	AC8	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AE7	DQS14B	DQS16B/CQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AF7	DQSn14B	DQSn16B/DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56p	AF8	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56n	AG8	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AH6	DQS15B	DQ16B/CQn16B	DQS17B/CQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AH7	DQSn15B	DQ16B	DQSn17B/DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58p	AG6	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58n	AH8	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AG5	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AH5	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60p	AF4	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60n	AH4	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AG3	DQS16B	DQS17B/CQ17B	DQ17B/CQn17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AH3	DQSn16B	DQSn17B/DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62p	AF6	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62n	AE6	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AE5	DQS17B	DQ17B/CQn17B	DQ17B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AF5	DQSn17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64p	AD6	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64n	AC6	DQ17B	DQ17B	DQ17B
		nIO_PULLUP		nIO_PULLUP			AA5			
		nCEO		nCEO			V7			
		DCLK		DCLK			W7			
		nCSO		nCSO			U8			

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		ASDO		ASDO			U9			
7A	VREFB7AN0	IO				DIFFOUT_T1n	C3	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C4	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A3	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B3	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	A2	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B2	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	B5	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	C5	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	A5	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	A4	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	A6	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	B6	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	F6	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	F7	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	D6	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	E6	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	D7	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	F8	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	C8	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	C7	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A8	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	D8	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B8	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	J7	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	G8	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	G6	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	H6	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	K8	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	J8	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	J11	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	K10	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	J9	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	K9	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	H9	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	J10	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	L9			
7A	VREFB7AN0	IO				DIFFOUT_T19p	M9			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	L10			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	M10			
7C	VREFB7CN0	IO				DIFFOUT_T21n	G9	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T21p	G11	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	F10	DQSn7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	G10	DQS7T	DQ7T/CQn7T	
7C	VREFB7CN0	IO				DIFFOUT_T23n	G12	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T23p	H11	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	E11	DQSn8T	DQSn7T/DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	F11	DQS8T	DQS7T/CQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25n	E12	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25p	F12	DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	D9	DQ8T	DQ7T	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	E9	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T27n	B9	DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T27p	C9	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	C10	DQSn9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	D10	DQS9T		
7C	VREFB7CN0	IO				DIFFOUT_T29n	D11	DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T29p	C11	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C12			
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D12			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A11			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B11			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	A12			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	B12			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	B15			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	A15			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	A13			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	A14			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	C14			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	B14			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	J15			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	H15			
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	D15			
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	C15			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	J16			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	G16			
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	B18	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A19	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40p	A20	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40n	B20	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C19	DQS10T	DQS11T/CQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C20	DQSn10T	DQSn11T/DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42p	F17	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42n	E17	DQ11T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	D19	DQS11T	DQ11T/CQn11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	D18	DQSn11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44p	E18	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44n	F18	DQ11T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T45p	J17			
8A	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T45n	J18			
8A	VREFB8AN0	IO				DIFFOUT_T46p	K18			
8A	VREFB8AN0	IO				DIFFOUT_T46n	K19			
8A	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	E20	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	D20	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48p	F20	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48n	F21	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	E21	DQS12T	DQS15T/CQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	D21	DQSn12T	DQSn15T/DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50p	G19	DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50n	G18	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	J20	DQS13T	DQ15T/CQn15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	H20	DQSn13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52p	H18	DQ13T	DQ15T	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8A	VREFB8AN0	IO				DIFFOUT_T52n	J19	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	B23	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	A22	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54p	B21	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54n	A21	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	B24	DQS14T	DQS16T/CQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	A23	DQSn14T	DQSn16T/DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56p	A25	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56n	A24	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	B26	DQS15T	DQ16T/CQn16T	DQS17T/CQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	A26	DQSn15T	DQ16T	DQSn17T/DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58p	A27	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58n	B27	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	G21	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	F22	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60p	G22	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60n	G23	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	F23	DQS16T	DQS17T/CQ17T	DQ17T/CQn17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	E23	DQSn16T	DQSn17T/DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62p	C22	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62n	D22	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	D23	DQS17T	DQ17T/CQn17T	DQ17T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	C23	DQSn17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64p	C25	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64n	C24	DQ17T	DQ17T	DQ17T
QR0		GXB_RX_R0p					AD2			
QR0		GXB_RX_R0n					AD1			
QR0		GXB_TX_R0p					AC4			
QR0		GXB_TX_R0n					AC3			
QR0		GXB_RX_R1p					AB2			
QR0		GXB_RX_R1n					AB1			
QR0		GXB_TX_R1p					AA4			
QR0		GXB_TX_R1n					AA3			
QR0		REFCLK_R0p, GXB_CMURX_R0p					Y2			
QR0		REFCLK_R0n, GXB_CMURX_R0n					Y1			
QR0		REFCLK_R1p, GXB_CMURX_R1p					W4			
QR0		REFCLK_R1n, GXB_CMURX_R1n					W3			
QR0		GXB_RX_R2p					V2			
QR0		GXB_RX_R2n					V1			
QR0		GXB_TX_R2p					U4			
QR0		GXB_TX_R2n					U3			
QR0		GXB_RX_R3p					T2			
QR0		GXB_RX_R3n					T1			
QR0		GXB_TX_R3p					R4			
QR0		GXB_TX_R3n					R3			
QR1		GXB_RX_R4p					P2			
QR1		GXB_RX_R4n					P1			
QR1		GXB_TX_R4p					N4			
QR1		GXB_TX_R4n					N3			
QR1		GXB_RX_R5p					M2			
QR1		GXB_RX_R5n					M1			
QR1		GXB_TX_R5p					L4			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
QR1		GXB_TX_R5n					L3			
QR1		REFCLK_R2p, GXB_CMURX_R2p					K2			
QR1		REFCLK_R2n, GXB_CMURX_R2n					K1			
QR1		REFCLK_R3p, GXB_CMURX_R3p					J4			
QR1		REFCLK_R3n, GXB_CMURX_R3n					J3			
QR1		GXB_RX_R6p					H2			
QR1		GXB_RX_R6n					H1			
QR1		GXB_TX_R6p					G4			
QR1		GXB_TX_R6n					G3			
QR1		GXB_RX_R7p					F2			
QR1		GXB_RX_R7n					F1			
QR1		GXB_TX_R7p					E4			
QR1		GXB_TX_R7n					E3			
		GND					M16			
		GND					V9			
		GND					P14			
		GND					V16			
		GND					P16			
		GND					W13			
		GND					U13			
		GND					N13			
		GND					L13			
		GND					H13			
		GND					V12			
		GND					T12			
		GND					P12			
		GND					M12			
		GND					K12			
		GND					AH2			
		GND					AH27			
		GND					AG4			
		GND					AG7			
		GND					AG10			
		GND					AG13			
		GND					AG16			
		GND					AG19			
		GND					AG22			
		GND					AG25			
		GND					AD7			
		GND					AD10			
		GND					AD13			
		GND					AD16			
		GND					AD19			
		GND					AD22			
		GND					AA7			
		GND					AA10			
		GND					AA13			
		GND					AA16			
		GND					AA19			
		GND					AA22			
		GND					W15			
		GND					W17			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					V8			
		GND					V10			
		GND					V14			
		GND					V18			
		GND					V21			
		GND					U11			
		GND					U15			
		GND					U17			
		GND					T10			
		GND					T14			
		GND					T16			
		GND					T18			
		GND					R11			
		GND					R13			
		GND					R17			
		GND					P18			
		GND					N11			
		GND					N15			
		GND					N17			
		GND					M14			
		GND					L8			
		GND					L11			
		GND					L15			
		GND					L17			
		GND					L19			
		GND					L21			
		GND					K14			
		GND					K16			
		GND					H7			
		GND					H10			
		GND					H16			
		GND					H19			
		GND					H22			
		GND					E7			
		GND					E10			
		GND					E13			
		GND					E16			
		GND					E19			
		GND					E22			
		GND					B1			
		GND					B4			
		GND					B7			
		GND					B10			
		GND					B13			
		GND					B16			
		GND					B19			
		GND					B22			
		GND					B25			
		GND					B28			
		GND					C2			
		GND					D4			
		GND					D3			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					D2			
		GND					E2			
		GND					E1			
		GND					F4			
		GND					F3			
		GND					G2			
		GND					G1			
		GND					H4			
		GND					H3			
		GND					J5			
		GND					J2			
		GND					J1			
		GND					K6			
		GND					K4			
		GND					K3			
		GND					L5			
		GND					L2			
		GND					L1			
		GND					M6			
		GND					M4			
		GND					M3			
		GND					N5			
		GND					N2			
		GND					N1			
		GND					P6			
		GND					P4			
		GND					P3			
		GND					R5			
		GND					R2			
		GND					R1			
		GND					T6			
		GND					T4			
		GND					T3			
		GND					U5			
		GND					U2			
		GND					U1			
		GND					V6			
		GND					V4			
		GND					V3			
		GND					W5			
		GND					W2			
		GND					W1			
		GND					Y6			
		GND					Y4			
		GND					Y3			
		GND					AA2			
		GND					AA1			
		GND					AB4			
		GND					AB3			
		GND					AC2			
		GND					AC1			
		GND					AD4			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					AD3			
		GND					AE2			
		GND					AE1			
		GND					AF2			
		GND					AG2			
		GND					AG1			
		GND					C1			
		VCC					R14			
		VCC					V11			
		VCC					P11			
		VCC					M11			
		VCC					V13			
		VCC					V15			
		VCC					V17			
		VCC					U12			
		VCC					U14			
		VCC					U16			
		VCC					U18			
		VCC					T11			
		VCC					T13			
		VCC					T15			
		VCC					T17			
		VCC					R12			
		VCC					R16			
		VCC					R18			
		VCC					P13			
		VCC					P15			
		VCC					P17			
		VCC					N12			
		VCC					N14			
		VCC					N16			
		VCC					M13			
		VCC					M15			
		VCC					M17			
		VCC					L12			
		VCC					L14			
		VCC					L16			
		VCC					L22			
		VCC					U22			
		VCC					L7			
		VCC					U7			
		VCC					T7			
		VCC					M7			
		VCCPGM					AA24			
		VCCPGM					AB5			
		TEMPDIODEn					G5			
		TEMPDIODEp					H5			
		VCC_CLKIN3C					AB15			
		VCC_CLKIN4C					AB14			
		VCC_CLKIN7C					G14			
		VCC_CLKIN8C					G15			
		VCCA_PLL_B1					AC16			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCA_PLL_T1					F16			
		VCCD_PLL_B1					AC15			
		VCCD_PLL_T1					F15			
		VCCIO1C					K21			
		VCCIO3A					AF25			
		VCCIO3A					AD20			
		VCCIO3A					AC23			
		VCCIO3A					W21			
		VCCIO3C					AF20			
		VCCIO3C					AE17			
		VCCIO3C					AA18			
		VCCIO4A					AF3			
		VCCIO4A					AD9			
		VCCIO4A					AA6			
		VCCIO4A					W9			
		VCCIO4C					AF9			
		VCCIO4C					AD14			
		VCCIO4C					Y12			
		VCCIO7A					M8			
		VCCIO7A					H8			
		VCCIO7A					E8			
		VCCIO7A					C6			
		VCCIO7C					H12			
		VCCIO7C					F9			
		VCCIO7C					D14			
		VCCIO8A					H21			
		VCCIO8A					F19			
		VCCIO8A					C21			
		VCCIO8A					C26			
		VCCIO8C					H17			
		VCCIO8C					E15			
		VCCIO8C					C18			
		VCCPD1C					J22			
		VCCPD3A					W18			
		VCCPD3C					W16			
		VCCPD4A					W10			
		VCCPD4C					W14			
		VCCPD7A					K11			
		VCCPD7C					K13			
		VCCPD8A					K17			
		VCCPD8C					K15			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				K22			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB19			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AB16			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB8			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AA12			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G7			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G13			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G20			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G17			
		NC					D24			
		NC					AB24			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		NC					AC5			
		NC					F5			
		NC					AE4			
		NC					AE3			
		NC					U19			
		NC					T8			
		NC					T9			
		NC					T19			
		NC					T20			
		NC					T21			
		NC					R9			
		NC					R19			
		NC					P9			
		NC					P10			
		NC					N10			
		NC *(4)*					D5			
		NC *(5)*					R21			
		NC *(5)*					P21			
		NC *(5)*					AD15			
		NC *(5)*					R8			
		NC *(5)*					P8			
		NC *(5)*					E14			
		NC *(7)*					J12			
		NC *(7)*					C13			
		NC *(7)*					D13			
		NC *(10)*					AC14			
		NC *(11)*					AC13			
		NC *(11)*					F13			
		NC *(10)*					F14			
		NC *(7)*					AG20			
		NC *(7)*					AH20			
		NC *(7)*					AG18			
		NC *(7)*					AF18			
		NC *(7)*					AH19			
		NC *(7)*					AH18			
		NC *(7)*					AG17			
		NC *(7)*					AF17			
		NC *(7)*					AE14			
		NC *(7)*					AF14			
		NC *(7)*					Y14			
		NC *(7)*					AA14			
		NC *(7)*					AE13			
		NC *(7)*					AF13			
		NC *(7)*					AB13			
		NC *(7)*					Y13			
		NC *(7)*					J13			
		NC *(7)*					H14			
		NC *(7)*					J14			
		NC *(7)*					A10			
		NC *(7)*					A9			
		NC *(7)*					D16			
		NC *(7)*					C16			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		NC *(7)*					A17			
		NC *(7)*					A16			
		NC *(7)*					C17			
		NC *(7)*					B17			
		NC *(7)*					A18			
		NC *(7)*					D17			
		NC *(19)*					D28			
		NC *(19)*					D1			
		NC *(6)*					R15			
		NC *(16)*					E26			
		NC *(16)*					E25			
		NC *(17)*					F28			
		NC *(17)*					F27			
		NC *(16)*					G26			
		NC *(16)*					G25			
		NC *(17)*					H28			
		NC *(17)*					H27			
		NC *(18)*					J26			
		NC *(18)*					J25			
		NC *(18)*					K28			
		NC *(18)*					K27			
		NC *(16)*					L26			
		NC *(16)*					L25			
		NC *(17)*					M28			
		NC *(17)*					M27			
		NC *(16)*					N26			
		NC *(16)*					N25			
		NC *(17)*					P28			
		NC *(17)*					P27			
		NC *(16)*					R26			
		NC *(16)*					R25			
		NC *(17)*					T28			
		NC *(17)*					T27			
		NC *(16)*					U26			
		NC *(16)*					U25			
		NC*(17)*					V28			
		NC *(17)*					V27			
		NC *(18)*					W26			
		NC *(18)*					W25			
		NC *(18)*					Y28			
		NC *(18)*					Y27			
		NC *(16)*					AA26			
		NC *(16)*					AA25			
		NC *(17)*					AB28			
		NC *(17)*					AB27			
		NC *(16)*					AC26			
		NC *(16)*					AC25			
		NC *(17)*					AD28			
		NC *(17)*					AD27			
		NC					AE26			
		NC					AE25			
		NC *(19)*					AF28			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		NC *(8)*					C28			
		NC *(8)*					D27			
		NC *(8)*					D26			
		NC *(8)*					D25			
		NC *(8)*					E28			
		NC *(8)*					E27			
		NC *(8)*					F26			
		NC *(8)*					F25			
		NC *(8)*					G28			
		NC *(8)*					G27			
		NC *(8)*					H26			
		NC *(8)*					H25			
		NC *(8)*					J28			
		NC *(8)*					J27			
		NC *(8)*					J24			
		NC *(8)*					K26			
		NC *(8)*					K25			
		NC *(8)*					K23			
		NC *(8)*					L28			
		NC *(8)*					L27			
		NC *(8)*					L24			
		NC *(8)*					M26			
		NC *(8)*					M25			
		NC *(8)*					M23			
		NC *(8)*					N28			
		NC *(8)*					N27			
		NC *(8)*					N24			
		NC *(8)*					P26			
		NC *(8)*					P25			
		NC *(8)*					P23			
		NC *(8)*					R28			
		NC *(8)*					R27			
		NC *(8)*					R24			
		NC *(8)*					T26			
		NC *(8)*					T25			
		NC *(8)*					T23			
		NC *(8)*					U28			
		NC *(8)*					U27			
		NC *(8)*					U24			
		NC *(8)*					V26			
		NC *(8)*					V25			
		NC *(8)*					C27			
		NC *(8)*					AG27			
		NC *(8)*					AG28			
		NC *(8)*					AF27			
		NC *(8)*					AE27			
		NC *(8)*					AE28			
		NC *(8)*					AD25			
		NC *(8)*					AD26			
		NC *(8)*					AC27			
		NC *(8)*					AC28			
		NC *(8)*					AB25			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		NC *(8)*					AB26			
		NC *(8)*					AA27			
		NC *(8)*					AA28			
		NC *(8)*					Y23			
		NC *(8)*					Y25			
		NC *(8)*					Y26			
		NC *(8)*					W24			
		NC *(8)*					W27			
		NC *(8)*					W28			
		NC *(8)*					V23			
		NC *(20)*					R23			
		NC *(20)*					N23			
		NC *(14)*					V24			
		NC *(14)*					L23			
		NC *(15)*					W23			
		NC *(15)*					Y24			
		NC *(15)*					J23			
		NC *(15)*					K24			
		NC *(21)*					U23			
		NC *(21)*					M24			
		NC *(22)*					T24			
		NC *(22)*					P24			
		NC *(13)*					N22			
		NC *(13)*					P22			
		NC *(13)*					R22			
		NC *(9)*					T22			
		NC *(9)*					M22			
		NC *(9)*					R10			
		NC *(9)*					U10			
		NC *(3)*		MSEL2			N8			
		NC *(3)*		MSEL1			K7			
		NC *(3)*		MSEL0			N9			
		VCCAUX					E24			
		VCCAUX					AC24			
		VCCAUX					AD5			
		VCCAUX					E5			
		VCCA_R					R6			
		VCCA_R					N6			
		VCCH_GXBR0					V5			
		VCCH_GXBR1					L6			
		VCCL_GXBR0					Y5			
		VCCL_GXBR0					W6			
		VCCL_GXBR1					J6			
		VCCL_GXBR1					K5			
		VCCR_R					U6			
		VCCR_R					M5			
		VCCT_R					T5			
		VCCT_R					P5			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780 *(12)*	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCHIP_R					N7			
		VCCHIP_R					P7			
		VCCHIP_R					R7			
		RREF_R0					AF1			

Notes:

(1) These pins should be connected on the board to properly configure the FPGA prototype. For more information, refer to Stratix® IV device pin table.
(2) The individual index number of the pin in this column may not be the same as its companion Stratix IV device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.
(6) This NC pin is a DNU pin in the Stratix IV device and must be left floating.
(7) This NC pin is IO pin in the Stratix IV device and can be left unconnected.
(8) This NC pin is GND pin in the Stratix IV device and should be connected to the ground for the FPGA prototype.
(9) This NC pin is VCC pin in the Stratix IV device and should be connected to VCC power for the FPGA prototype.
(10) This NC pin is a VCCD_PLL in the Stratix IV device and should be connected to the VCCD_PLL power for the FPGA prototype.
(11) This NC pin is a VCCA_PLL in the Stratix IV device and should be connected to the VCCA_PLL power for the FPGA prototype.
(12) These pins (pin with *) should be connected for the FPGA prototype. These pins cannot be used as regular I/O.
(13) This NC pin is VCCHIP in the Stratix IV device and may be connected to GND for the FPGA prototype.
(14) This NC pin is VCCH_GXB in the Stratix IV device and should be connected to GND for the FPGA prototype.
(15) This NC pin is VCCL_GXB in the Stratix IV device and should be connected to GND for the FPGA prototype.
(16) This NC pin is GXB_TX in the Stratix IV device and should be left floating for the FPGA prototype.
(17) This NC pin is GXB_RX in the Stratix IV device and should be connected to GND through a 10-kΩ resistor for FPGA prototype.
(18) This NC pin is REFCLK, GXB_CMURX in the Stratix IV device and should be connected to GND through a 10-kΩ resistor for FPGA prototype.
(19) This NC pin is a RREF pin in the Stratix IV device and should be connected to GND for the FPGA prototype.
(20) This NC pin is VCCA in the Stratix IV device and should be connected to GND for the FPGA prototype.
(21) This NC pin is VCCR in the Stratix IV device and should be connected to GND for the FPGA prototype.
(22) This NC pin is VCCT in the Stratix IV device and should be connected to GND for the FPGA prototype.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Clock and PLL Pins
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, ,L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
		Optional/Dual-Purpose Configuration Pins
nCSO	I/O, Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	I/O, Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin for HardCopy IV.
		Differential I/O Pins
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

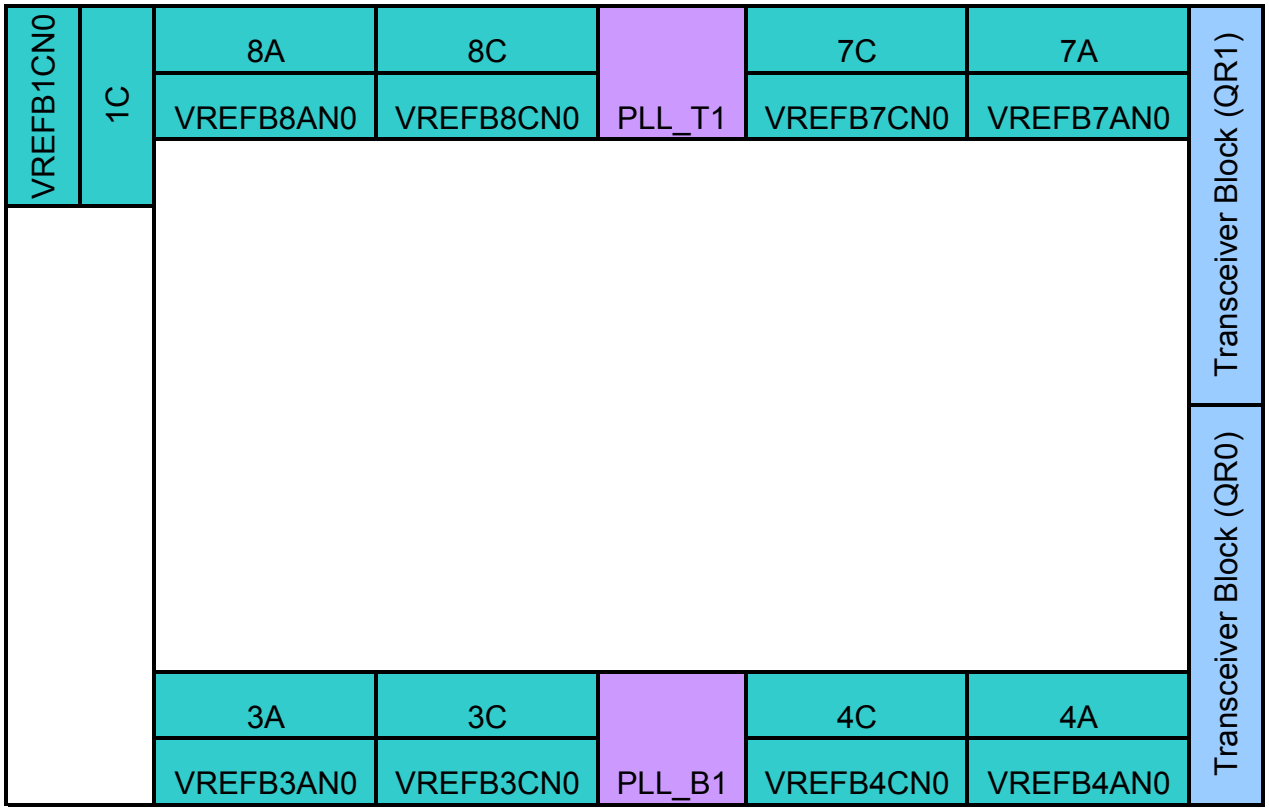
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	External Memory Interface Pins	
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
	Reference Pins	
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
	Supply Pins	
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5V, 3.3V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
VREFB[1:8][A,C]N0, VREFB[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
	Transceiver (I/O Banks) Pins	
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p GXB_CMURX_[L,R][0:7]p	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n GXB_CMURX_[L,R][0:7]n	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
GXB_CMUTX_[L,R][0:7]p GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC4GX35. Refer to the pin list for the availability of pins in each density.

(2) For the recommended power supply operating conditions, refer to HardCopy IV handbook and for the recommended transceiver power supply operating conditions, refer to the Stratix IV GX pin connections guidelines and datasheet.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	7/10/2009	Preliminary release.
1.1	7/30/2010	Initial release.