Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		TDI		TDI			J20			
		TMS		TMS			G23			
		TRST		TRST			D26			
		TCK		TCK			D25			
		TDO		TDO			E25			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	H23			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	H22			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	D28			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G25	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G24	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C28	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	F26	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	F25	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	E28	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E27	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	H25	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	H24	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	G27	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	G26	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K24	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K23	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	F28	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G28	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K22	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K21	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	L21	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	L20	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	H28	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	H27	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	L23			
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L22			
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	K26			
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	K25			
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	L24			
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	M23			
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	L26	DQSn5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	L25	DQS5L		
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	N21	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	N20	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	J28	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	K28	DQ5L		
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	N23	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	N22	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	L28	DQSn6L	DQ5L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	K27	DQS6L	DQ5L/CQn5L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	P21	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	P20	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	M26	DQSn7L	DQSn5L/DQ5L	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	M25	DQS7L	DQS5L/CQ5L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	N25	DQ7L	DQ5L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	N24	DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	M28	DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	L27	DQ7L	DQ5L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	P26			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	P25			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	N28			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	N27			
1C	VREFB1CN0	CLK1n	CLK1n				P28			
1C	VREFB1CN0	CLK1p	CLK1p				P27			
2C	VREFB2CN0	CLK3p	CLK3p				T28			
2C	VREFB2CN0	CLK3n	CLK3n				R28			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	T27			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	U28			
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	R25			
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	R26			
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	T25	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	U26	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	R20	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	T21	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	U27	DQS8L	DQS10L/CQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	V28	DQSn8L	DQSn10L/DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	T22	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	T23	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	U25	DQS9L	DQ10L/CQn10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	V26	DQSn9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	T20	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	U21	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	W27	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	W28	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	U23	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	U24	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	V25	DQS10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	W26	DQSn10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	V22			
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	V23			
2A	VREFB2AN0	IO			DIFFIO_RX_L21p	DIFFOUT_L41p	Y27			
2A	VREFB2AN0	IO			DIFFIO_RX_L21n	DIFFOUT_L41n	Y28			
2A	VREFB2AN0	IO			DIFFIO_TX_L21p	DIFFOUT_L42p	W24			
2A	VREFB2AN0	IO			DIFFIO_TX_L21n	DIFFOUT_L42n	W25			
2A	VREFB2AN0	IO			DIFFIO_RX_L22p	DIFFOUT_L43p	AB28	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L22n	DIFFOUT_L43n	AA28	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22p	DIFFOUT_L44p	W22	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22n	DIFFOUT_L44n	W23	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	AB27	DQS11L	DQS13L/CQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	AC28	DQSn11L	DQSn13L/DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	V20	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	W21	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC27	DQS12L	DQ13L/CQn13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AD28	DQSn12L	DQ13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	Y25	DQ12L	DQ13L	DQ14L

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	Y26	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AA25	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AA26	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AB25	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AC26	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AE27	DQS13L	DQS14L/CQ14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AE28	DQSn13L	DQSn14L/DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	Y23	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	Y24	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AF27	DQS14L	DQ14L/CQn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AF28	DQSn14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	AB23	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AB24	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AH27			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AG28			
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AC25			
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AD26			
		nCONFIG		nCONFIG			AA22			
		nSTATUS		nSTATUS			AC23			
		CONF_DONE		CONF_DONE			AC24			
		PORSEL		PORSEL			W20			
		nCE		nCE			Y21			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AB21	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AC21	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AD22	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AC22	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AA20	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AB20	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE23	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD23	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AE24	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AE25	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AG23	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AF24	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AF25	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AF26	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH25	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG25	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AG26	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AH26	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH24	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH23	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AG22	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AH22	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AF22	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AE22	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AH20	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AH21	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AG19	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AG20	DQ5B	DQ3B	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AF19	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AE20	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AD19	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AC19	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD20	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AA19			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AB18			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y18			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y17			
3C	VREFB3CN0	IO				DIFFOUT_B21n	AA17	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B21p	AA16	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AC18	DQSn7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AB17	DQS7B	DQ7B/CQn7B	
3C	VREFB3CN0	IO				DIFFOUT_B23n	Y15	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B23p	Y16	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AH19	DQSn8B	DQSn7B/DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AH18	DQS8B	DQS7B/CQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25n	AE17	DQ8B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25p	AG17	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF18	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE18	DQ8B	DQ7B	
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	AD17			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	AD16			
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AF16			
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AE16			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AC16			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	AB15			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AF15			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AE15			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AH17			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AG16			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AH16			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AH15			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AG14			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AH14			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AH12			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AH13			
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AF14			
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AG13			
4C	VREFB4CN0	IO				DIFFOUT_B36p	Y13	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B36n	Y14	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AA13	DQS9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AA14	DQSn9B		
4C	VREFB4CN0	IO				DIFFOUT_B38p	AB12	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B38n	AB11	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AD13	DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AE12	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40p	AE13	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40n	AE14	DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AC12	DQS10B	DQS11B/CQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AD11	DQSn10B	DQSn11B/DQ11B	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
4C	VREFB4CN0	IO				DIFFOUT_B42p	AF12	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42n	AH11	DQ11B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AE11	DQS11B	DQ11B/CQn11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AF11	DQSn11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44p	AH10	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44n	AG11	DQ11B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B45p	Y12			
4A	VREFB4AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B45n	AA11			
4A	VREFB4AN0	IO				DIFFOUT_B46p	Y10			
4A	VREFB4AN0	IO				DIFFOUT_B46n	Y11			
4A	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AC10	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AD10	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48p	AB9	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48n	AB10	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AE9	DQS12B	DQS15B/CQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AE10	DQSn12B	DQSn15B/DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50p	AF10	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50n	AF9	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AG8	DQS13B	DQ15B/CQn15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AH8	DQSn13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52p	AH9	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52n	AG10	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AG7	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AH6	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54p	AH5	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54n	AH7	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AF6	DQS14B	DQS16B/CQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AG5	DQSn14B	DQSn16B/DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56p	AE7	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56n	AE8	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AE6	DQS15B	DQ16B/CQn16B	DQS17B/CQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AF7	DQSn15B	DQ16B	DQSn17B/DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58p	AD7	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58n	AD8	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AG4	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AH4	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60p	AF3	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60n	AF4	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AH2	DQS16B	DQS17B/CQ17B	DQ17B/CQn17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AH3	DQSn16B	DQSn17B/DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62p	AC6	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62n	AC8	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AA8	DQS17B	DQ17B/CQn17B	DQ17B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AB7	DQSn17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64p	Y9	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64n	AA10	DQ17B	DQ17B	DQ17B
		nIO_PULLUP		nIO_PULLUP			Y8			
		nCEO		nCEO			W6			
		DCLK		DCLK			Y6			
		nCSO		nCSO			W7			
		ASDO		ASDO			Y7			
7A	VREFB7AN0	IO				DIFFOUT_T1n	F7	DQ1T	DQ1T	DQ1T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
7A	VREFB7AN0	IO				DIFFOUT_T1p	G8	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	E7	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	F8	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	G9	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	H9	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D6	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E6	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	D5	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	F6	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	C4	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	C5	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	A2	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	B3	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	A3	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	B4	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	A5	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	A4	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A6	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	B6	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	C7	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	D7	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B7	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B9	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	A8	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	B10	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	A9	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	D10	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	E9	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	F10	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	E10	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	C10	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	D9	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	H10			
7A	VREFB7AN0	IO				DIFFOUT_T19p	G11			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	J11			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	J12			
7C	VREFB7CN0	IO				DIFFOUT_T21n	A11	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T21p	A10	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	C11	DQSn7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	D11	DQS7T	DQ7T/CQn7T	
7C	VREFB7CN0	IO				DIFFOUT_T23n	B12	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T23p	D12	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	E12	DQSn8T	DQSn7T/DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	F11	DQS8T	DQS7T/CQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25n	F13	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25p	E13	DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C13	DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D13	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T27n	H12	DQ9T		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
7C	VREFB7CN0	IO				DIFFOUT_T27p	G12	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	G14	DQSn9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	H13	DQS9T		
7C	VREFB7CN0	IO				DIFFOUT_T29n	J14	DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T29p	J13	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C14			
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D14			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A14			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B13			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	A12			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	A13			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	B15			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	A15			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	B16			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	A16			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	D15			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	C15			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	J15			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	H15			
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	E16			
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D16			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	J16			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	H16			
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	A19	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A18	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40p	A17	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40n	B18	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C18	DQS10T	DQS11T/CQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C17	DQSn10T	DQSn11T/DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42p	G17	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42n	D17	DQ11T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	F17	DQS11T	DQ11T/CQn11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	E18	DQSn11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44p	D18	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44n	F18	DQ11T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T45p	J17			
8A	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T45n	H18			
8A	VREFB8AN0	IO				DIFFOUT_T46p	H19			
8A	VREFB8AN0	IO				DIFFOUT_T46n	J18			
8A	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	C19	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	B19	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48p	A20	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48n	A21	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	C20	DQS12T	DQS15T/CQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	B21	DQSn12T	DQSn15T/DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50p	F19	DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50n	G19	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	E19	DQS13T	DQ15T/CQn15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	D19	DQSn13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52p	D20	DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52n	F20	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	D21	DQ14T	DQ16T	DQ17T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8A	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	C21	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54p	A22	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54n	A23	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	C22	DQS14T	DQS16T/CQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	B22	DQSn14T	DQSn16T/DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56p	H21	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56n	E21	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	E22	DQS15T	DQ16T/CQn16T	DQS17T/CQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	D22	DQSn15T	DQ16T	DQSn17T/DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58p	G21	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58n	F21	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	B24	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	A24	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60p	D24	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60n	C25	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	D23	DQS16T	DQS17T/CQ17T	DQ17T/CQn17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C24	DQSn16T	DQSn17T/DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62p	A26	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62n	C26	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	B25	DQS17T	DQ17T/CQn17T	DQ17T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	A25	DQSn17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64p	A27	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64n	B27	DQ17T	DQ17T	DQ17T
QR0		GXB_RX_R0p					AD2			
QR0		GXB_RX_R0n					AD1			
QR0		GXB_TX_R0p					AC4			
QR0		GXB_TX_R0n					AC3			
QR0		GXB_RX_R1p					AB2			
QR0		GXB_RX_R1n					AB1			
QR0		GXB_TX_R1p					AA4			
QR0		GXB_TX_R1n					AA3			
QR0		REFCLK_R0p, GXB_CMURX_R0p					Y2			
QR0		REFCLK_R0n, GXB_CMURX_R0n					Y1			
QR0		REFCLK_R1p, GXB_CMURX_R1p					W4			
QR0		REFCLK_R1n, GXB_CMURX_R1n					W3			
QR0		GXB_RX_R2p					V2			
QR0		GXB_RX_R2n					V1			
QR0		GXB_TX_R2p					U4			
QR0		GXB_TX_R2n					U3			
QR0		GXB_RX_R3p					T2			
QR0		GXB_RX_R3n					T1			
QR0		GXB_TX_R3p					R4			
QR0		GXB_TX_R3n					R3			
QR1		GXB_RX_R4p					P2			
QR1		GXB_RX_R4n					P1			
QR1		GXB_TX_R4p					N4			
QR1		GXB_TX_R4n					N3			
QR1		GXB_RX_R5p					M2			
QR1		GXB_RX_R5n					M1			
QR1		GXB_TX_R5p					L4			
QR1		GXB_TX_R5n					L3			
QR1		REFCLK_R2p, GXB_CMURX_R2p					K2			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
QR1		REFCLK_R2n, GXB_CMURX_R2n					K1			
QR1		REFCLK_R3p, GXB_CMURX_R3p					J4			
QR1		REFCLK_R3n, GXB_CMURX_R3n					J3			
QR1		GXB_RX_R6p					H2			
QR1		GXB_RX_R6n					H1			
QR1		GXB_TX_R6p					G4			
QR1		GXB_TX_R6n					G3			
QR1		GXB_RX_R7p					F2			
QR1		GXB_RX_R7n					F1			
QR1		GXB_TX_R7p					E4			
QR1		GXB_TX_R7n					E3			
		GND					M17			
		GND					W8			
		GND					P15			
		GND					AG3			
		GND					AG6			
		GND					AG9			
		GND					AG12			
		GND					AG15			
		GND					AG18			
		GND					AG21			
		GND					AG24			
		GND					AG27			
		GND					AD6			
		GND					AD9			
		GND					AD12			
		GND					AD15			
		GND					AD18			
		GND					AD21			
		GND					AD24			
		GND					AD27			
		GND					AA6			
		GND					AA9			
		GND					AA12			
		GND					AA15			
		GND					AA18			
		GND					AA21			
		GND					AA24			
		GND					AA27			
		GND					W12			
		GND					W14			
		GND					W16			
		GND					W18			
		GND					W19			
		GND					V9			
		GND					V11			
		GND					V13			
		GND					V15			
		GND					V17			
		GND					V19			
		GND					V21			
		GND					V24			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					V27			
		GND					U12			
		GND					U14			
		GND					U16			
		GND					U18			
		GND					T11			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					R12			
		GND					R16			
		GND					R18			
		GND					R21			
		GND					R24			
		GND					R27			
		GND					P11			
		GND					P13			
		GND					P17			
		GND					P19			
		GND					N12			
		GND					N14			
		GND					N16			
		GND					N18			
		GND					M11			
		GND					M13			
		GND					M15			
		GND					M19			
		GND					M21			
		GND					M24			
		GND					M27			
		GND					L8			
		GND					L12			
		GND					L14			
		GND					L16			
		GND					L18			
		GND					K11			
		GND					K13			
		GND					K15			
		GND					K17			
		GND					K19			
		GND					J21			
		GND					J24			
		GND					J27			
		GND					H5			
		GND					H8			
		GND					H11			
		GND					H14			
		GND					H17			
		GND					H20			
		GND					F24			
		GND					F27			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					E5			
		GND					E8			
		GND					E11			
		GND					E14			
		GND					E17			
		GND					E20			
		GND					E23			
		GND					C27			
		GND					B2			
		GND					B5			
		GND					B8			
		GND					B11			
		GND					B14			
		GND					B17			
		GND					B20			
		GND					B23			
		GND					B26			
		GND					C2			
		GND					C1			
		GND					D4			
		GND					D3			
		GND					D2			
		GND					E2			
		GND					E1			
		GND					F4			
		GND					F3			
		GND					G2			
		GND					G1			
		GND					H4			
		GND					H3			
		GND					J2			
		GND					J1			
		GND					K4			
		GND					K3			
		GND					L5			
		GND					L2			
		GND					L1			
		GND					M6			
		GND					M4			
		GND					M3			
		GND					N7			
		GND					N5			
		GND					N2			
		GND					N1			
		GND					P8			
		GND					P6			
		GND					P4			
		GND					P3			
		GND					R7			
		GND					R5			
		GND					R2			
		GND					R1			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					T8			
		GND					T6			
		GND					T4			
		GND					T3			
		GND					U5			
		GND					U2			
		GND					U1			
		GND					V6			
		GND					V4			
		GND					V3			
		GND					W2			
		GND					W1			
		GND					Y4			
		GND					Y3			
		GND					AA2			
		GND					AA1			
		GND					AB4			
		GND					AB3			
		GND					AC2			
		GND					AC1			
		GND					AD4			
		GND					AD3			
		GND					AE2			
		GND					AE1			
		GND					AF2			
		GND					AG2			
		GND					AG1			
		VCC					P14			
		VCC					V12			
		VCC					V14			
		VCC					V16			
		VCC					V18			
		VCC					U11			
		VCC					U13			
		VCC					U15			
		VCC					U17			
		VCC					T12			
		VCC					T14			
		VCC					T16			
		VCC					T18			
		VCC					R11			
		VCC					R13			
		VCC					R15			
		VCC					R17			
		VCC					P12			
		VCC					P16			
		VCC					P18			
		VCC					N11			
		VCC					N13			
		VCC					N15			
		VCC					N17			
		VCC					M12			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCC					M14			
		VCC					M16			
		VCC					M18			
		VCC					L11			
		VCC					L13			
		VCC					L15			
		VCC					L17			
		VCC					U7			
		VCC					U8			
		VCC					M7			
		VCC					M8			
		VCCPGM					Y20			
		VCCPGM					W9			
		TEMPDIODEn					H7			
		TEMPDIODEp					G6			
		VCC_CLKIN3C					AD14			
		VCC_CLKIN4C					AC13			
		VCC_CLKIN7C					F14			
		VCC_CLKIN8C					F16			
		VCCA_PLL_B1					AC14			
		VCCA_PLL_L2					R23			
		VCCA_PLL_T1					E15			
		VCCD_PLL_B1					AC15			
		VCCD_PLL_L2					P23			
		VCCD_PLL_T1					F15			
		VCCIO1A					J23			
		VCCIO1A					H26			
		VCCIO1A					E26			
		VCCIO1C					P24			
		VCCIO1C					N26			
		VCCIO2A					AD25			
		VCCIO2A					AB26			
		VCCIO2A					AA23			
		VCCIO2C					T24			
		VCCIO2C					T26			
		VCCIO3A					AF20			
		VCCIO3A					AF23			
		VCCIO3A					AC20			
		VCCIO3A					Y19			
		VCCIO3C					AF17			
		VCCIO3C					AC17			
		VCCIO4A					AF5			
		VCCIO4A					AF8			
		VCCIO4A					AC7			
		VCCIO4A					AC9			
		VCCIO4C					AF13			
		VCCIO4C					AC11			
		VCCIO7A					J10			
		VCCIO7A					F9			
		VCCIO7A					C6			
		VCCIO7A					C9			
		VCCIO7C					F12			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCIO7C					C12			
		VCCIO8A					J19			
		VCCIO8A					F22			
		VCCIO8A					E24			
		VCCIO8A					C23			
		VCCIO8C					G18			
		VCCIO8C					C16			
		VCCPD1A					L19			
		VCCPD1C					N19			
		VCCPD2A					U19			
		VCCPD2C					R19			
		VCCPD3A					W17			
		VCCPD3C					W15			
		VCCPD4A					W11			
		VCCPD4C					W13			
		VCCPD7A					K12			
		VCCPD7C					K14			
		VCCPD8A					K18			
		VCCPD8C					K16			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				J22			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				M22			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				Y22			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				U22			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB19			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AB16			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB8			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AB13			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G10			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G13			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G20			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G16			
		NC					F23			
		NC					AE26			
		NC					AB6			
		NC					J8			
		NC					AE4			
		NC					AE3			
		NC					AE5			
		NC					AD5			
		NC					AC5			
		NC					AB5			
		NC					AA5			
		NC					Y5			
		NC					W5			
		NC					W10			
		NC					V7			
		NC					V8			
		NC					V10			
		NC					U9			
		NC					U10			
		NC					U20			
		NC					T9			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		NC					T10			
		NC					N10			
		NC					M9			
		NC					M10			
		NC					M20			
		NC					L7			
		NC					L9			
		NC					L10			
		NC					K5			
		NC					K6			
		NC					K7			
		NC					K8			
		NC					K10			
		NC					K20			
		NC					J5			
		NC					J6			
		NC					G5			
		NC					F5			
		NC					C3			
		NC					B1			
		NC *(4)*					H6			
		NC *(5)*					R22			
		NC *(5)*					P22			
		NC *(5)*					AB14			
		NC *(5)*					R10			
		NC *(5)*					P10			
		NC *(5)*					G15			
		NC *(7)*					D1			
		NC *(6)*					R14			
		NC *(3)*		MSEL2			J7			
		NC *(3)*		MSEL1			J9			
		NC *(3)*		MSEL0			K9			
		VCCAUX					G22			
		VCCAUX					AB22			
		VCCAUX					AA7			
		VCCAUX					G7			
		VCCA_R					N6			
		VCCA_R					T5			
		VCCH_GXBR0					V5			
		VCCH_GXBR1					L6			
		VCCL_GXBR0					R8			
		VCCL_GXBR0					T7			
		VCCL_GXBR1					N8			
		VCCL_GXBR1					P7			
		VCCR_R					M5			
		VCCR_R					R6			
		VCCT_R					P5			
		VCCT_R					U6			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F780	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCHIP_R					N9			
		VCCHIP_R					P9			
		VCCHIP_R					R9			
		RREF_R0					AF1			

Notes:

(1) These pins should be connected on the board to properly configure the FPGA prototype. For more information, refer to Stratix® IV device pin table.
(2) The individual index number of the pin in this column may not be the same as its companion, the Stratix IV device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.
(6) This NC pin is a DNU pin in the Stratix IV device and must be left floating.
(7) This NC pin is a RREF pin in the Stratix IV device and should be connected to GND for the FPGA prototype.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, ,L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
	Optional/Dual-Purpose Configuration Pins	
nCSO	I/O, Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	I/O, Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin for HardCopy IV.
	Differential I/O Pins	
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signa for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

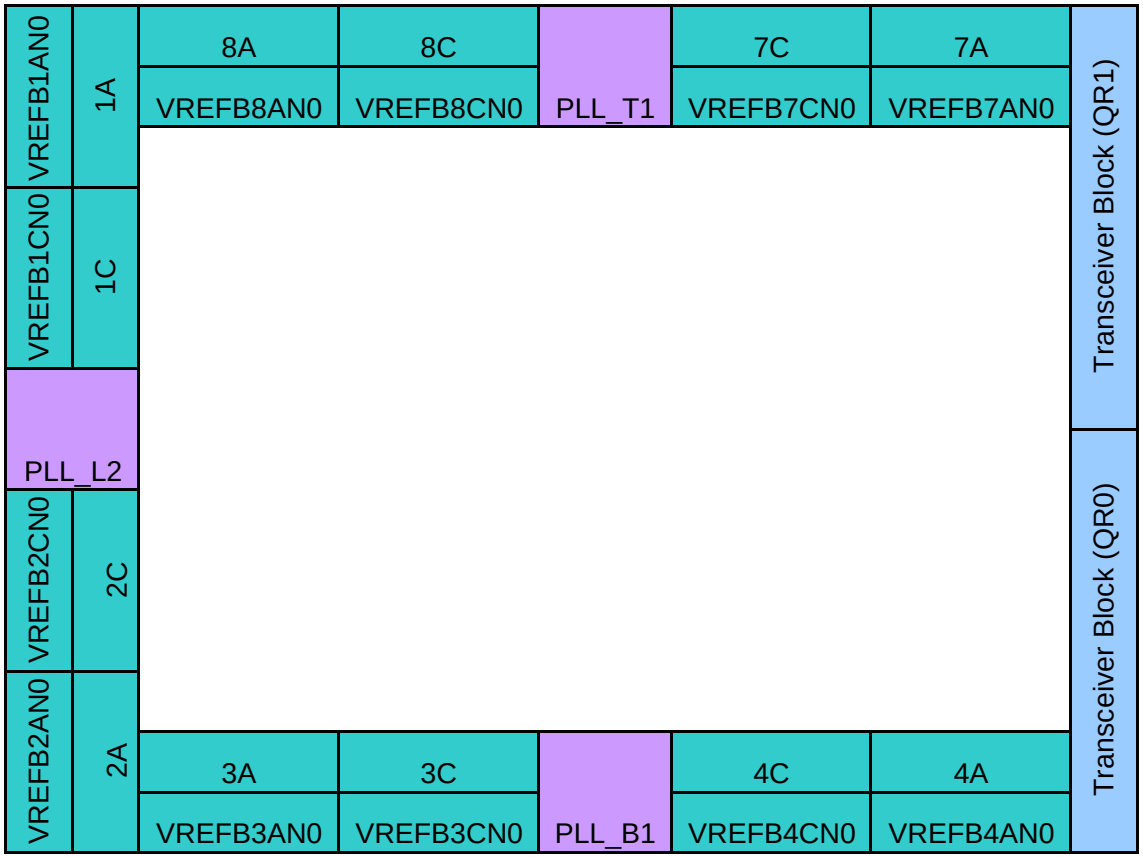
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		External Memory Interface Pins
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
		Reference Pins
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
		Supply Pins
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18),SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
VREFB[1:8][A,C]N0, VREFB[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
		Transceiver (I/O Banks) Pins
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
REFCLK_[L,R][0:7]p GXB_CMURX_[L,R][0:7]p	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n GXB_CMURX_[L,R][0:7]n	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC4GX35. Refer to the pin list for the availability of pins in each density.

(2) For the recommended power supply operating conditions, refer to HardCopy IV handbook and for the recommended transceiver power supply operating conditions, refer to the Stratix IV GX pin connections guidelines and datasheet.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	7/10/2009	Preliminary release.
1.1	7/30/2010	Initial release.