



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
		TDI		TDI			F24		
		TMS		TMS			H22		
		TRST		TRST			D26		
		TCK		TCK			C26		
		TDO		TDO			G24		
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	F26		
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	F25		
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C28		
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27		
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G26	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G25	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	DQSn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C27	DQS1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	H25	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	J24	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	D28	DQS2L	DQS1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E28	DQS2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	J23	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J22	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	F28	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	F27	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K21	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K20	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	G28	DQS3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G27	DQS3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K26	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K25	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26		
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25		
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	M23		
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	M22		
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	L26	DQS5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	L25	DQS5L	
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	M21	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	M20	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	K28	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	L28	DQ5L	
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	N21	DQ6L	DQ5L
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	N20	DQ6L	DQ5L
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	M26	DQS6L	DQ5L
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	M25	DQS6L	DQ5L/CQn5L
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	N25	DQ6L	DQ5L
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	M24	DQ6L	DQ5L
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	M28	DQS7L	DQS5L/DQ5L
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	M27	DQS7L	DQS5L/CQ5L
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	N23	DQ7L	DQ5L
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	P23	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	P25	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	N24	DQ7L	DQ5L
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	P20		
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	P19		
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	N27		
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	N26		
1C	VREFB1CN0	CLK1n	CLK1n				N28		
1C	VREFB1CN0	CLK1p	CLK1p				P28		



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2C	VREFB2CN0	CLK3p	CLK3p				R27		
2C	VREFB2CN0	CLK3n	CLK3n				R28		
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	U28		
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	T28		
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	R20		
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	R21		
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	R26	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	T27	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	T25	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	R25	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	V27	DQS8L	DQS10L/CQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	V28	DQSn8L	DQSn10L/DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	T20	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	T21	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	V26	DQS9L	DQ10L/CQn10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	U26	DQSn9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	T24	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	U25	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	W27	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	W28	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	T22	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	T23	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	V24	DQS10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	V25	DQSn10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	V23		
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	U23		
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	Y25		
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	Y26		
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	V20	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	V21	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC28	DQS12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AB28	DQSn12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AA25	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	AA26	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AB25	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AB26	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AC25	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AC26	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AD27	DQS13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AD28	DQSn13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	W20	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	W21	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AG28	DQS14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AF28	DQSn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	Y23	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AA24	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AE27		
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AE28		
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AA23		
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AB24		
		nCONFIG		nCONFIG			W19		
		nSTATUS		nSTATUS			AD25		
		CONF_DONE		CONF_DONE			AE26		
		PORSEL		PORSEL			AB23		
		nCE		nCE			Y20		



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3A	VREFB3AN0	IO				DIFFOUT_B1n	AF26	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AH27	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AH25	DQS1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AG25	DQS1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AG27	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AH26	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE22	DQS2B	DQS1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD22	DQS2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AB20	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AB21	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AD21	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AC21	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AC20	DQ5B	DQ2B
3A	VREFB3AN0	IO				DIFFOUT_B13p	AG21	DQ5B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21	DQS5B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21	DQS5B	DQ2B/CQn2B
3A	VREFB3AN0	IO				DIFFOUT_B15n	AF20	DQ5B	DQ2B
3A	VREFB3AN0	IO				DIFFOUT_B15p	AE20	DQ5B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AD19	DQS6B	DQS2B/DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AC19	DQS6B	DQS2B/CQ2B
3A	VREFB3AN0	IO				DIFFOUT_B17n	AB19	DQ6B	DQ2B
3A	VREFB3AN0	IO				DIFFOUT_B17p	AA19	DQ6B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19	DQ6B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD18	DQ6B	DQ2B
3C	VREFB3CN0	IO				DIFFOUT_B21n	AF19	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B21p	AG19	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AH19	DQS7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AG18	DQS7B	DQ7B/CQn7B
3C	VREFB3CN0	IO				DIFFOUT_B23n	AH17	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B23p	AH18	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AF17	DQS8B	DQS7B/DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AE18	DQS8B	DQS7B/CQ7B
3C	VREFB3CN0	IO				DIFFOUT_B25n	AE16	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B25p	AD16	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF16	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE17	DQ8B	DQ7B
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	AC17		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	AB17		
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AC16		
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AB16		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AA15		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	Y15		
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AH16		
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AG16		
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AH15		
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AG15		
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AF15		
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AE15		
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AE14		
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AF14		
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AG13		
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AH14		
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AG12		
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AH13		
4C	VREFB4CN0	IO				DIFFOUT_B36p	Y13	DQ9B	



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4C	VREFB4CN0	IO				DIFFOUT_B36n	Y14	DQ9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AD13	DQS9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AE13	DQSn9B	
4C	VREFB4CN0	IO				DIFFOUT_B38p	AA13	DQ9B	
4C	VREFB4CN0	IO				DIFFOUT_B38n	AB13	DQ9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AG10	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AH10	DQ10B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B40p	AH11	DQ10B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B40n	AH12	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AF10	DQS10B	DQS11B/CQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AF11	DQSn10B	DQSn11B/DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42p	AF12	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42n	AC12	DQ11B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AD12	DQS11B	DQ11B/CQn11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AE12	DQSn11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B44p	AC11	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B44n	AE11	DQ11B	DQ11B
4A	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AG9	DQ12B	DQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AH8	DQ12B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B48p	AE10	DQ12B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B48n	AH9	DQ12B	DQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AE9	DQS12B	DQS16B/CQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AF9	DQSn12B	DQSn16B/DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B50p	AF8	DQ13B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B50n	AE8	DQ13B	DQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AG7	DQS13B	DQ16B/CQn16B
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AH7	DQSn13B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B52p	AG6	DQ13B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B52n	AH6	DQ13B	DQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AE6	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AF6	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60p	AE4	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60n	AE7	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AE5	DQS16B	DQS17B/CQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AF5	DQSn16B	DQSn17B/DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62p	AB8	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62n	AC8	DQ17B	DQ17B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AC7	DQS17B	DQ17B/CQn17B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AD7	DQSn17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64p	AB7	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64n	AD6	DQ17B	DQ17B
		nIO_PULLUP		nIO_PULLUP			AE3		
		nCEO		nCEO			AB5		
		DCLK		DCLK			AC5		
		nCSO		nCSO			AD4		
		ASDO		ASDO			AA6		
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AC3		
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AC4		
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AF1		
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AE2		
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AB3	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AB4	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AG1	DQSn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AF2	DQS1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	Y6	DQ1R	DQ1R



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	Y7	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AE1	DQSn2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AD1	DQS2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AA4	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	Y5	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AC1	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AC2	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	Y3	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	Y4	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AB1	DQSn3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AB2	DQS3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	W8	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	W9	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AA1		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	Y2		
5C	VREFB5CN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	U6		
5C	VREFB5CN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	U7		
5C	VREFB5CN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	V3	DQSn5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	V4	DQS5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	U8	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	U9	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	W1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	V1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	T4	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	U5	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	U3	DQSn6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	U4	DQS6R	DQ5R/CQn5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	T8	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	T9	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	T2	DQSn7R	DQSn5R/DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	T3	DQS7R	DQS5R/CQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	T6	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	R6	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	R4	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	T5	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	R9		
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	R10		
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R14n	DIFFOUT_R28n	U1		
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R14p	DIFFOUT_R28p	U2		
5C	VREFB5CN0	CLK8n	CLK8n				T1		
5C	VREFB5CN0	CLK8p	CLK8p				R1		
6C	VREFB6CN0	CLK10p	CLK10p				P2		
6C	VREFB6CN0	CLK10n	CLK10n				P1		
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R15p	DIFFOUT_R29p	M1		
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R15n	DIFFOUT_R29n	N1		
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R15p	DIFFOUT_R30p	P9		
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R15n	DIFFOUT_R30n	P8		
6C	VREFB6CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R31p	N4	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R31n	P4	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R32p	N7	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R32n	N6	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R33p	P3	DQS8R	DQS10R/CQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R33n	N2	DQSn8R	DQSn10R/DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R34p	N5	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R34n	M4	DQ9R	DQ10R



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
6C	VREFB6CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R35p	L2	DQS9R	DQ10R/CQn10R
6C	VREFB6CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R35n	L1	DQS9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R36p	N9	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R36n	N8	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R37p	L3	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R37n	M3	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R38p	L5	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R38n	L4	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R39p	K2	DQS10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R39n	K1	DQS10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R40p	L6		
6C	VREFB6CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R40n	M6		
6A	VREFB6AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R45p	F1		
6A	VREFB6AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R45n	G1		
6A	VREFB6AN0	IO			DIFFIO_TX_R23p	DIFFOUT_R46p	J4	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R23n	DIFFOUT_R46n	J3	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	E2	DQS12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	E1	DQS12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	L9	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	L8	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	H4	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	H3	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	K9	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	K8	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	D2	DQS13R	DQS14R/CQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	D1	DQS13R	DQS14R/DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	J6	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	H5	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	F4	DQS14R	DQ14R/CQn14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	F3	DQS14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	G4	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	G3	DQ14R	DQ14R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R28p	DIFFOUT_R55p	B1		
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R28n	DIFFOUT_R55n	C1		
6A	VREFB6AN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	H6		
6A	VREFB6AN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	G5		
7A	VREFB7AN0	IO				DIFFOUT_T1n	A2	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C3	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A4	DQS1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B4	DQS1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	A3	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B2	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D7	DQS2T	DQS1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E7	DQS2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	G8	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	G9	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	E8	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	F8	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B8	DQ5T	DQ2T
7A	VREFB7AN0	IO				DIFFOUT_T13p	F9	DQ5T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	DQS5T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	DQS5T	DQ2T/CQn2T
7A	VREFB7AN0	IO				DIFFOUT_T15n	D9	DQ5T	DQ2T
7A	VREFB7AN0	IO				DIFFOUT_T15p	C9	DQ5T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	E10	DQS6T	DQS2T/DQ2T



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	F10	DQS6T	DQS2T/CQ2T
7A	VREFB7AN0	IO				DIFFOUT_T17n	H10	DQ6T	DQ2T
7A	VREFB7AN0	IO				DIFFOUT_T17p	G10	DQ6T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	D10	DQ6T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	E11	DQ6T	DQ2T
7C	VREFB7CN0	IO				DIFFOUT_T21n	B10	DQ7T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T21p	C10	DQ7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	A10	DQSn7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	B11	DQS7T	DQ7T/CQn7T
7C	VREFB7CN0	IO				DIFFOUT_T23n	A11	DQ7T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T23p	A12	DQ7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	C12	DQSn8T	DQS7T/DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	D11	DQS8T	DQS7T/CQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25n	E13	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25p	D13	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C13	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D12	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T27n	G12	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T27p	F12	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	F13	DQSn9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	G13	DQS9T	
7C	VREFB7CN0	IO				DIFFOUT_T29n	H14	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T29p	J14	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	A13		
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	B13		
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A14		
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B14		
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	C14		
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	D14		
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	D15		
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	C15		
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	B16		
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	A15		
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	B17		
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	A16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	J16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	J15		
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	E16		
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	G16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	H16		
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	B19	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A19	DQ10T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T40p	A17	DQ10T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T40n	A18	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C19	DQS10T	DQS11T/CQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C18	DQSn10T	DQS11T/DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42p	F17	DQ11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42n	C17	DQ11T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	E17	DQS11T	DQ11T/CQn11T
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	D17	DQSn11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T44p	D18	DQ11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T44n	F18	DQ11T	DQ11T
8A	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	B20	DQ12T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	A21	DQ12T	DQ16T



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
8A	VREFB8AN0	IO				DIFFOUT_T48p	A20	DQ12T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T48n	D19	DQ12T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	D20	DQS12T	DQS16T/CQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	C20	DQSn12T	DQSn16T/DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T50p	D21	DQ13T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T50n	C21	DQ13T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	B22	DQS13T	DQ16T/CQn16T
8A	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	A22	DQSn13T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T52p	A23	DQ13T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T52n	B23	DQ13T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	D23	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	C23	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60p	D22	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60n	D25	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	D24	DQS16T	DQS17T/CQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C24	DQSn16T	DQSn17T/DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62p	F21	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62n	G21	DQ17T	DQ17T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	F22	DQS17T	DQ17T/CQn17T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	E22	DQSn17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64p	E23	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64n	G22	DQ17T	DQ17T
		GND					M17		
		GND					AF3		
		GND					R14		
		GND					K11		
		GND					B24		
		GND					AG2		
		GND					AG5		
		GND					AG8		
		GND					AG11		
		GND					AG14		
		GND					AG17		
		GND					AG20		
		GND					AG23		
		GND					AG26		
		GND					AF27		
		GND					AD2		
		GND					AD5		
		GND					AD8		
		GND					AD11		
		GND					AD14		
		GND					AD17		
		GND					AD20		
		GND					AD23		
		GND					AC24		
		GND					AC27		
		GND					AA2		
		GND					AA5		
		GND					AA8		
		GND					AA11		
		GND					AA14		
		GND					AA17		
		GND					AA20		
		GND					Y12		





Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
		GND					Y16		
		GND					Y21		
		GND					Y24		
		GND					Y27		
		GND					W12		
		GND					W14		
		GND					W16		
		GND					W18		
		GND					V2		
		GND					V5		
		GND					V8		
		GND					V11		
		GND					V13		
		GND					V15		
		GND					V17		
		GND					V19		
		GND					U10		
		GND					U12		
		GND					U14		
		GND					U16		
		GND					U18		
		GND					U21		
		GND					U24		
		GND					U27		
		GND					T11		
		GND					T13		
		GND					T15		
		GND					T17		
		GND					T19		
		GND					R2		
		GND					R5		
		GND					R8		
		GND					R12		
		GND					R16		
		GND					R18		
		GND					P11		
		GND					P13		
		GND					P17		
		GND					P21		
		GND					P24		
		GND					P27		
		GND					N10		
		GND					N12		
		GND					N14		
		GND					N16		
		GND					N18		
		GND					M2		
		GND					M5		
		GND					M8		
		GND					M11		
		GND					M13		
		GND					M15		
		GND					M19		
		GND					L10		
		GND					L12		



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
		GND					L14		
		GND					L16		
		GND					L18		
		GND					L21		
		GND					L24		
		GND					L27		
		GND					K13		
		GND					K15		
		GND					K17		
		GND					K19		
		GND					J2		
		GND					J5		
		GND					J8		
		GND					J13		
		GND					J17		
		GND					H9		
		GND					H12		
		GND					H15		
		GND					H18		
		GND					H21		
		GND					H24		
		GND					H27		
		GND					F2		
		GND					F5		
		GND					E6		
		GND					E9		
		GND					E12		
		GND					E15		
		GND					E18		
		GND					E21		
		GND					E24		
		GND					E27		
		GND					C2		
		GND					B3		
		GND					B6		
		GND					B9		
		GND					B12		
		GND					B15		
		GND					B18		
		GND					B21		
		GND					B27		
		VCC					R15		
		VCC					L17		
		VCC					V14		
		VCC					V18		
		VCC					U11		
		VCC					U13		
		VCC					U15		
		VCC					U17		
		VCC					T12		
		VCC					T14		
		VCC					T16		
		VCC					R13		
		VCC					R17		
		VCC					P12		



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
		VCC					P14		
		VCC					P16		
		VCC					P18		
		VCC					N13		
		VCC					N15		
		VCC					N17		
		VCC					M12		
		VCC					M14		
		VCC					M16		
		VCC					L11		
		VCC					T18		
		VCC					V12		
		VCC					V16		
		VCC					R11		
		VCC					N11		
		VCC					M18		
		VCC					L13		
		VCC					L15		
		DNU					P15		
		VCCPGM					AA21		
		VCCPGM					Y8		
		TEMPDIODEn					D4		
		TEMPDIODEp					D3		
		VCC_CLKIN3C					AB14		
		VCC_CLKIN4C					AC13		
		VCC_CLKIN7C					F14		
		VCC_CLKIN8C					F16		
		VCCA_PLL_B1					AC14		
		VCCA_PLL_L2					R22		
		VCCA_PLL_R2					R7		
		VCCA_PLL_T1					F15		
		VCCD_PLL_B1					AB15		
		VCCD_PLL_L2					P22		
		VCCD_PLL_R2					P7		
		VCCD_PLL_T1					G15		
		VCCIO1A					E26		
		VCCIO1A					H23		
		VCCIO1A					H26		
		VCCIO1C					P26		
		VCCIO1C					R23		
		VCCIO2A					W26		
		VCCIO2A					AD26		
		VCCIO2A					AA22		
		VCCIO2C					T26		
		VCCIO2C					V22		
		VCCIO3A					AC22		
		VCCIO3A					AF22		
		VCCIO3A					AF25		
		VCCIO3A					AC18		
		VCCIO3C					AF18		
		VCCIO3C					AC15		
		VCCIO4A					AC6		
		VCCIO4A					AF4		
		VCCIO4A					AF7		
		VCCIO4A					AD10		



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
		VCCIO4C					AB12		
		VCCIO4C					AF13		
		VCCIO5A					AA7		
		VCCIO5A					AD3		
		VCCIO5A					AA3		
		VCCIO5C					P6		
		VCCIO5C					R3		
		VCCIO6A					E3		
		VCCIO6A					K3		
		VCCIO6A					H7		
		VCCIO6C					L7		
		VCCIO6C					N3		
		VCCIO7A					C7		
		VCCIO7A					F7		
		VCCIO7A					F11		
		VCCIO7A					C4		
		VCCIO7C					C11		
		VCCIO7C					G14		
		VCCIO8A					C25		
		VCCIO8A					F23		
		VCCIO8A					E19		
		VCCIO8A					C22		
		VCCIO8C					C16		
		VCCIO8C					G17		
		VCCPD1A					L19		
		VCCPD1C					N19		
		VCCPD2A					U19		
		VCCPD2C					R19		
		VCCPD3A					W17		
		VCCPD3C					W15		
		VCCPD4A					W11		
		VCCPD4C					W13		
		VCCPD5A					V10		
		VCCPD5C					T10		
		VCCPD6A					M10		
		VCCPD6C					P10		
		VCCPD7A					K12		
		VCCPD7C					K14		
		VCCPD8A					K18		
		VCCPD8C					K16		
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				K22		
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				N22		
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				Y22		
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				U22		
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB18		
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AA16		
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB10		
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AA12		
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				W7		
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				T7		
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				J7		
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				M7		
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G11		
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				H13		
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G19		



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				H17		
		NC					E25		
		NC					AB22		
		NC					W10		
		NC					E4		
		NC					V9		
		NC (4)					F6		
		NC (5)					R24		
		NC (5)					AD15		
		NC (5)					P5		
		NC (5)					E14		
		NC					AE25		
		NC (5)					U20		
		NC (5)					M9		
		NC					L20		
		NC					K10		
		NC					J21		
		NC (6)					K24		
		NC (6)					K23		
		NC (6)					H28		
		NC (6)					J27		
		NC (6)					L23		
		NC (6)					L22		
		NC (6)					J28		
		NC (6)					K27		
		NC (6)					AA27		
		NC (6)					Y28		
		NC (6)					W22		
		NC (6)					W23		
		NC (6)					AB27		
		NC (6)					AA28		
		NC (6)					W24		
		NC (6)					W25		
		NC (6)					AD24		
		NC (6)					AE23		
		NC (6)					AF24		
		NC (6)					AE24		
		NC (6)					AF23		
		NC (6)					AG24		
		NC (6)					AH24		
		NC (6)					AH23		
		NC (6)					AH20		
		NC (6)					AH21		
		NC (6)					AH22		
		NC (6)					AG22		
		NC (6)					Y19		
		NC (6)					AA18		
		NC (6)					Y18		
		NC (6)					Y17		
		NC (6)					AB11		
		NC (6)					AC10		
		NC (6)					Y10		
		NC (6)					Y11		
		NC (6)					AG4		
		NC (6)					AH3		



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
		NC (6)					AH4		
		NC (6)					AH5		
		NC (6)					AG3		
		NC (6)					AH2		
		NC (6)					AD9		
		NC (6)					AC9		
		NC (6)					AA9		
		NC (6)					AB9		
		NC (6)					Y9		
		NC (6)					AA10		
		NC (6)					W5		
		NC (6)					W6		
		NC (6)					Y1		
		NC (6)					W2		
		NC (6)					V6		
		NC (6)					V7		
		NC (6)					W3		
		NC (6)					W4		
		NC (6)					H2		
		NC (6)					J1		
		NC (6)					K7		
		NC (6)					K6		
		NC (6)					G2		
		NC (6)					H1		
		NC (6)					K5		
		NC (6)					K4		
		NC (6)					D6		
		NC (6)					E5		
		NC (6)					C5		
		NC (6)					D5		
		NC (6)					B5		
		NC (6)					C6		
		NC (6)					A5		
		NC (6)					A6		
		NC (6)					A8		
		NC (6)					A9		
		NC (6)					A7		
		NC (6)					B7		
		NC (6)					H11		
		NC (6)					J10		
		NC (6)					J11		
		NC (6)					J12		
		NC (6)					G18		
		NC (6)					F19		
		NC (6)					J18		
		NC (6)					J19		
		NC (6)					B25		
		NC (6)					A26		
		NC (6)					A24		
		NC (6)					A25		
		NC (6)					B26		
		NC (6)					A27		
		NC (6)					F20		
		NC (6)					E20		
		NC (6)					H20		



Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only (1)	Dedicated Tx_Rx Channel (2)	Emulated LVDS Output Channel (2)	F780	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode (2)
		NC (6)					G20		
		NC (6)					H19		
		NC (6)					J20		
		NC (3)		MSEL2			G7		
		NC (3)		MSEL1			J9		
		NC (3)		MSEL0			H8		
		VCCAUX					G23		
		VCCAUX					AC23		
		VCCAUX					AB6		
		VCCAUX					G6		

**Notes:**

- (1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix® IV device pin table for details.
- (2) The individual index number of the pin in this column may not be the same as its companion Stratix IV device, but the functionality of the pin is fully migratable.
- (3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.
- (4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.
- (5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.
- (6) This NC pin is an IO pin in the Stratix IV device and can be left unconnected.



Pin Name	Pin Type (1st and 2nd Function)	Pin Description
<b>Clock and PLL Pins</b>		
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	
PLL_[L1, L2, L3, L4]_FB_CLKOUT0p	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
<b>Dedicated Configuration/JTAG Pins</b>		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nstatus	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
<b>Optional/Dual-Purpose Configuration Pins</b>		
nCSO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin for HardCopy IV.
<b>Differential I/O Pins</b>		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

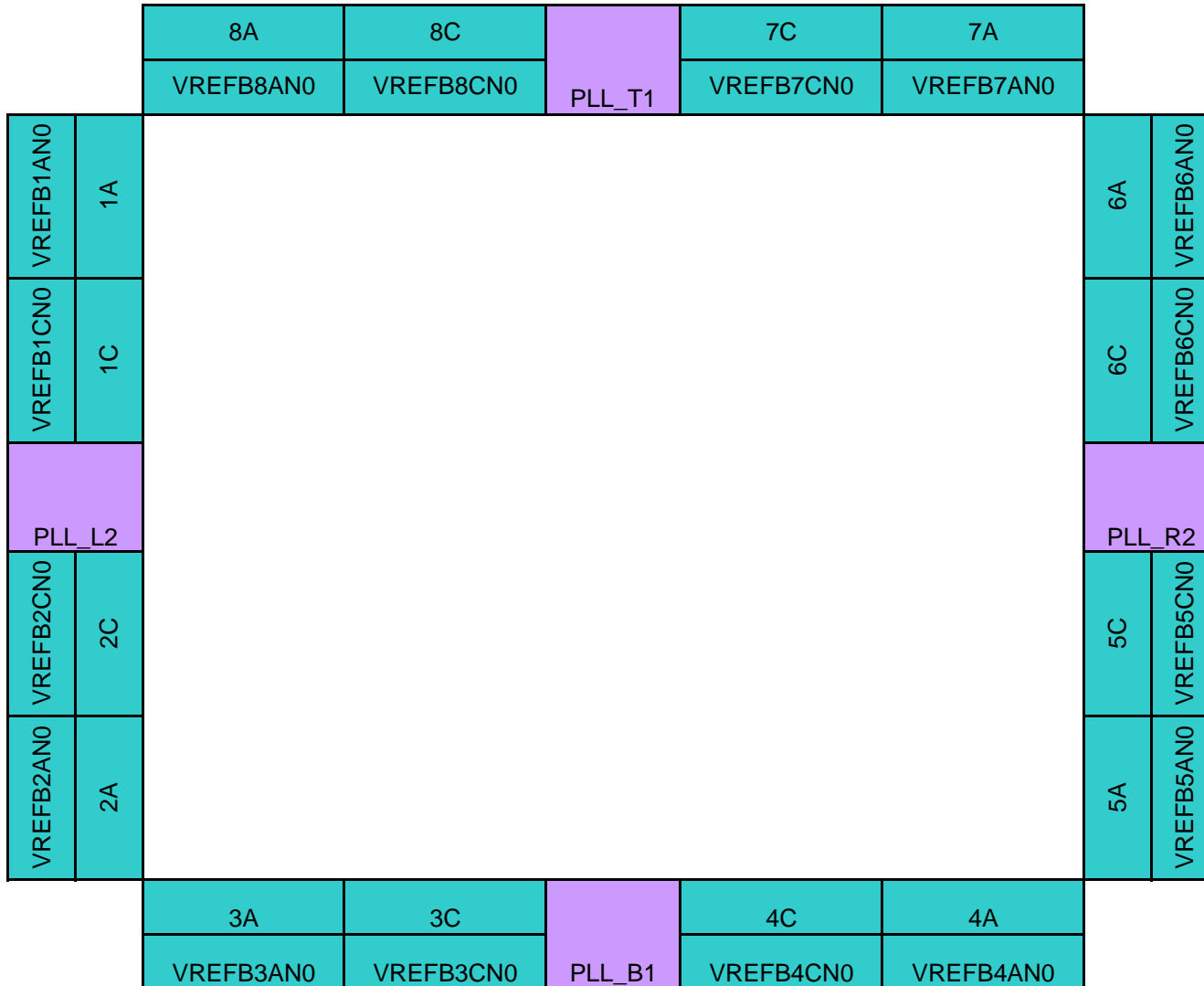




Pin Name	Pin Type (1st and 2nd Function)	Pin Description
<b>External Memory Interface Pins</b>		
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
<b>Reference Pins</b>		
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
<b>Supply Pins</b>		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18),SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
VREFB[1:8][A,B,C]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.

**Notes:**

- (1) These pin definitions are prepared based on the device with the largest density, HC4E35. Refer to the pin list for the availability of pins in each density.
- (2) Refer to HardCopy IV handbook for the power supply recommended operating conditions.



**Notes:**

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.



Version Number	Date	Changes Made
1.0	10/28/2009	Initial release.