Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		TDI		TDI			E17	F24		
		TMS		TMS			D17	H22		
		TRST		TRST			F18	D26		
		TCK		TCK			D18	C26		
		TDO		TDO			A18	G24		
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	B19	F26		
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	C19	F25		
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	A20	C28		
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	A19	D27		
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G17	G26	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G16	G25	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B20	B28	DQSn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C20	C27	DQS1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	D19	H25	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	E19	J24	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	A22	D28	DQSn2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	A21	E28	DQS2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	D20	J23	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	E20	J22	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	B22	F28	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	C22	F27	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	F16	K21	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	F15	K20	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	C21	G28	DQSn3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D21	G27	DQS3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	H16	K26	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	G15	K25	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	D22	J26		
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	E22	J25		
1A	VREFB1AN0	IO						K24		
1A	VREFB1AN0	IO						K23		
1A	VREFB1AN0	IO						H28		
1A	VREFB1AN0	IO						J27		
1A	VREFB1AN0	IO						L23		
1A	VREFB1AN0	IO						L22		
1A	VREFB1AN0	IO						J28		
1A	VREFB1AN0	IO						K27		
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	G19	M23		
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	H19	M22		
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	F20	L26	DQSn5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	G20	L25	DQS5L	
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	H20	M21	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	J19	M20	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	F22	K28	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	F21	L28	DQ5L	
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	J18	N21	DQ6L	DQ5L
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	J17	N20	DQ6L	DQ5L
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	K20	M26	DQSn6L	DQ5L
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	K19	M25	DQS6L	DQ5L/CQn5L
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	H17	N25	DQ6L	DQ5L
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	J16	M24	DQ6L	DQ5L

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	J21	M28	DQSn7L	DQSn5L/DQ5L
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	J20	M27	DQS7L	DQS5L/CQ5L
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	K16	N23	DQ7L	DQ5L
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	L16	P23	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	G22	P25	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	G21	N24	DQ7L	DQ5L
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	L20	P20		
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	L19	P19		
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	J22	N27		
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	K21	N26		
1C	VREFB1CN0	CLK1n	CLK1n				K22	N28		
1C	VREFB1CN0	CLK1p	CLK1p				L22	P28		
2C	VREFB2CN0	CLK3p	CLK3p				M19	R27		
2C	VREFB2CN0	CLK3n	CLK3n				M20	R28		
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	M21	U28		
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	M22	T28		
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	M15	R20		
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	M16	R21		
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	N21	R26	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	N22	T27	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	P16	T25	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	P17	R25	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	N19	V27	DQS8L	DQS10L/CQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	N20	V28	DQSn8L	DQSn10L/DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	N16	T20	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	N17	T21	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	R21	V26	DQS9L	DQ10L/CQn10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	R22	U26	DQSn9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	P19	T24	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	P20	U25	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	U22	W27	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	T22	W28	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	R19	T22	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	R20	T23	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	T20	V24	DQS10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	T21	V25	DQSn10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	R18	V23		
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	T19	U23		
2A	VREFB2AN0	IO						AA27		
2A	VREFB2AN0	IO						Y28		
2A	VREFB2AN0	IO						W22		
2A	VREFB2AN0	IO						W23		
2A	VREFB2AN0	IO						AB27		
2A	VREFB2AN0	IO						AA28		
2A	VREFB2AN0	IO						W24		
2A	VREFB2AN0	IO						W25		
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	V21	Y25		
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	V22	Y26		
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	U15	V20	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	T15	V21	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	Y22	AC28	DQS12L	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	W22	AB28	DQSn12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	U16	AA25	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	T17	AA26	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	W20	AB25	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	W21	AB26	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	U19	AC25	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	U20	AC26	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AA21	AD27	DQS13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AA22	AD28	DQSn13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	V19	W20	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	V20	W21	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AB20	AG28	DQS14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AB21	AF28	DQSn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	V16	Y23	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	W17	AA24	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AB18	AE27		
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AB19	AE28		
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AA19	AA23		
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	Y19	AB24		
		nCONFIG		nCONFIG			AB17	W19		
		nSTATUS		nSTATUS			W18	AD25		
		CONF_DONE		CONF_DONE			V18	AE26		
		PORSEL		PORSEL			Y18	AB23		
		nCE		nCE			Y17	Y20		
3A	VREFB3AN0	IO						AF26		
3A	VREFB3AN0	IO						AH27		
3A	VREFB3AN0	IO						AH25		
3A	VREFB3AN0	IO						AG25		
3A	VREFB3AN0	IO						AG27		
3A	VREFB3AN0	IO						AH26		
3A	VREFB3AN0	IO						AE22		
3A	VREFB3AN0	IO						AD22		
3A	VREFB3AN0	IO						AB20		
3A	VREFB3AN0	IO						AB21		
3A	VREFB3AN0	IO						AD21		
3A	VREFB3AN0	IO						AC21		
3A	VREFB3AN0	IO						AD24		
3A	VREFB3AN0	IO						AE23		
3A	VREFB3AN0	IO						AF24		
3A	VREFB3AN0	IO						AE24		
3A	VREFB3AN0	IO						AF23		
3A	VREFB3AN0	IO						AG24		
3A	VREFB3AN0	IO						AH24		
3A	VREFB3AN0	IO						AH23		
3A	VREFB3AN0	IO						AH20		
3A	VREFB3AN0	IO						AH21		
3A	VREFB3AN0	IO						AH22		
3A	VREFB3AN0	IO						AG22		
3A	VREFB3AN0	IO						AC20		
3A	VREFB3AN0	IO						AG21		
3A	VREFB3AN0	IO						AF21		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
3A	VREFB3AN0	IO						AE21		
3A	VREFB3AN0	IO						AF20		
3A	VREFB3AN0	IO						AE20		
3A	VREFB3AN0	IO						AD19		
3A	VREFB3AN0	IO						AC19		
3A	VREFB3AN0	IO						AB19		
3A	VREFB3AN0	IO						AA19		
3A	VREFB3AN0	IO						AE19		
3A	VREFB3AN0	IO						AD18		
3A	VREFB3AN0	IO						Y19		
3A	VREFB3AN0	IO						AA18		
3A	VREFB3AN0	IO						Y18		
3A	VREFB3AN0	IO						Y17		
3C	VREFB3CN0	IO				DIFFOUT_B21n	W16	AF19	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B21p	V15	AG19	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	Y14	AH19	DQSn7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	W14	AG18	DQS7B	DQ7B/CQn7B
3C	VREFB3CN0	IO				DIFFOUT_B23n	Y15	AH17	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B23p	W15	AH18	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AB16	AF17	DQSn8B	DQSn7B/DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AA16	AE18	DQS8B	DQS7B/CQ7B
3C	VREFB3CN0	IO				DIFFOUT_B25n	Y16	AE16	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B25p	AB14	AD16	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AB15	AF16	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AA15	AE17	DQ8B	DQ7B
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	T13	AC17		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	R13	AB17		
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	W13	AC16		
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	V13	AB16		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	Y12	AA15		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	W12	Y15		
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	U14	AH16		
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	U13	AG16		
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AB12	AH15		
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AA12	AG15		
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AB13	AF15		
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AA13	AE15		
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	Y10	AE14		
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AA10	AF14		
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AB10	AG13		
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AB11	AH14		
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	W11	AG12		
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	Y11	AH13		
4C	VREFB4CN0	IO				DIFFOUT_B36p	T10	Y13	DQ9B	
4C	VREFB4CN0	IO				DIFFOUT_B36n	R10	Y14	DQ9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	U9	AD13	DQS9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	V9	AE13	DQSn9B	
4C	VREFB4CN0	IO				DIFFOUT_B38p	R9	AA13	DQ9B	
4C	VREFB4CN0	IO				DIFFOUT_B38n	T9	AB13	DQ9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AA9	AG10	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AB9	AH10	DQ10B	DQ11B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
4C	VREFB4CN0	IO				DIFFOUT_B40p	W8	AH11	DQ10B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B40n	AB8	AH12	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	W9	AF10	DQS10B	DQS11B/CQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	Y9	AF11	DQSn10B	DQSn11B/DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42p	Y7	AF12	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42n	W7	AC12	DQ11B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AA7	AD12	DQS11B	DQ11B/CQn11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AB7	AE12	DQSn11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B44p	AB6	AC11	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B44n	AA6	AE11	DQ11B	DQ11B
4A	VREFB4AN0	IO						AB11		
4A	VREFB4AN0	IO						AC10		
4A	VREFB4AN0	IO						Y10		
4A	VREFB4AN0	IO						Y11		
4A	VREFB4AN0	IO						AG9		
4A	VREFB4AN0	IO						AH8		
4A	VREFB4AN0	IO						AE10		
4A	VREFB4AN0	IO						AH9		
4A	VREFB4AN0	IO						AE9		
4A	VREFB4AN0	IO						AF9		
4A	VREFB4AN0	IO						AF8		
4A	VREFB4AN0	IO						AE8		
4A	VREFB4AN0	IO						AG7		
4A	VREFB4AN0	IO						AH7		
4A	VREFB4AN0	IO						AG6		
4A	VREFB4AN0	IO						AH6		
4A	VREFB4AN0	IO						AG4		
4A	VREFB4AN0	IO						AH3		
4A	VREFB4AN0	IO						AH4		
4A	VREFB4AN0	IO						AH5		
4A	VREFB4AN0	IO						AG3		
4A	VREFB4AN0	IO						AH2		
4A	VREFB4AN0	IO						AD9		
4A	VREFB4AN0	IO						AC9		
4A	VREFB4AN0	IO						AA9		
4A	VREFB4AN0	IO						AB9		
4A	VREFB4AN0	IO						Y9		
4A	VREFB4AN0	IO						AA10		
4A	VREFB4AN0	IO						AE6		
4A	VREFB4AN0	IO						AF6		
4A	VREFB4AN0	IO						AE4		
4A	VREFB4AN0	IO						AE7		
4A	VREFB4AN0	IO						AE5		
4A	VREFB4AN0	IO						AF5		
4A	VREFB4AN0	IO						AB8		
4A	VREFB4AN0	IO						AC8		
4A	VREFB4AN0	IO						AC7		
4A	VREFB4AN0	IO						AD7		
4A	VREFB4AN0	IO						AB7		
4A	VREFB4AN0	IO						AD6		
		nIO_PULLUP		nIO_PULLUP			AB4	AE3		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		nCEO		nCEO			U5	AB5		
		DCLK		DCLK			Y4	AC5		
		nCSO		nCSO			Y6	AD4		
		ASDO		ASDO			Y3	AA6		
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	W4	AC3		
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	W5	AC4		
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AA3	AF1		
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AA4	AE2		
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	V6	AB3	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	V7	AB4	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AB2	AG1	DQSn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AB3	AF2	DQS1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	U4	Y6	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	T4	Y7	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AB1	AE1	DQSn2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AA1	AD1	DQS2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	V3	AA4	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	V4	Y5	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	W2	AC1	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	W3	AC2	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	U7	Y3	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	U8	Y4	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	Y1	AB1	DQSn3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	Y2	AB2	DQS3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	T7	W8	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	T8	W9	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	W1	AA1		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	V1	Y2		
5A	VREFB5AN0	IO						W5		
5A	VREFB5AN0	IO						W6		
5A	VREFB5AN0	IO						Y1		
5A	VREFB5AN0	IO						W2		
5A	VREFB5AN0	IO						V6		
5A	VREFB5AN0	IO						V7		
5A	VREFB5AN0	IO						W3		
5A	VREFB5AN0	IO						W4		
5C	VREFB5CN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	R6	U6		
5C	VREFB5CN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	P7	U7		
5C	VREFB5CN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	R3	V3	DQSn5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	R4	V4	DQS5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	P3	U8	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	P4	U9	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	U3	W1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	T3	V1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	P6	T4	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	N6	U5	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	U1	U3	DQSn6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	U2	U4	DQS6R	DQ5R/CQn5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	N4	T8	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	N5	T9	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	T1	T2	DQSn7R	DQSn5R/DQ5R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
5C	VREFB5CN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	T2	T3	DQS7R	DQS5R/CQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	M6	T6	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	M7	R6	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	P1	R4	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	P2	T5	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	M3	R9		
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	M4	R10		
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R14n	DIFFOUT_R28n	N2	U1		
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R14p	DIFFOUT_R28p	N3	U2		
5C	VREFB5CN0	CLK8n	CLK8n				N1	T1		
5C	VREFB5CN0	CLK8p	CLK8p				M1	R1		
6C	VREFB6CN0	CLK10p	CLK10p				L2	P2		
6C	VREFB6CN0	CLK10n	CLK10n				L1	P1		
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R15p	DIFFOUT_R29p	K2	M1		
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R15n	DIFFOUT_R29n	K1	N1		
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R15p	DIFFOUT_R30p	L4	P9		
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R15n	DIFFOUT_R30n	L3	P8		
6C	VREFB6CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R31p	H1	N4	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R31n	J1	P4	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R32p	K8	N7	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R32n	K7	N6	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R33p	K4	P3	DQS8R	DQS10R/CQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R33n	K3	N2	DQSn8R	DQSn10R/DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R34p	H7	N5	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R34n	J7	M4	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R35p	F1	L2	DQS9R	DQ10R/CQn10R
6C	VREFB6CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R35n	G1	L1	DQSn9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R36p	J4	N9	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R36n	J3	N8	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R37p	H3	L3	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R37n	H2	M3	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R38p	H5	L5	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R38n	H4	L4	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R39p	G4	K2	DQS10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R39n	G3	K1	DQSn10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R40p	H6	L6		
6C	VREFB6CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R40n	J6	M6		
6A	VREFB6AN0	IO						H2		
6A	VREFB6AN0	IO						J1		
6A	VREFB6AN0	IO						K7		
6A	VREFB6AN0	IO						K6		
6A	VREFB6AN0	IO						G2		
6A	VREFB6AN0	IO						H1		
6A	VREFB6AN0	IO						K5		
6A	VREFB6AN0	IO						K4		
6A	VREFB6AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R45p	E2	F1		
6A	VREFB6AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R45n	E1	G1		
6A	VREFB6AN0	IO			DIFFIO_TX_R23p	DIFFOUT_R46p	F8	J4	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R23n	DIFFOUT_R46n	G8	J3	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	D2	E2	DQS12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	D1	E1	DQSn12R	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
6A	VREFB6AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	F7	L9	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	G6	L8	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	B1	H4	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	C1	H3	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	F4	K9	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	F3	K8	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	A2	D2	DQS13R	DQS14R/CQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	B2	D1	DQSn13R	DQSn14R/DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	E5	J6	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	E4	H5	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	D3	F4	DQS14R	DQ14R/CQn14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	E3	F3	DQSn14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	B4	G4	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	C4	G3	DQ14R	DQ14R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R28p	DIFFOUT_R55p	A4	B1		
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R28n	DIFFOUT_R55n	A3	C1		
6A	VREFB6AN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	B5	H6		
6A	VREFB6AN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	C5	G5		
7A	VREFB7AN0	IO						A2		
7A	VREFB7AN0	IO						C3		
7A	VREFB7AN0	IO						A4		
7A	VREFB7AN0	IO						B4		
7A	VREFB7AN0	IO						A3		
7A	VREFB7AN0	IO						B2		
7A	VREFB7AN0	IO						D7		
7A	VREFB7AN0	IO						E7		
7A	VREFB7AN0	IO						G8		
7A	VREFB7AN0	IO						G9		
7A	VREFB7AN0	IO						E8		
7A	VREFB7AN0	IO						F8		
7A	VREFB7AN0	IO						D6		
7A	VREFB7AN0	IO						E5		
7A	VREFB7AN0	IO						C5		
7A	VREFB7AN0	IO						D5		
7A	VREFB7AN0	IO						B5		
7A	VREFB7AN0	IO						C6		
7A	VREFB7AN0	IO						A5		
7A	VREFB7AN0	IO						A6		
7A	VREFB7AN0	IO						A8		
7A	VREFB7AN0	IO						A9		
7A	VREFB7AN0	IO						A7		
7A	VREFB7AN0	IO						B7		
7A	VREFB7AN0	IO						B8		
7A	VREFB7AN0	IO						F9		
7A	VREFB7AN0	IO						C8		
7A	VREFB7AN0	IO						D8		
7A	VREFB7AN0	IO						D9		
7A	VREFB7AN0	IO						C9		
7A	VREFB7AN0	IO						E10		
7A	VREFB7AN0	IO						F10		
7A	VREFB7AN0	IO						H10		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
7A	VREFB7AN0	IO						G10		
7A	VREFB7AN0	IO						D10		
7A	VREFB7AN0	IO						E11		
7A	VREFB7AN0	IO						H11		
7A	VREFB7AN0	IO						J10		
7A	VREFB7AN0	IO						J11		
7A	VREFB7AN0	IO						J12		
7C	VREFB7CN0	IO				DIFFOUT_T21n	D7	B10	DQ7T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T21p	D9	C10	DQ7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	C10	A10	DQSn7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	D10	B11	DQS7T	DQ7T/CQn7T
7C	VREFB7CN0	IO				DIFFOUT_T23n	D8	A11	DQ7T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T23p	C9	A12	DQ7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	A7	C12	DQSn8T	DQSn7T/DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	B7	D11	DQS8T	DQS7T/CQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25n	A9	E13	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25p	C7	D13	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	A8	C13	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	B8	D12	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T27n	F10	G12	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T27p	G10	F12	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	F9	F13	DQSn9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	G9	G13	DQS9T	
7C	VREFB7CN0	IO				DIFFOUT_T29n	H10	H14	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T29p	G11	J14	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C11	A13		
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D11	B13		
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A11	A14		
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B11	B14		
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	A10	C14		
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	B10	D14		
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	A13	D15		
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	A12	C15		
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	D12	B16		
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	C12	A15		
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	C13	B17		
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	B13	A16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	H14	J16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	G14	J15		
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	D14	E16		
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D13	D16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	E14	G16		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	F14	H16		
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	A15	B19	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A14	A19	DQ10T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T40p	B14	A17	DQ10T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T40n	D15	A18	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C15	C19	DQS10T	DQS11T/CQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C14	C18	DQSn10T	DQSn11T/DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42p	C17	F17	DQ11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42n	B17	C17	DQ11T	DQ11T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	A17	E17	DQS11T	DQ11T/CQn11T
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	A16	D17	DQSn11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T44p	D16	D18	DQ11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T44n	C16	F18	DQ11T	DQ11T
8A	VREFB8AN0	IO						G18		
8A	VREFB8AN0	IO						F19		
8A	VREFB8AN0	IO						J18		
8A	VREFB8AN0	IO						J19		
8A	VREFB8AN0	IO						B20		
8A	VREFB8AN0	IO						A21		
8A	VREFB8AN0	IO						A20		
8A	VREFB8AN0	IO						D19		
8A	VREFB8AN0	IO						D20		
8A	VREFB8AN0	IO						C20		
8A	VREFB8AN0	IO						D21		
8A	VREFB8AN0	IO						C21		
8A	VREFB8AN0	IO						B22		
8A	VREFB8AN0	IO						A22		
8A	VREFB8AN0	IO						A23		
8A	VREFB8AN0	IO						B23		
8A	VREFB8AN0	IO						B25		
8A	VREFB8AN0	IO						A26		
8A	VREFB8AN0	IO						A24		
8A	VREFB8AN0	IO						A25		
8A	VREFB8AN0	IO						B26		
8A	VREFB8AN0	IO						A27		
8A	VREFB8AN0	IO						F20		
8A	VREFB8AN0	IO						E20		
8A	VREFB8AN0	IO						H20		
8A	VREFB8AN0	IO						G20		
8A	VREFB8AN0	IO						H19		
8A	VREFB8AN0	IO						J20		
8A	VREFB8AN0	IO						D23		
8A	VREFB8AN0	IO						C23		
8A	VREFB8AN0	IO						D22		
8A	VREFB8AN0	IO						D25		
8A	VREFB8AN0	IO						D24		
8A	VREFB8AN0	IO						C24		
8A	VREFB8AN0	IO						F21		
8A	VREFB8AN0	IO						G21		
8A	VREFB8AN0	IO						F22		
8A	VREFB8AN0	IO						E22		
8A	VREFB8AN0	IO						E23		
8A	VREFB8AN0	IO						G22		
		GND					L14	M17		
		GND					AB5	AF3		
		GND					M11	R14		
		GND					E18	K11		
		GND					AB22	B24		
		GND					AA20	AG2		
		GND					AA17	AG5		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		GND					AA14	AG8		
		GND					AA11	AG11		
		GND					AA8	AG14		
		GND					AA5	AG17		
		GND					AA2	AG20		
		GND					Y21	AG23		
		GND					V17	AG26		
		GND					V14	AF27		
		GND					V11	AD2		
		GND					V8	AD5		
		GND					V5	AD8		
		GND					V2	AD11		
		GND					U21	AD14		
		GND					U18	AD17		
		GND					R14	AD20		
		GND					R11	AD23		
		GND					R8	AC24		
		GND					R5	AC27		
		GND					R2	AA2		
		GND					P21	AA5		
		GND					P18	AA8		
		GND					P15	AA11		
		GND					P13	AA14		
		GND					P11	AA17		
		GND					P9	AA20		
		GND					N14	Y12		
		GND					N12	Y16		
		GND					N10	Y21		
		GND					M13	Y24		
		GND					M9	Y27		
		GND					M8	W12		
		GND					M5	W14		
		GND					M2	W16		
		GND					L21	W18		
		GND					L18	V2		
		GND					L15	V5		
		GND					L10	V8		
		GND					K13	V11		
		GND					K11	V13		
		GND					K9	V15		
		GND					J14	V17		
		GND					J12	V19		
		GND					J10	U10		
		GND					J8	U12		
		GND					J5	U14		
		GND					J2	U16		
		GND					H21	U18		
		GND					H18	U21		
		GND					H15	U24		
		GND					H12	U27		
		GND					H9	T11		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		GND					F5	T13		
		GND					F2	T15		
		GND					E21	T17		
		GND					E15	T19		
		GND					E12	R2		
		GND					E9	R5		
		GND					E6	R8		
		GND					C2	R12		
		GND					B21	R16		
		GND					B18	R18		
		GND					B15	P11		
		GND					B12	P13		
		GND					B9	P17		
		GND					B6	P21		
		GND					B3	P24		
		GND					A1	P27		
		GND						N10		
		GND						N12		
		GND						N14		
		GND						N16		
		GND						N18		
		GND						M2		
		GND						M5		
		GND						M8		
		GND						M11		
		GND						M13		
		GND						M15		
		GND						M19		
		GND						L10		
		GND						L12		
		GND						L14		
		GND						L16		
		GND						L18		
		GND						L21		
		GND						L24		
		GND						L27		
		GND						K13		
		GND						K15		
		GND						K17		
		GND						K19		
		GND						J2		
		GND						J5		
		GND						J8		
		GND						J13		
		GND						J17		
		GND						H9		
		GND						H12		
		GND						H15		
		GND						H18		
		GND						H21		
		GND						H24		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		GND						H27		
		GND						F2		
		GND						F5		
		GND						E6		
		GND						E9		
		GND						E12		
		GND						E15		
		GND						E18		
		GND						E21		
		GND						E24		
		GND						E27		
		GND						C2		
		GND						B3		
		GND						B6		
		GND						B9		
		GND						B12		
		GND						B15		
		GND						B18		
		GND						B21		
		GND						B27		
		VCC					L11	R15		
		VCC					K14	L17		
		VCC					P12	V14		
		VCC					N13	V18		
		VCC					N11	U11		
		VCC					N9	U13		
		VCC					M12	U15		
		VCC					M10	U17		
		VCC					L13	T12		
		VCC					K12	T14		
		VCC					K10	T16		
		VCC					J13	R13		
		VCC					J11	R17		
		VCC						P12		
		VCC						P14		
		VCC						P16		
		VCC						P18		
		VCC						N13		
		VCC						N15		
		VCC						N17		
		VCC						M12		
		VCC						M14		
		VCC						M16		
		VCC						L11		
		VCC					J9	T18		
		VCC					P14	V12		
		VCC					M14	V16		
		VCC					L9	R11		
		VCC						N11		
		VCC						M18		
		VCC						L13		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		VCC						L15		
		DNU					L12	P15		
		VCCPGM					T16	AA21		
		VCCPGM					T6	Y8		
		TEMPDIODEn					A6	D4		
		TEMPDIODEp					A5	D3		
		VCC_CLKIN3C					T12	AB14		
		VCC_CLKIN4C					U10	AC13		
		VCC_CLKIN7C					E11	F14		
		VCC_CLKIN8C					F13	F16		
		VCCA_PLL_B1					U11	AC14		
		VCCA_PLL_L2					M18	R22		
		VCCA_PLL_R2					L5	R7		
		VCCA_PLL_T1					F12	F15		
		VCCD_PLL_B1					U12	AB15		
		VCCD_PLL_L2					M17	P22		
		VCCD_PLL_R2					L6	P7		
		VCCD_PLL_T1					G12	G15		
		VCCIO1A					C18	E26		
		VCCIO1A					F19	H23		
		VCCIO1A						H26		
		VCCIO1C					H22	P26		
		VCCIO1C					K17	R23		
		VCCIO2A					R16	W26		
		VCCIO2A					Y20	AD26		
		VCCIO2A						AA22		
		VCCIO2C					P22	T26		
		VCCIO2C					R17	V22		
		VCCIO3A						AC22		
		VCCIO3A						AF22		
		VCCIO3A						AF25		
		VCCIO3A						AC18		
		VCCIO3C					T14	AF18		
		VCCIO3C					Y13	AC15		
		VCCIO4A						AC6		
		VCCIO4A						AF4		
		VCCIO4A						AF7		
		VCCIO4A						AD10		
		VCCIO4C					W10	AB12		
		VCCIO4C					Y8	AF13		
		VCCIO5A					R7	AA7		
		VCCIO5A					Y5	AD3		
		VCCIO5A						AA3		
		VCCIO5C					N7	P6		
		VCCIO5C					R1	R3		
		VCCIO6A					D5	E3		
		VCCIO6A					C3	K3		
		VCCIO6A						H7		
		VCCIO6C					G2	L7		
		VCCIO6C					K6	N3		
		VCCIO7A						C7		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		VCCIO7A						F7		
		VCCIO7A						F11		
		VCCIO7A						C4		
		VCCIO7C					E8	C11		
		VCCIO7C					C8	G14		
		VCCIO8A						C25		
		VCCIO8A						F23		
		VCCIO8A						E19		
		VCCIO8A						C22		
		VCCIO8C					B16	C16		
		VCCIO8C					G13	G17		
		VCCPD1A					J15	L19		
		VCCPD1C					K15	N19		
		VCCPD2A					R15	U19		
		VCCPD2C					N15	R19		
		VCCPD3A						W17		
		VCCPD3C					R12	W15		
		VCCPD4A						W11		
		VCCPD4C					P10	W13		
		VCCPD5A					P8	V10		
		VCCPD5C					N8	T10		
		VCCPD6A					H8	M10		
		VCCPD6C					L8	P10		
		VCCPD7A						K12		
		VCCPD7C					H11	K14		
		VCCPD8A						K18		
		VCCPD8C					H13	K16		
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				G18	K22		
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				K18	N22		
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				T18	Y22		
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				N18	U22		
3A	VREFB3AN0	VREFB3AN0						AB18		
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				V12	AA16		
4A	VREFB4AN0	VREFB4AN0						AB10		
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				V10	AA12		
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				T5	W7		
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				P5	T7		
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				G5	J7		
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				K5	M7		
7A	VREFB7AN0	VREFB7AN0						G11		
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				E10	H13		
8A	VREFB8AN0	VREFB8AN0						G19		
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				E13	H17		
		NC					E16	E25		
		NC					AA18	AB22		
		NC					W6	W10		
		NC					D6	E4		
		NC					W19	V9		
		NC *(4)*					D4	F6		
		NC *(5)*					L17	R24		
		NC *(5)*					T11	AD15		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F484	F780 for Stratix IV only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		NC *(5)*					L7	P5		
		NC *(5)*					F11	E14		
		NC						AE25		
		VCCPT						U20		
		VCCPT						M9		
		NC						L20		
		NC						K10		
		NC						J21		
		NC *(3)*		MSEL2			G7	G7		
		NC *(3)*		MSEL1			C6	J9		
		NC *(3)*		MSEL0			E7	H8		
		VCCAUX					F17	G23		
		VCCAUX					U17	AC23		
		VCCAUX					U6	AB6		
		VCCAUX					F6	G6		

Notes:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix® IV device pin table for details.
(2) The individual index number of the pin in this column may not be the same as its companion Stratix IV device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.

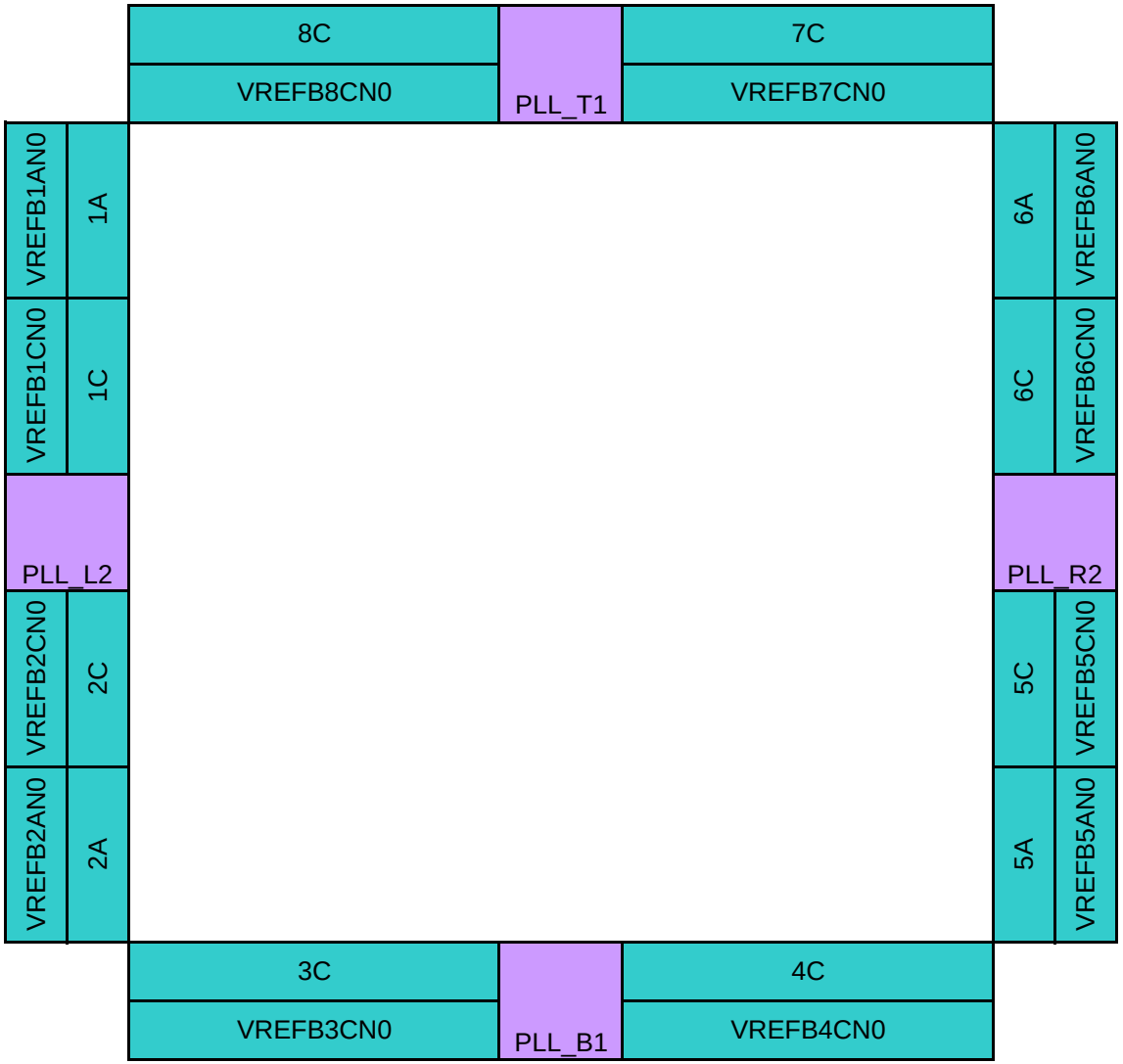
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, ,L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
Nstatus	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
	Optional/Dual-Purpose Configuration Pins	
nCSO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin for HardCopy IV.
	Differential I/O Pins	
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	External Memory Interface Pins	
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
	Reference Pins	
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
	Supply Pins	
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18),SSTL(15, 18, 2),3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
VREFB[1:8][A,B,C]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC4E35. Refer to the pin list for the availability of pins in each density.

(2) Refer to HardCopy IV handbook for the power supply recommended operating conditions.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	10/28/2009	Initial release.