Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		TDI		TDI			F24	G28		
		TMS		TMS			H22	H28		
		TRST		TRST			D26	J28		
		TCK		TCK			C26	F30		
		TDO		TDO			G24	G29		
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	F26	G31		
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	F25	G30		
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C28	E32		
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27	E31		
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G26	J30	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G25	J29	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	F32	DQSn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C27	F31	DQS1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	H25	K28	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	J24	K27	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	D28	C34	DQSn2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E28	C33	DQS2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	J23	N25	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J22	M24	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	F28	H32	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	F27	H31	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K21	M27	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K20	M26	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	G28	D34	DQSn3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G27	D33	DQS3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K26	K30	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K25	K29	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26	J32		
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25	J31		
1A	VREFB1AN0	IO						N26		
1A	VREFB1AN0	IO						P25		
1A	VREFB1AN0	IO						K32		
1A	VREFB1AN0	IO						K31		
1A	VREFB1AN0	IO						L32		
1A	VREFB1AN0	IO						L31		
1A	VREFB1AN0	IO						G34		
1A	VREFB1AN0	IO						H34		
1A	VREFB1AN0	IO						N24		
1A	VREFB1AN0	IO						P23		
1A	VREFB1AN0	IO						J34		
1A	VREFB1AN0	IO						J33		
1A	VREFB1AN0	IO						M30		
1A	VREFB1AN0	IO						M29		
1A	VREFB1AN0	IO						K34		
1A	VREFB1AN0	IO						K33		
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	M23	R28		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	M22	R27		
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	L26	R32	DQSn5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	L25	P31	DQS5L	
1C	VREFB1CN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	M21	R30	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	M20	R29	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	K28	N34	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	L28	P34	DQ5L	
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	N21	T28	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	N20	T27	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	M26	R34	DQSn6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	M25	R33	DQS6L	DQ5L/CQn5L
1C	VREFB1CN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	N25	T25	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	M24	T24	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	M28	T32	DQSn7L	DQSn5L/DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	M27	R31	DQS7L	DQS5L/CQ5L
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	N23	T26	DQ7L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	P23	U25	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	P25	U32	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	N24	U31	DQ7L	DQ5L
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	P20	T30		
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	P19	T29		
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	N27	V32		
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	N26	V31		
1C	VREFB1CN0	CLK1n	CLK1n				N28	T34		
1C	VREFB1CN0	CLK1p	CLK1p				P28	T33		
1C	VREFB1CN0	IO						N30		
1C	VREFB1CN0	IO						N29		
1C	VREFB1CN0	IO						N32		
1C	VREFB1CN0	IO						M31		
1C	VREFB1CN0	IO						P29		
1C	VREFB1CN0	IO						P28		
1C	VREFB1CN0	IO						L34		
1C	VREFB1CN0	IO						M33		
1C	VREFB1CN0	IO						R26		
1C	VREFB1CN0	IO						R25		
1C	VREFB1CN0	IO						P32		
1C	VREFB1CN0	IO						N31		
1C	VREFB1CN0	IO						R24		
1C	VREFB1CN0	IO						T23		
1C	VREFB1CN0	IO						M34		
1C	VREFB1CN0	IO						N33		
2C	VREFB2CN0	CLK3p	CLK3p				R27	V33		
2C	VREFB2CN0	CLK3n	CLK3n				R28	V34		
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	U28	W33		
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	T28	W34		
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	R20	W28		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	R21	V29		
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	R26	AA33	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	T27	Y34	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	T25	W26	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	R25	W27	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	V27	Y31	DQS8L	DQS10L/CQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	V28	Y32	DQSn8L	DQSn10L/DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	T20	V24	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	T21	V25	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	V26	AB33	DQS9L	DQ10L/CQn10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	U26	AA34	DQSn9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	T24	W30	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	U25	W31	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	W27	AA31	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	W28	AA32	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	T22	Y28	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	T23	Y29	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	V24	AC34	DQS10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	V25	AB34	DQSn10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	V23	Y23		
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	U23	W24		
2C	VREFB2CN0	IO						AB31		
2C	VREFB2CN0	IO						AB32		
2C	VREFB2CN0	IO						AA29		
2C	VREFB2CN0	IO						AA30		
2C	VREFB2CN0	IO						AD33		
2C	VREFB2CN0	IO						AD34		
2C	VREFB2CN0	IO						Y25		
2C	VREFB2CN0	IO						Y26		
2C	VREFB2CN0	IO						AC31		
2C	VREFB2CN0	IO						AC32		
2C	VREFB2CN0	IO						AA27		
2C	VREFB2CN0	IO						AA28		
2C	VREFB2CN0	IO						AE33		
2C	VREFB2CN0	IO						AE34		
2C	VREFB2CN0	IO						AB29		
2C	VREFB2CN0	IO						AB30		
2A	VREFB2AN0	IO						AG33		
2A	VREFB2AN0	IO						AF34		
2A	VREFB2AN0	IO						AA24		
2A	VREFB2AN0	IO						AA25		
2A	VREFB2AN0	IO						AE31		
2A	VREFB2AN0	IO						AE32		
2A	VREFB2AN0	IO						AC28		
2A	VREFB2AN0	IO						AC29		
2A	VREFB2AN0	IO						AH33		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
2A	VREFB2AN0	IO						AG34		
2A	VREFB2AN0	IO						AD30		
2A	VREFB2AN0	IO						AD31		
2A	VREFB2AN0	IO						AF31		
2A	VREFB2AN0	IO						AF32		
2A	VREFB2AN0	IO						AB24		
2A	VREFB2AN0	IO						AB25		
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	Y25	AK33		
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	Y26	AK34		
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	V20	AD28	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	V21	AD29	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC28	AJ31	DQS12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AB28	AJ32	DQSn12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AA25	AF28	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	AA26	AF29	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AB25	AM34	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AB26	AL34	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AC25	AE27	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AC26	AE28	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AD27	AH30	DQS13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AD28	AH31	DQSn13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	W20	AD26	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	W21	AD27	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AG28	AL32	DQS14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AF28	AL33	DQSn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	Y23	AC25	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AA24	AC26	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AE27	AK31		
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AE28	AK32		
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AA23	AG29		
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AB24	AG30		
		nCONFIG		nCONFIG			W19	AE25		
		nSTATUS		nSTATUS			AD25	AH28		
		CONF_DONE		CONF_DONE			AE26	AH29		
		PORSEL		PORSEL			AB23	AF26		
		nCE		nCE			Y20	AE26		
3A	VREFB3AN0	IO				DIFFOUT_B1n	AF26	AH27	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AH27	AJ27	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AH25	AK28	DQSn1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AG25	AJ28	DQS1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AG27	AJ29	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AH26	AJ26	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE22	AM32	DQSn2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD22	AM31	DQS2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AB20	AL29	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AB21	AM29	DQ2B	DQ1B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AD21	AN30	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AC21	AM30	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AC20	AK27	DQ5B	DQ2B
3A	VREFB3AN0	IO				DIFFOUT_B13p	AG21	AL28	DQ5B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21	AL27	DQSn5B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21	AL26	DQS5B	DQ2B/CQn2B
3A	VREFB3AN0	IO				DIFFOUT_B15n	AF20	AK25	DQ5B	DQ2B
3A	VREFB3AN0	IO				DIFFOUT_B15p	AE20	AM26	DQ5B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AD19	AP28	DQSn6B	DQSn2B/DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AC19	AN28	DQS6B	DQS2B/CQ2B
3A	VREFB3AN0	IO				DIFFOUT_B17n	AB19	AM28	DQ6B	DQ2B
3A	VREFB3AN0	IO				DIFFOUT_B17p	AA19	AP29	DQ6B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19	AP27	DQ6B	DQ2B
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD18	AN27	DQ6B	DQ2B
3B	VREFB3BN0	IO						AH23		
3B	VREFB3BN0	IO						AJ24		
3B	VREFB3BN0	IO						AJ22		
3B	VREFB3BN0	IO						AH22		
3B	VREFB3BN0	IO						AJ23		
3B	VREFB3BN0	IO						AK22		
3B	VREFB3BN0	IO						AM24		
3B	VREFB3BN0	IO						AL24		
3B	VREFB3BN0	IO						AK24		
3B	VREFB3BN0	IO						AL25		
3B	VREFB3BN0	IO						AM23		
3B	VREFB3BN0	IO						AL23		
3B	VREFB3BN0	IO						AE22		
3B	VREFB3BN0	IO						AE21		
3B	VREFB3BN0	IO						AG21		
3B	VREFB3BN0	IO						AF21		
3B	VREFB3BN0	IO						AD21		
3B	VREFB3BN0	IO						AE20		
3B	VREFB3BN0	IO						AP25		
3B	VREFB3BN0	IO						AN25		
3B	VREFB3BN0	IO						AP26		
3B	VREFB3BN0	IO						AP23		
3B	VREFB3BN0	IO						AP24		
3B	VREFB3BN0	IO						AN24		
3C	VREFB3CN0	IO				DIFFOUT_B21n	AF19	AL22	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B21p	AG19	AM22	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AH19	AL21	DQSn7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AG18	AK21	DQS7B	DQ7B/CQn7B
3C	VREFB3CN0	IO				DIFFOUT_B23n	AH17	AJ20	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B23p	AH18	AJ21	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AF17	AP22	DQSn8B	DQSn7B/DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AE18	AN22	DQS8B	DQS7B/CQ7B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
3C	VREFB3CN0	IO				DIFFOUT_B25n	AE16	AM21	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B25p	AD16	AP20	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF16	AP21	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE17	AN21	DQ8B	DQ7B
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	AC17	AE19		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	AB17	AD19		
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AC16	AH19		
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AB16	AG19		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AA15	AE18		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	Y15	AD18		
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AH16	AK19		
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AG16	AJ19		
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AH15	AP19		
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AG15	AN19		
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AF15	AP18		
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AE15	AN18		
3C	VREFB3CN0	IO						AL20		
3C	VREFB3CN0	IO						AM18		
3C	VREFB3CN0	IO						AM19		
3C	VREFB3CN0	IO						AL19		
3C	VREFB3CN0	IO						AK18		
3C	VREFB3CN0	IO						AL18		
3C	VREFB3CN0	IO						AF20		
3C	VREFB3CN0	IO						AF19		
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AE14	AN16		
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AF14	AP16		
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AG13	AN15		
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AH14	AP15		
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AG12	AJ16		
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AH13	AK16		
4C	VREFB4CN0	IO				DIFFOUT_B36p	Y13	AL15	DQ9B	
4C	VREFB4CN0	IO				DIFFOUT_B36n	Y14	AM15	DQ9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AD13	AL14	DQS9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AE13	AM14	DQSn9B	
4C	VREFB4CN0	IO				DIFFOUT_B38p	AA13	AK13	DQ9B	
4C	VREFB4CN0	IO				DIFFOUT_B38n	AB13	AL13	DQ9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AG10	AH15	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AH10	AJ15	DQ10B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B40p	AH11	AG15	DQ10B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B40n	AH12	AK15	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AF10	AH14	DQS10B	DQS11B/CQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AF11	AJ14	DQSn10B	DQSn11B/DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42p	AF12	AP14	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42n	AC12	AN13	DQ11B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AD12	AN12	DQS11B	DQ11B/CQn11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AE12	AP12	DQSn11B	DQ11B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
4C	VREFB4CN0	IO				DIFFOUT_B44p	AC11	AM12	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B44n	AE11	AP13	DQ11B	DQ11B
4C	VREFB4CN0	IO						AL17		
4C	VREFB4CN0	IO						AM17		
4C	VREFB4CN0	IO						AE16		
4C	VREFB4CN0	IO						AF16		
4C	VREFB4CN0	IO						AL16		
4C	VREFB4CN0	IO						AM16		
4C	VREFB4CN0	IO						AD15		
4C	VREFB4CN0	IO						AD16		
4B	VREFB4BN0	IO						AN10		
4B	VREFB4BN0	IO						AP10		
4B	VREFB4BN0	IO						AP9		
4B	VREFB4BN0	IO						AP11		
4B	VREFB4BN0	IO						AM9		
4B	VREFB4BN0	IO						AN9		
4B	VREFB4BN0	IO						AE15		
4B	VREFB4BN0	IO						AF15		
4B	VREFB4BN0	IO						AF13		
4B	VREFB4BN0	IO						AF14		
4B	VREFB4BN0	IO						AE13		
4B	VREFB4BN0	IO						AE14		
4B	VREFB4BN0	IO						AK12		
4B	VREFB4BN0	IO						AL12		
4B	VREFB4BN0	IO						AK10		
4B	VREFB4BN0	IO						AM11		
4B	VREFB4BN0	IO						AL10		
4B	VREFB4BN0	IO						AL11		
4B	VREFB4BN0	IO						AM8		
4B	VREFB4BN0	IO						AP8		
4B	VREFB4BN0	IO						AN7		
4B	VREFB4BN0	IO						AP7		
4B	VREFB4BN0	IO						AP6		
4B	VREFB4BN0	IO						AM7		
4A	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AG9	AH12	DQ12B	DQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AH8	AJ12	DQ12B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B48p	AE10	AG12	DQ12B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B48n	AH9	AJ13	DQ12B	DQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AE9	AH11	DQS12B	DQS16B/CQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AF9	AJ11	DQSn12B	DQSn16B/DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B50p	AF8	AJ10	DQ13B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B50n	AE8	AL8	DQ13B	DQ16B
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AG7	AK9	DQS13B	DQ16B/CQn16B
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AH7	AL9	DQSn13B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B52p	AG6	AL7	DQ13B	DQ16B
4A	VREFB4AN0	IO				DIFFOUT_B52n	AH6	AJ9	DQ13B	DQ16B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AE6	AJ7	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AF6	AK7	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60p	AE4	AJ6	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60n	AE7	AK6	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AE5	AH8	DQS16B	DQS17B/CQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AF5	AJ8	DQSn16B	DQSn17B/DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62p	AB8	AE11	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62n	AC8	AF11	DQ17B	DQ17B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AC7	AG9	DQS17B	DQ17B/CQn17B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AD7	AH9	DQSn17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64p	AB7	AE10	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64n	AD6	AF10	DQ17B	DQ17B
		nIO_PULLUP		nIO_PULLUP			AE3	AF8		
		nCEO		nCEO			AB5	AJ5		
		DCLK		DCLK			AC5	AL3		
		nCSO		nCSO			AD4	AE9		
		ASDO		ASDO			AA6	AH6		
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AC3	AH4		
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AC4	AH5		
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AF1	AK3		
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AE2	AK4		
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AB3	AE7	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AB4	AE8	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AG1	AM1	DQSn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AF2	AM2	DQS1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	Y6	AF5	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	Y7	AF6	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AE1	AJ3	DQSn2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AD1	AJ4	DQS2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AA4	AC8	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	Y5	AC9	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AC1	AL1	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AC2	AL2	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	Y3	AE5	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	Y4	AE6	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AB1	AG3	DQSn3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AB2	AG4	DQS3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	W8	AB10	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	W9	AC11	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AA1	AK1		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	Y2	AJ2		
5A	VREFB5AN0	IO						AB9		
5A	VREFB5AN0	IO						AA10		
5A	VREFB5AN0	IO						AH1		
5A	VREFB5AN0	IO						AG1		
5A	VREFB5AN0	IO						AC5		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
5A	VREFB5AN0	IO						AC6		
5A	VREFB5AN0	IO						AF1		
5A	VREFB5AN0	IO						AF2		
5A	VREFB5AN0	IO						AB11		
5A	VREFB5AN0	IO						AA12		
5A	VREFB5AN0	IO						AE3		
5A	VREFB5AN0	IO						AE4		
5A	VREFB5AN0	IO						AD3		
5A	VREFB5AN0	IO						AD4		
5A	VREFB5AN0	IO						AE1		
5A	VREFB5AN0	IO						AE2		
5C	VREFB5CN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	U6	Y11		
5C	VREFB5CN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	U7	W12		
5C	VREFB5CN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	V3	Y3	DQSn5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	V4	AA4	DQS5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	U8	Y5	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	U9	Y6	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	W1	AB1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	V1	AA1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	T4	W7	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	U5	W8	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	U3	W3	DQSn6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	U4	Y4	DQS6R	DQ5R/CQn5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	T8	W10	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	T9	W11	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	T2	Y1	DQSn7R	DQSn5R/DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	T3	Y2	DQS7R	DQS5R/CQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	T6	W5	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	R6	W6	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	R4	V3	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	T5	V4	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	R9	W9		
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	R10	V10		
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R14n	DIFFOUT_R28n	U1	U3		
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R14p	DIFFOUT_R28p	U2	U4		
5C	VREFB5CN0	CLK8n	CLK8n				T1	W1		
5C	VREFB5CN0	CLK8p	CLK8p				R1	W2		
5C	VREFB5CN0	IO						AB5		
5C	VREFB5CN0	IO						AB6		
5C	VREFB5CN0	IO						AB3		
5C	VREFB5CN0	IO						AC4		
5C	VREFB5CN0	IO						AA6		
5C	VREFB5CN0	IO						AA7		
5C	VREFB5CN0	IO						AD1		
5C	VREFB5CN0	IO						AC2		
5C	VREFB5CN0	IO						Y9		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
5C	VREFB5CN0	IO						Y10		
5C	VREFB5CN0	IO						AA3		
5C	VREFB5CN0	IO						AB4		
5C	VREFB5CN0	IO						Y7		
5C	VREFB5CN0	IO						Y8		
5C	VREFB5CN0	IO						AC1		
5C	VREFB5CN0	IO						AB2		
6C	VREFB6CN0	CLK10p	CLK10p				P2	U2		
6C	VREFB6CN0	CLK10n	CLK10n				P1	U1		
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R15p	DIFFOUT_R29p	M1	T2		
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R15n	DIFFOUT_R29n	N1	T1		
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R15p	DIFFOUT_R30p	P9	U11		
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R15n	DIFFOUT_R30n	P8	U10		
6C	VREFB6CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R31p	N4	P2	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R31n	P4	R1	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R32p	N7	T7	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R32n	N6	U6	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R33p	P3	R4	DQS8R	DQS10R/CQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R33n	N2	R3	DQSn8R	DQSn10R/DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R34p	N5	T9	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R34n	M4	T8	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R35p	L2	N2	DQS9R	DQ10R/CQn10R
6C	VREFB6CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R35n	L1	P1	DQSn9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R36p	N9	T5	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R36n	N8	T4	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R37p	L3	P4	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R37n	M3	P3	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R38p	L5	R7	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R38n	L4	R6	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R39p	K2	M1	DQS10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R39n	K1	N1	DQSn10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R40p	L6	P6		
6C	VREFB6CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R40n	M6	P5		
6C	VREFB6CN0	IO						N4		
6C	VREFB6CN0	IO						N3		
6C	VREFB6CN0	IO						R12		
6C	VREFB6CN0	IO						T11		
6C	VREFB6CN0	IO						L2		
6C	VREFB6CN0	IO						L1		
6C	VREFB6CN0	IO						R10		
6C	VREFB6CN0	IO						R9		
6C	VREFB6CN0	IO						M4		
6C	VREFB6CN0	IO						M3		
6C	VREFB6CN0	IO						P8		
6C	VREFB6CN0	IO						P7		
6C	VREFB6CN0	IO						K2		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
6C	VREFB6CN0	IO						K1		
6C	VREFB6CN0	IO						N6		
6C	VREFB6CN0	IO						N5		
6A	VREFB6AN0	IO						H2		
6A	VREFB6AN0	IO						J1		
6A	VREFB6AN0	IO						P11		
6A	VREFB6AN0	IO						P10		
6A	VREFB6AN0	IO						K4		
6A	VREFB6AN0	IO						K3		
6A	VREFB6AN0	IO						M7		
6A	VREFB6AN0	IO						M6		
6A	VREFB6AN0	IO						G2		
6A	VREFB6AN0	IO						H1		
6A	VREFB6AN0	IO						L5		
6A	VREFB6AN0	IO						L4		
6A	VREFB6AN0	IO						J4		
6A	VREFB6AN0	IO						J3		
6A	VREFB6AN0	IO						L7		
6A	VREFB6AN0	IO						L6		
6A	VREFB6AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R45p	F1	E2		
6A	VREFB6AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R45n	G1	E1		
6A	VREFB6AN0	IO			DIFFIO_TX_R23p	DIFFOUT_R46p	J4	N11	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R23n	DIFFOUT_R46n	J3	N10	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	E2	F4	DQS12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	E1	F3	DQSn12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	L9	J7	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	L8	J6	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	H4	G5	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	H3	G4	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	K9	K8	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	K8	K7	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	D2	C1	DQS13R	DQS14R/CQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	D1	D1	DQSn13R	DQSn14R/DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	J6	M10	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	H5	M9	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	F4	D3	DQS14R	DQ14R/CQn14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	F3	D2	DQSn14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	G4	L9	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	G3	L8	DQ14R	DQ14R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R28p	DIFFOUT_R55p	B1	E4		
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R28n	DIFFOUT_R55n	C1	E3		
6A	VREFB6AN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	H6	H6		
6A	VREFB6AN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	G5	H5		
7A	VREFB7AN0	IO				DIFFOUT_T1n	A2	F8	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C3	F6	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A4	E7	DQSn1T	DQ1T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B4	F7	DQS1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	A3	F9	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B2	G8	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D7	C3	DQSn2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E7	C4	DQS2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	G8	C6	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	G9	D6	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	E8	B5	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	F8	C5	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B8	D7	DQ5T	DQ2T
7A	VREFB7AN0	IO				DIFFOUT_T13p	F9	E8	DQ5T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	C9	DQSn5T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	D9	DQS5T	DQ2T/CQn2T
7A	VREFB7AN0	IO				DIFFOUT_T15n	D9	E10	DQ5T	DQ2T
7A	VREFB7AN0	IO				DIFFOUT_T15p	C9	D8	DQ5T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	E10	A7	DQSn6T	DQSn2T/DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	F10	B7	DQS6T	DQS2T/CQ2T
7A	VREFB7AN0	IO				DIFFOUT_T17n	H10	A6	DQ6T	DQ2T
7A	VREFB7AN0	IO				DIFFOUT_T17p	G10	C7	DQ6T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	D10	A8	DQ6T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	E11	B8	DQ6T	DQ2T
7B	VREFB7BN0	IO						G12		
7B	VREFB7BN0	IO						F11		
7B	VREFB7BN0	IO						F12		
7B	VREFB7BN0	IO						F13		
7B	VREFB7BN0	IO						G13		
7B	VREFB7BN0	IO						E11		
7B	VREFB7BN0	IO						C11		
7B	VREFB7BN0	IO						D11		
7B	VREFB7BN0	IO						D13		
7B	VREFB7BN0	IO						D10		
7B	VREFB7BN0	IO						C12		
7B	VREFB7BN0	IO						D12		
7B	VREFB7BN0	IO						K14		
7B	VREFB7BN0	IO						K13		
7B	VREFB7BN0	IO						H14		
7B	VREFB7BN0	IO						J14		
7B	VREFB7BN0	IO						K15		
7B	VREFB7BN0	IO						L14		
7B	VREFB7BN0	IO						A10		
7B	VREFB7BN0	IO						B10		
7B	VREFB7BN0	IO						A12		
7B	VREFB7BN0	IO						A9		
7B	VREFB7BN0	IO						A11		
7B	VREFB7BN0	IO						B11		
7C	VREFB7CN0	IO				DIFFOUT_T21n	B10	D14	DQ7T	DQ7T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
7C	VREFB7CN0	IO				DIFFOUT_T21p	C10	E13	DQ7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	A10	E14	DQSn7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	B11	F14	DQS7T	DQ7T/CQn7T
7C	VREFB7CN0	IO				DIFFOUT_T23n	A11	F15	DQ7T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T23p	A12	D15	DQ7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	C12	A13	DQSn8T	DQSn7T/DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	D11	B13	DQS8T	DQS7T/CQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25n	E13	A15	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25p	D13	C14	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C13	A14	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D12	B14	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T27n	G12	C17	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T27p	F12	C15	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	F13	C16	DQSn9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	G13	D16	DQS9T	
7C	VREFB7CN0	IO				DIFFOUT_T29n	H14	D17	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T29p	J14	E17	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	A13	J16		
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	B13	J15		
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A14	A16		
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B14	B16		
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	C14	A17		
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	D14	B17		
7C	VREFB7CN0	IO						L16		
7C	VREFB7CN0	IO						K16		
7C	VREFB7CN0	IO						G16		
7C	VREFB7CN0	IO						H16		
7C	VREFB7CN0	IO						K17		
7C	VREFB7CN0	IO						L17		
7C	VREFB7CN0	IO						E16		
7C	VREFB7CN0	IO						F16		
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	D15	B19		
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	C15	A19		
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	B16	B20		
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	A15	A20		
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	B17	D18		
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	A16	C18		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	J16	K19		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	J15	J19		
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	E16	D19		
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D16	C19		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	G16	L19		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	H16	L20		
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	B19	G20	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A19	F20	DQ10T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T40p	A17	E20	DQ10T	DQ11T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
8C	VREFB8CN0	IO				DIFFOUT_T40n	A18	H20	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C19	G21	DQS10T	DQS11T/CQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C18	F21	DQSn10T	DQSn11T/DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42p	F17	A22	DQ11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42n	C17	A21	DQ11T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	E17	B23	DQS11T	DQ11T/CQn11T
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	D17	A23	DQSn11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T44p	D18	B22	DQ11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T44n	F18	C23	DQ11T	DQ11T
8C	VREFB8CN0	IO						F19		
8C	VREFB8CN0	IO						E19		
8C	VREFB8CN0	IO						C20		
8C	VREFB8CN0	IO						D20		
8C	VREFB8CN0	IO						D21		
8C	VREFB8CN0	IO						C21		
8C	VREFB8CN0	IO						D22		
8C	VREFB8CN0	IO						E22		
8B	VREFB8BN0	IO						B25		
8B	VREFB8BN0	IO						A25		
8B	VREFB8BN0	IO						A24		
8B	VREFB8BN0	IO						A26		
8B	VREFB8BN0	IO						C26		
8B	VREFB8BN0	IO						B26		
8B	VREFB8BN0	IO						K20		
8B	VREFB8BN0	IO						J20		
8B	VREFB8BN0	IO						J22		
8B	VREFB8BN0	IO						J21		
8B	VREFB8BN0	IO						K21		
8B	VREFB8BN0	IO						K22		
8B	VREFB8BN0	IO						D25		
8B	VREFB8BN0	IO						D24		
8B	VREFB8BN0	IO						C24		
8B	VREFB8BN0	IO						E25		
8B	VREFB8BN0	IO						E23		
8B	VREFB8BN0	IO						D23		
8B	VREFB8BN0	IO						A27		
8B	VREFB8BN0	IO						C27		
8B	VREFB8BN0	IO						B28		
8B	VREFB8BN0	IO						A28		
8B	VREFB8BN0	IO						C28		
8B	VREFB8BN0	IO						A29		
8A	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	B20	G23	DQ12T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	A21	F23	DQ12T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T48p	A20	F22	DQ12T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T48n	D19	H23	DQ12T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	D20	G24	DQS12T	DQS16T/CQ16T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	C20	F24	DQSn12T	DQSn16T/DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T50p	D21	F25	DQ13T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T50n	C21	D27	DQ13T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	B22	E26	DQS13T	DQ16T/CQn16T
8A	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	A22	D26	DQSn13T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T52p	A23	F26	DQ13T	DQ16T
8A	VREFB8AN0	IO				DIFFOUT_T52n	B23	D28	DQ13T	DQ16T
8A	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	D23	F28	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	C23	E28	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60p	D22	F27	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60n	D25	G27	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	D24	F29	DQS16T	DQS17T/CQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C24	E29	DQSn16T	DQSn17T/DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62p	F21	J24	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62n	G21	K24	DQ17T	DQ17T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	F22	H26	DQS17T	DQ17T/CQn17T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	E22	G26	DQSn17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64p	E23	J25	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64n	G22	K25	DQ17T	DQ17T
		GND					M17	V2		
		GND					AF3	AF9		
		GND					R14	V17		
		GND					K11	E21		
		GND					B24	N14		
		GND					AG2	AN5		
		GND					AG5	AN8		
		GND					AG8	AN11		
		GND					AG11	AN14		
		GND					AG14	AN17		
		GND					AG17	AN20		
		GND					AG20	AN23		
		GND					AG23	AN26		
		GND					AG26	AN29		
		GND					AF27	AN32		
		GND					AD2	AM33		
		GND					AD5	AK2		
		GND					AD8	AK5		
		GND					AD11	AK8		
		GND					AD14	AK11		
		GND					AD17	AK14		
		GND					AD20	AK17		
		GND					AD23	AK20		
		GND					AC24	AK23		
		GND					AC27	AK26		
		GND					AA2	AK29		
		GND					AA5	AJ30		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		GND					AA8	AJ33		
		GND					AA11	AG2		
		GND					AA14	AG5		
		GND					AA17	AG8		
		GND					AA20	AG11		
		GND					Y12	AG14		
		GND					Y16	AG17		
		GND					Y21	AG20		
		GND					Y24	AG23		
		GND					Y27	AG26		
		GND					W12	AF27		
		GND					W14	AF30		
		GND					W16	AF33		
		GND					W18	AD2		
		GND					V2	AD5		
		GND					V5	AD8		
		GND					V8	AD11		
		GND					V11	AD14		
		GND					V13	AD17		
		GND					V15	AD20		
		GND					V17	AD23		
		GND					V19	AC14		
		GND					U10	AC16		
		GND					U12	AC18		
		GND					U14	AC20		
		GND					U16	AC24		
		GND					U18	AC27		
		GND					U21	AC30		
		GND					U24	AC33		
		GND					U27	AB13		
		GND					T11	AB15		
		GND					T13	AB17		
		GND					T15	AB19		
		GND					T17	AB21		
		GND					T19	AB23		
		GND					R2	AA2		
		GND					R5	AA5		
		GND					R8	AA8		
		GND					R12	AA11		
		GND					R16	AA14		
		GND					R18	AA16		
		GND					P11	AA18		
		GND					P13	AA20		
		GND					P17	AA22		
		GND					P21	Y13		
		GND					P24	Y15		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		GND					P27	Y17		
		GND					N10	Y19		
		GND					N12	Y21		
		GND					N14	Y24		
		GND					N16	Y27		
		GND					N18	Y30		
		GND					M2	Y33		
		GND					M5	W14		
		GND					M8	W16		
		GND					M11	W18		
		GND					M13	W20		
		GND					M15	W22		
		GND					M19	V5		
		GND					L10	V8		
		GND					L12	V11		
		GND					L14	V12		
		GND					L16	V13		
		GND					L18	V15		
		GND					L21	V19		
		GND					L24	V21		
		GND					L27	V23		
		GND					K13	U12		
		GND					K15	U14		
		GND					K17	U16		
		GND					K19	U20		
		GND					J2	U22		
		GND					J5	U23		
		GND					J8	U24		
		GND					J13	U27		
		GND					J17	U30		
		GND					H9	U33		
		GND					H12	T13		
		GND					H15	T15		
		GND					H18	T17		
		GND					H21	T19		
		GND					H24	T21		
		GND					H27	R2		
		GND					F2	R5		
		GND					F5	R8		
		GND					E6	R11		
		GND					E9	R14		
		GND					E12	R16		
		GND					E15	R18		
		GND					E18	R20		
		GND					E21	R22		
		GND					E24	P13		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		GND					E27	P15		
		GND					C2	P17		
		GND					B3	P19		
		GND					B6	P21		
		GND					B9	P24		
		GND					B12	P27		
		GND					B15	P30		
		GND					B18	P33		
		GND					B21	N12		
		GND					B27	AN2		
		GND						N16		
		GND						N18		
		GND						N20		
		GND						N22		
		GND						M2		
		GND						M5		
		GND						M8		
		GND						M11		
		GND						M15		
		GND						M17		
		GND						M19		
		GND						M21		
		GND						L12		
		GND						L15		
		GND						L18		
		GND						L21		
		GND						L24		
		GND						L27		
		GND						L30		
		GND						L33		
		GND						J2		
		GND						J5		
		GND						J8		
		GND						H9		
		GND						H12		
		GND						H15		
		GND						H18		
		GND						H21		
		GND						H24		
		GND						H27		
		GND						H30		
		GND						H33		
		GND						F2		
		GND						F5		
		GND						E6		
		GND						E9		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		GND						E12		
		GND						E15		
		GND						E18		
		GND						E24		
		GND						E27		
		GND						E30		
		GND						E33		
		GND						C2		
		GND						B3		
		GND						B6		
		GND						B9		
		GND						B12		
		GND						B15		
		GND						B18		
		GND						B21		
		GND						B24		
		GND						B27		
		GND						B30		
		GND						B33		
		VCCL					R15	U17		
		VCCL					L17	T14		
		VCCL					V14	AB22		
		VCCL					V18	AA13		
		VCCL					U11	AA15		
		VCCL					U13	AA17		
		VCCL					U15	AA19		
		VCCL					U17	AA21		
		VCCL					T12	Y14		
		VCCL					T14	Y16		
		VCCL					T16	Y18		
		VCCL					R13	Y20		
		VCCL					R17	W15		
		VCCL					P12	W17		
		VCCL					P14	W19		
		VCCL					P16	W21		
		VCCL					P18	V14		
		VCCL					N13	V16		
		VCCL					N15	V18		
		VCCL					N17	AB14		
		VCCL					M12	V20		
		VCCL					M14	U15		
		VCCL					M16	U19		
		VCCL					L11	U21		
		VCCL						T16		
		VCCL						T18		
		VCCL						T20		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		VCCL						R15		
		VCCL						R17		
		VCCL						R19		
		VCCL						R21		
		VCCL						P14		
		VCCL						P16		
		VCCL						P18		
		VCCL						P20		
		VCCL						P22		
		VCCL						N13		
		VCCL						N21		
		VCC					T18	AB20		
		VCC					V12	AB16		
		VCC					V16	AB18		
		VCC					R11	Y22		
		VCC					N11	W13		
		VCC					M18	N19		
		VCC					L13	V22		
		VCC					L15	U13		
		VCC						T22		
		VCC						R13		
		VCC						N15		
		VCC						N17		
		VCCPT					G23	J27		
		VCCPT					AC23	AG27		
		VCCPT					AB6	AG7		
		VCCPT					G6	H8		
		DNU					P15	U18		
		VCCPGM					AA21	AD24		
		VCCPGM					Y8	AD10		
		TEMPDIODEn					D4	D4		
		TEMPDIODEp					D3	E5		
		VCC_CLKIN3C					AB14	AG18		
		VCC_CLKIN4C					AC13	AE17		
		VCC_CLKIN7C					F14	H17		
		VCC_CLKIN8C					F16	K18		
		VCCA_PLL_B1					AC14	AH18		
		VCCA_PLL_L2					R22	U28		
		VCCA_PLL_R2					R7	U7		
		VCCA_PLL_T1					F15	G18		
		VCCA_PLL_L3						V28		
		VCCA_PLL_B2						AH17		
		VCCA_PLL_R3						V7		
		VCCA_PLL_T2						G17		
		VCCD_PLL_B1					AB15	AF18		
		VCCD_PLL_L2					P22	U26		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		VCCD_PLL_R2					P7	U9		
		VCCD_PLL_T1					G15	J18		
		VCCD_PLL_L3						V26		
		VCCD_PLL_B2						AF17		
		VCCD_PLL_R3						V9		
		VCCD_PLL_T2						J17		
		VCCIO1A					E26	H29		
		VCCIO1A					H23	L26		
		VCCIO1A					H26	N28		
		VCCIO1A						G32		
		VCCIO1A						B34		
		VCCIO1C					P26	M32		
		VCCIO1C					R23	V30		
		VCCIO1C						U34		
		VCCIO1C						T31		
		VCCIO2A					W26	AH32		
		VCCIO2A					AD26	AB28		
		VCCIO2A					AA22	AN34		
		VCCIO2A						AG28		
		VCCIO2A						AD25		
		VCCIO2C					T26	W25		
		VCCIO2C					V22	AD32		
		VCCIO2C						W29		
		VCCIO2C						W32		
		VCCIO3A					AC22	AM27		
		VCCIO3A					AF22	AL30		
		VCCIO3A					AF25	AJ25		
		VCCIO3A					AC18	AF25		
		VCCIO3B						AF22		
		VCCIO3B						AM25		
		VCCIO3C					AF18	AM20		
		VCCIO3C					AC15	AH21		
		VCCIO3C						AJ18		
		VCCIO4A					AC6	AH10		
		VCCIO4A					AF4	AM3		
		VCCIO4A					AF7	AL6		
		VCCIO4A					AD10	AF12		
		VCCIO4B						AH13		
		VCCIO4B						AM10		
		VCCIO4C					AB12	AG16		
		VCCIO4C					AF13	AP17		
		VCCIO4C						AM13		
		VCCIO5A					AA7	AH3		
		VCCIO5A					AD3	AD9		
		VCCIO5A					AA3	AN1		
		VCCIO5A						AG6		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		VCCIO5A						AB7		
		VCCIO5C					P6	AC3		
		VCCIO5C					R3	W4		
		VCCIO5C						V1		
		VCCIO5C						U5		
		VCCIO6A					E3	H7		
		VCCIO6A					K3	L10		
		VCCIO6A					H7	N7		
		VCCIO6A						G3		
		VCCIO6A						B1		
		VCCIO6C					L7	T10		
		VCCIO6C					N3	T3		
		VCCIO6C						T6		
		VCCIO6C						L3		
		VCCIO7A					C7	C8		
		VCCIO7A					F7	J10		
		VCCIO7A					F11	F10		
		VCCIO7A					C4	D5		
		VCCIO7B						C10		
		VCCIO7B						J13		
		VCCIO7C					C11	C13		
		VCCIO7C					G14	G14		
		VCCIO7C						F17		
		VCCIO8A					C25	D29		
		VCCIO8A					F23	J23		
		VCCIO8A					E19	G25		
		VCCIO8A					C22	C32		
		VCCIO8B						C25		
		VCCIO8B						G22		
		VCCIO8C					C16	C22		
		VCCIO8C					G17	H19		
		VCCIO8C						A18		
		VCCPD1A					L19	N23		
		VCCPD1C					N19	R23		
		VCCPD2A					U19	AA23		
		VCCPD2C					R19	W23		
		VCCPD3A					W17	AC23		
		VCCPD3B						AC21		
		VCCPD3C					W15	AC19		
		VCCPD4A					W11	AC13		
		VCCPD4B						AC15		
		VCCPD4C					W13	AC17		
		VCCPD5A					V10	AB12		
		VCCPD5C					T10	Y12		
		VCCPD6A					M10	P12		
		VCCPD6C					P10	T12		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		VCCPD7A					K12	M12		
		VCCPD7B						M14		
		VCCPD7C					K14	M16		
		VCCPD8A					K18	M22		
		VCCPD8B						M20		
		VCCPD8C					K16	M18		
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				K22	J26		
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				N22	P26		
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				Y22	AA26		
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				U22	V27		
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB18	AG25		
3B	VREFB3BN0	VREFB3BN0						AG22		
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AA16	AH20		
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB10	AG10		
4B	VREFB4BN0	VREFB4BN0						AG13		
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AA12	AH16		
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				W7	AF7		
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				T7	AA9		
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				J7	P9		
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				M7	U8		
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G11	H10		
7B	VREFB7BN0	VREFB7BN0						H13		
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				H13	G15		
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G19	H25		
8B	VREFB8BN0	VREFB8BN0						H22		
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				H17	G19		
		NC					E25	D32		
		NC					AB22	AL31		
		NC					W10	AH7		
		NC					E4	G7		
		NC					V9	AC10		
		NC *(3)*		MSEL2			G7	K9		
		NC *(3)*		MSEL1			J9	J9		
		NC *(3)*		MSEL0			H8	K10		
		NC *(4)*					F6	G6		
		NC *(5)*					R24	U29		
		NC *(5)*					AD15	AJ17		
		NC *(5)*					P5	V6		
		NC *(5)*					E14	F18		
		NC					AE25	AK30		
		NC					U20	M25		
		NC					M9	L11		
		NC					L20	L25		
		NC					K10	K26		
		NC					J21			
		NC *(6)*					K24	L29		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		NC *(6)*					K23	L28		
		NC *(6)*					H28	E34		
		NC *(6)*					J27	F33		
		NC *(6)*					L23	M28		
		NC *(6)*					L22	N27		
		NC *(6)*					J28	F34		
		NC *(6)*					K27	G33		
		NC *(6)*					AA27	AJ34		
		NC *(6)*					Y28	AH34		
		NC *(6)*					W22	AB26		
		NC *(6)*					W23	AB27		
		NC *(6)*					AB27	AG31		
		NC *(6)*					AA28	AG32		
		NC *(6)*					W24	AE29		
		NC *(6)*					W25	AE30		
		NC *(6)*					AD24	AH26		
		NC *(6)*					AE23	AF24		
		NC *(6)*					AF24	AH24		
		NC *(6)*					AE24	AG24		
		NC *(6)*					AF23	AH25		
		NC *(6)*					AG24	AF23		
		NC *(6)*					AH24	AP33		
		NC *(6)*					AH23	AN33		
		NC *(6)*					AH20	AP32		
		NC *(6)*					AH21	AP30		
		NC *(6)*					AH22	AP31		
		NC *(6)*					AG22	AN31		
		NC *(6)*					Y19	AE24		
		NC *(6)*					AA18	AE23		
		NC *(6)*					Y18	AD22		
		NC *(6)*					Y17	AC22		
		NC *(6)*					AB11	AC12		
		NC *(6)*					AC10	AD12		
		NC *(6)*					Y10	AE12		
		NC *(6)*					Y11	AD13		
		NC *(6)*					AG4	AN4		
		NC *(6)*					AH3	AP4		
		NC *(6)*					AH4	AP2		
		NC *(6)*					AH5	AP5		
		NC *(6)*					AG3	AN3		
		NC *(6)*					AH2	AP3		
		NC *(6)*					AD9	AM6		
		NC *(6)*					AC9	AN6		
		NC *(6)*					AA9	AL5		
		NC *(6)*					AB9	AM5		
		NC *(6)*					Y9	AL4		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		NC *(6)*					AA10	AM4		
		NC *(6)*					W5	AD6		
		NC *(6)*					W6	AD7		
		NC *(6)*					Y1	AJ1		
		NC *(6)*					W2	AH2		
		NC *(6)*					V6	AC7		
		NC *(6)*					V7	AB8		
		NC *(6)*					W3	AF3		
		NC *(6)*					W4	AF4		
		NC *(6)*					H2	F1		
		NC *(6)*					J1	G1		
		NC *(6)*					K7	N9		
		NC *(6)*					K6	N8		
		NC *(6)*					G2	H4		
		NC *(6)*					H1	H3		
		NC *(6)*					K5	K6		
		NC *(6)*					K4	K5		
		NC *(6)*					D6	J11		
		NC *(6)*					E5	G9		
		NC *(6)*					C5	G11		
		NC *(6)*					D5	H11		
		NC *(6)*					B5	J12		
		NC *(6)*					C6	G10		
		NC *(6)*					A5	A2		
		NC *(6)*					A6	B2		
		NC *(6)*					A8	A5		
		NC *(6)*					A9	A3		
		NC *(6)*					A7	A4		
		NC *(6)*					B7	B4		
		NC *(6)*					H11	M13		
		NC *(6)*					J10	L13		
		NC *(6)*					J11	K11		
		NC *(6)*					J12	K12		
		NC *(6)*					G18	M23		
		NC *(6)*					F19	L23		
		NC *(6)*					J18	L22		
		NC *(6)*					J19	K23		
		NC *(6)*					B25	B31		
		NC *(6)*					A26	A31		
		NC *(6)*					A24	A30		
		NC *(6)*					A25	A33		
		NC *(6)*					B26	B32		
		NC *(6)*					A27	A32		
		NC *(6)*					F20	C29		
		NC *(6)*					E20	B29		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	WF780	H1152 for Stratix III only	DQ Group for DQS X4 Mode (2)	DQ Group for DQS X8/X9 Mode *(2)*
		NC *(6)*					H20	D30		
		NC *(6)*					G20	C30		
		NC *(6)*					H19	C31		
		NC *(6)*					J20	D31		

Notes:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix ® III device pin table for details.

(2) The individual index number of the pin in this column may not be the same as its companion Stratix III device, but the functionality of the pin is fully migratable.

(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix III device and should be connected on the board to configure the FPGA prototype.

(4) This NC pin is a VCCBAT pin in the Stratix III device and should be connected for the FPGA prototype.

(5) This NC pin is a VCCPT pin in the Stratix III device and should be connected for the FPGA prototype.

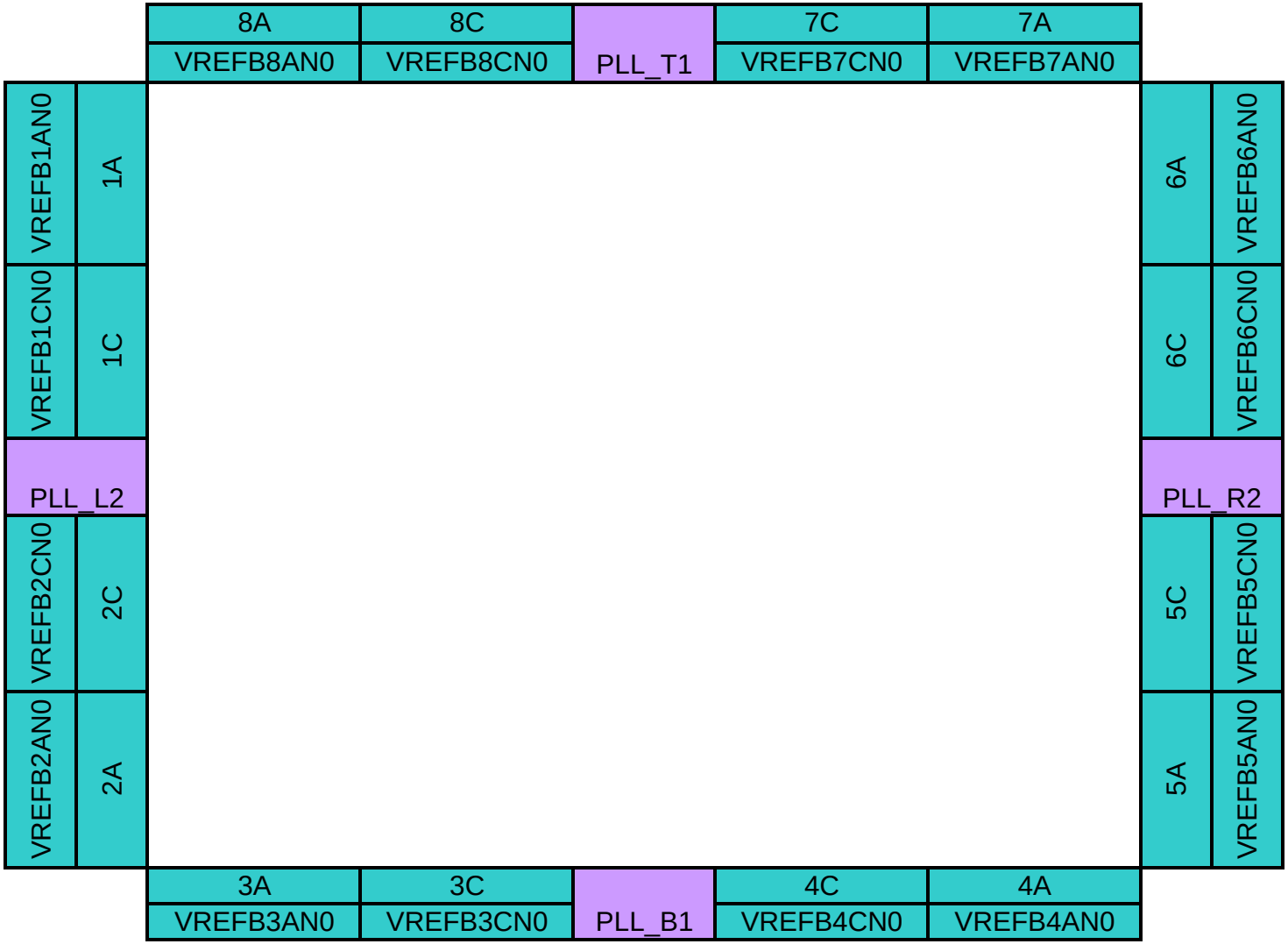
(6) This NC pin is an IO pin in the Stratix III device and can be left unconnected.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCL	Power	VCCL supplies power to the core voltage power supply pins.
VCC	Power	VCC supplies power to the periphery circuitry.
RUP[1..8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1..8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
VCCIO[1..8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0-V PCI/PCI-X I/O, and 3.0 V LVTTL I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), 3.0-V PCI/PCI-X and 3.0 V LVTTL I/O standards.
VREF[1..8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, these pins are used as the voltage-referenced pins for the bank.
VCCA_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Analog power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must power up these pins even if the PLL is not used. You are advised to keep this pin isolated from other VCC for better jitter performance.
VCCD_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Digital power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must power up these pins even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCPGM	Power	Power supply for configuration pins. Can be connected to 1.8 V, 2.5 V or 3.0 V depending on the particular design.
VCCPD[1..8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.0 V or 2.5 V. VCCPD for 3.0-V I/O standard is 3.0 V, and VCCPD for 2.5-V/1.8-V/1.2-V I/O standards is 2.5 V.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high (0.9 V) turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the HardCopy III device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the HardCopy III device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy III to enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy III drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V,3.0 V) selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin. Connect TCK to GND if the JTAG circuitry is not used.
TMS	Input	Dedicated JTAG input pin. Connect TMS to VCCPD if the JTAG circuitry is not used.
TDI	Input	Dedicated JTAG input pin. Connect TDI to VCCPD if the JTAG circuitry is not used.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,4,5,6,7,9,11..15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[0,2,4,5,6,7,9,11..15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for dfferential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L2,L3,R2,R3]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single-ended I/O or one differential I/O pair. When using both pins as single-ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L2,L3,R2,R3]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual-purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock ouput pins.
PLL_[T1,T2,B1,B2]_CLKOUT0[p,n]	I/O, Clock	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.
	Optional/Dual-Purpose Configuration Pins	
nCSO	Output	Dedicated control signal from Stratix III devices, but kept in HardCopy III for compatibility reasons.
ASDO	Output	Dedicated control signal from Stratix III devices, but kept in HardCopy III for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix III devices, but kept in HardCopy III for compatibility reasons. It's not required to clock this pin for HardCopy III.
	Differential I/O Pins	
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers.Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
	External Memory Interface Pins	
DQS[1..44][T,B], DQS[1..40][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1..44][T,B], DQSn[1..40][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry.
DQ[1..44][T,B],DQ[1..40][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1..44][T,B], CQ[1..40][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1..44][T,B], CQn[1..40][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.

Note:

(1) These pin definitions are prepared based on the device with the largest density, HC335. Refer to the pin list for the availability of pins in each density.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	10/28/2009	Initial release.