Pin Name	144-Pin TQFP	208-Pin PQFP/RQFP	240-Pin PQFP/RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA
MSEL0 (2)	77	108	124	P1	D4	U4
MSEL1 (2)	76	107	123	R1	D3	V4
nSTATUS (2)	35	52	60	T16	D24	W19
nCONFIG (2)	74	105	121	N4	D2	T7
DCLK (2)	107	155	179	B2	AC5	E5
CONF_DONE (2)	2	2	2	C15	AC24	F18
INIT_DONE (3)	14	19	26	G16	T24	K19
nCE (2)	106	154	178	B1	AC2	E4
nCEO (2)	3	3	3	B16	AC22	E19
nWS (4)	142	206	238	B14	AE24	E17
nRS (4)	141	204	236	C14	AE23	F17
nCS (4)	144	208	240	A16	AD24	D19
CS (4)	143	207	239	A15	AD23	D18
RDYnBSY (4)	11	16	23	G14	U22	K17
CLKUSR (4)	7	10	11	D15	AA24	G18
DATA7 (4)	116	166	190	B5	AF4	E8
DATA6 (4)	114	164	188	D4	AD8	G7
DATA5 (4)	113	162	186	A4	AE5	D7
DATA4 (4)	112	161	185	B4	AD6	E7
DATA3 (4)	111	159	183	C3	AF2	F6
DATA2 (4)	110	158	182	A2	AD5	D5
DATA1 (4)	109	157	181	B3	AD4	E6
DATA0 (2), (5)	108	156	180	A1	AD3	D4
TDI (2)	105	153	177	C2	AC3	F5
TDO (2)	4	4	4	C16	AC23	F19
TCK (2)	1	1	1	B15	AD25	E18
TMS (2)	34	50	58	P15	D22	U18
TRST (2)	(6)	51	59	R16	D23	V19
Dedicated Inputs	54, 56, 124, 126	78, 80, 182, 184	90, 92, 210, 212	B9, E8, M9, R8	A13, B14, AF14, AE13,	E12, H11, R12, V11
Dedicated Clock Pins	55, 125	79, 183	91, 211	A9, L8	A14, AF13	D12, P11
DEV_CLRn (3)	122	180	209	D8	AD13	G11
DEV_OE (3)	128	186	213	C9	AE14	F12
VCCINT	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L9, L12, M11, R2	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12
VCCIO	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	(16)	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13

Pin Name	144-Pin TQFP	208-Pin PQFP/RQFP	240-Pin PQFP/RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA
GNDINT	16, 57, 58, 84, 103, 127	21, 33, 49, 81, 82, 123, 129, 151, 185	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K7,K10, L6, L11, M5, M12, T8	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16
GNDIO	15, 40, 50, 66, 85, 104, 129, 139	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–	–	–	–
No Connect (N.C.) (7)	–	–	–	–	C1, D1, D26, E1, E2, G1, G5, G23, G26, H1, H25, H26, J25, K25, P24, R24, T23, U25, V1, V3, V4, V26, W2, W3, Y1, Y2, Y23, AC26 (9)	A2, A3, A4, A5, A7, A9, A11, A12, A14, A15, A20, A21, B3, B4, B9, B10, B12, B16, B19, B20, C1, C6, C9, C10, C12, C13, C14, C16, C17, C22, D1, D2, D3, D20, D21, E2, E3, E20, E22, F1, F2, F3, F20, F21, G2, G20, G22, H3, J1, J2, J3, J21, J22, K2, K22, L1, L2, L3, L20, L21, L22, M2, M3, M21, M22, N1, N2, N21, N22, P2, P3, P20, P21, P22, R2, R3, R20, R21, T2, T20, T21, U1, U2, U3, U20, U21, U22, V2, V20, W1, W2, W22, Y4, Y9, Y12, Y13, Y16, Y19, Y20, AA2, AA3, AA4, AA9, AA11, AA13, AA15, AA21, AB1, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB12, AB15, AB17, AB18, AB19, AB20, AB21, AB22 (9)
Total User I/O Pins (8)	102	147	189	191	246	246

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.