

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	672-Pin FineLine BGA	484-Pin Fineline BGA
B2	1	SD_A12	H8	D19
B2	2	VCCIO	VCCIO2	VCCIO2
-	3	GND_IO	GND	GND
B2	4	SD_A13	J8	C19
B2	5	SD_A14	F6	E18
B2	6	SD_DQ0	J13	B20
B2	7	VCCIO	VCCIO2	VCCIO2
-	8	GND_IO	GND	GND
B2	9	SD_DQ1	H13	C20
B2	10	SD_DQ2	F13	F18
B2	11	SD_DQ3	G13	C21
B2	12	VCCIO	VCCIO2	VCCIO2
-	13	GND_IO	GND	GND
B2	14	SD_DQ4	E13	E20
B2	15	SD_DQ5	D13	F19
B2	16	DDR_VS0	D12	D21
B2	17	VCCIO	VCCIO2	VCCIO2
-	18	GND_IO	GND	GND
B2	19	SD_DQ6	C13	F20
B2	20	SD_DQ7	B12	G18
B2	21	SD_DQS0	F12	D22
B2	22	VCCIO	VCCIO2	VCCIO2
-	23	GND_IO	GND	GND
B2	24	SD_DQM0	H12	E21
B2	25	SD_DQ8	E12	H19
B2	26	SD_DQ9	G12	G20
B2	27	VCCIO	VCCIO2	VCCIO2
-	28	GND_IO	GND	GND
B2	29	SD_DQ10	J12	E22
B2	30	SD_DQ11	A12	H18
B2	31	SD_DQ12	C12	G21
B2	32	VCCIO	VCCIO2	VCCIO2
-	33	GND_IO	GND	GND
B2	34	SD_DQ13	B11	H20
B2	35	SD_DQ14	K13	H17
B2	36	DDR_VS1	E11	G22
B2	37	VCCIO	VCCIO2	VCCIO2
-	38	GND_IO	GND	GND
B2	39	SD_DQ15	A11	H22
B2	40	SD_DQS1	H11	J17
B2	41	SD_DQM1	G11	J20
-	42	VCC_INT	VCC_INT	VCC_INT
-	43	GND_INT	GND	GND
B2	44	VCCIO	VCCIO2	VCCIO2
-	45	GND_IO	GND	GND
B2	46	SD_DQ16	A9	-
B2	47	SD_DQ17	H10	-
B2	48	SD_DQ18	B9	-
B2	49	SD_DQ19	C9	-
B8	50	VCCIO	VCCIO8	VCCIO8

B13	51	I/O	E4	K19
B13	52	I/O	E3	K17
B13	53	I/O	H5	K18
B13	54	VCCIO	VCCIO13	VCCIO13
-	55	VCC_INT	VCC_INT	VCC_INT
B13	56	I/O	F4	K15
B13	57	I/O	G3	L19
B13	58	I/O	J5	L15
B13	59	I/O	G4	K20
B13	60	I/O	H4	L16
B13	61	I/O	H3	K21
B13	62	VCCIO	VCCIO13	VCCIO13
B13	63	I/O	F3	L20
B13	64	I/O	J4	L17
B13	65	I/O	J3	L21
B13	66	I/O	K4	L18
B13	67	I/O, DATA6 (1)	V3	L22
-	68	GND_INT	GND	GND
B13	69	I/O	L5	M19
B13	70	I/O	K3	M16
B13	71	I/O	K5	M20
B13	72	I/O	L4	M17
B13	73	I/O, DATA7 (1)	T7	M18
-	74	GND_INT	GND	GND
B13	75	I/O, nWS (1)	Y3	M21
B13	76	I/O	L3	N16
B13	77	I/O	R5	M22
B13	78	I/O, nRS (1)	T6	P16
B13	79	I/O, nCS (1)	Y4	N20
-	80	VCC_INT	VCC_INT	VCC_INT
-	81	VCC_CK4 (2)	R9	N17
-	82	GND_CK4 (2)	R8	N19
-	83	GND_CK4 (2)	R8	N18
B13	84	I/O	R6	P20
B13	85	I/O, CS (1)	V7	P17
B13	86	I/O, DEV_CLRn (3)	V5	R20
B13	87	VCCIO	VCCIO13	VCCIO13
B13	88	I/O	M5	N22
-	89	CLKLK_FB2p	N5	N21
B13	90	I/O	W5	P22
-	91	CLK4p	Y5	P21
B13	92	I/O	Y6	R22
-	93	DATA0 (5), (6)	W7	P18
-	94	DCLK (5)	R7	R16
-	95	CLK2P	W6	R21
-	96	nCE (5)	P6	P19
-	97	TDI (5)	P5	T20
B12	98	VCCIO	VCCIO12	VCCIO12
-	99	GND_CK2 (2)	T9	R17
-	100	GND_CK2 (2)	T9	R19
-	101	GND_INT	GND	GND
-	102	VCC_CK2 (2)	T8	R18
B12	103	I/O, DEV_OE (3)	AA3	U16

-	104	VCC_CKOUT2 (7)	U8	T19
-	105	GND_CKOUT2 (7)	V8	T17
B12	106	I/O	K2	W22
B12	107	I/O	L2	V16
-	108	GND_IO	GND	GND
-	109	CLKLK_OUT2p (8)	M4	U22
B12	110	I/O	M3	U21
B12	111	I/O, LOCK2 (9)	AB3	U17
B12	112	I/O	M1	U20
B12	113	I/O	M2	T18
-	114	VCC_INT	VCC_INT	VCC_INT
B12	115	I/O, LOCK4 (9)	AB4	Y22
B12	116	I/O	T2	U19
B12	117	I/O	R1	W21
B12	118	I/O	R2	V17
B12	119	I/O	L1	V20
B12	120	VCCIO	VCCIO12	VCCIO12
B12	121	I/O	U1	Y21
B12	122	I/O	U2	U18
B12	123	I/O	T1	W20
B12	124	I/O	V1	V18
B12	125	I/O	V2	Y20
-	126	GND_INT	GND	GND
B12	127	I/O	W1	AB19
B12	128	I/O	W2	Y17
B12	129	I/O	Y1	AA20
B12	130	I/O	Y2	W17
B12	131	I/O	AA1	V19
-	132	GND_IO	GND	GND
-	133	VCC_INT	VCC_INT	VCC_INT
B12	134	I/O	AA2	AA19
B12	135	I/O	AB1	Y19
B12	136	I/O	AC2	W18
B12	137	I/O	AB2	Y18
B12	138	VCCIO	VCCIO12	VCCIO12
-	139	GND_IO	GND	GND
B11	140	VCCIO	VCCIO11	VCCIO11
B11	141	I/O	AB8	Y16
B11	142	I/O	AC8	W16
B11	143	I/O	AD7	AA17
B11	144	I/O	AE7	T15
B11	145	I/O	AD8	AB17
B11	146	I/O	AC9	U15
B11	147	I/O	AE9	V15
B11	148	I/O	AA10	AA16
B11	149	I/O	AD9	W15
B11	150	I/O	AB9	Y15
-	151	GND_IO	GND	GND
B11	152	I/O	AC10	T14
B11	153	I/O	AF9	AB16
B11	154	I/O	AB10	U14
B11	155	I/O	AE10	AA15
B11	156	I/O	AA11	V14

B11	157	I/O	AF10	Y14
B11	158	I/O	AD10	R13
B11	159	I/O	AB11	W14
B11	160	I/O	AC11	T13
B11	161	I/O	AD11	AB15
B11	162	VCCIO	VCCIO11	VCCIO11
B11	163	I/O	AF11	AA14
B11	164	I/O	AA12	U13
B11	165	I/O	AB12	Y13
B11	166	I/O	AE11	V13
B11	167	I/O	AC12	W13
B11	168	I/O	AD12	T12
B11	169	VCCIO	VCCIO11	VCCIO11
B11	170	I/O	AC13	AB14
B11	171	I/O	AB14	AA12
B11	172	I/O	AA13	U12
B11	173	I/O	AB13	Y12
-	174	CONF_DONE (5)	AD13	V12
-	175	NSTATUS (5)	AE12	AB12
B10	176	FAST4	AF12	W12
-	177	GND_IO	GND	GND
B10	178	VCCIO	VCCIO10	VCCIO10
-	179	GND_INT	GND	GND
-	180	GND_INT	GND	GND
-	181	VCC_INT	VCC_INT	VCC_INT
-	182	VCC_INT	VCC_INT	VCC_INT
-	183	GND_INT	GND	GND
-	184	GND_INT	GND	GND
-	185	GND_IO	GND	GND
B10	186	FAST3	AF15	V11
-	187	TCK (5)	AD14	Y11
-	188	TMS (5)	AE15	U11
B10	189	I/O	AA14	W11
B10	190	I/O	W14	T11
B10	191	I/O	W15	AB10
B10	192	I/O	Y15	V10
B10	193	I/O	AC14	AA10
B10	194	I/O	V15	W10
B10	195	I/O	AD15	Y10
B10	196	I/O	AC15	U10
B10	197	I/O	AB15	AB9
B10	198	I/O	AA15	T10
B10	199	VCCIO	VCCIO10	VCCIO10
B10	200	I/O	AF16	AA9
B10	201	I/O	AE16	R10
B10	202	I/O	AD16	Y9
B10	203	I/O	AB16	W9
B10	204	I/O	AC16	AB8
B10	205	I/O	AA16	V9
B10	206	I/O	V16	AA8
B10	207	I/O	W16	AB6
B10	208	I/O	Y16	U9
B10	209	I/O	AF17	Y8

-	210	GND_IO	GND	GND
B10	211	VCCIO	VCCIO10	VCCIO10
B10	212	I/O	AE17	AA7
B10	213	I/O	AD17	W8
B10	214	I/O	AC17	AB5
B10	215	I/O	W17	V8
B10	216	I/O	AB17	AA6
B10	217	I/O	AA17	AA5
B10	218	I/O	Y17	V7
B10	219	I/O	AF18	Y7
B10	220	I/O	AE18	W7
B10	221	I/O	AB18	Y6
B10	222	VCCIO	VCCIO10	VCCIO10
-	223	GND_IO	GND	GND
B10	224	VCCIO	VCCIO10	VCCIO10
B10	225	I/O	Y18	V5
B10	226	I/O	AD18	V4
B10	227	I/O	AD19	V6
B10	228	I/O	AC20	W5
-	229	GND_INT	GND	GND
-	230	GND_IO	GND	GND
B10	231	I/O	AD20	Y5
B10	232	I/O	AC19	U6
B10	233	I/O	AC18	Y4
B10	234	I/O	AE22	U7
B10	235	I/O	W18	AA4
-	236	VCC_INT	VCC_INT	VCC_INT
B10	237	I/O	AA18	AB4
B10	238	I/O	AE23	U8
B10	239	I/O	AD21	AA3
B10	240	I/O	AE20	T9
B10	241	I/O	AF20	Y3
B10	242	VCCIO	VCCIO10	VCCIO10
B10	243	I/O	AC21	Y2
B9	244	I/O	AB20	U4
B9	245	I/O	AB19	W3
B9	246	I/O	Y20	T5
B9	247	I/O	AD22	T4
-	248	GND_INT	GND	GND
B9	249	I/O	AA19	V3
B9	250	I/O	AB22	T6
B9	251	I/O	AC22	W2
B9	252	I/O	AA20	T7
B9	253	I/O	Y19	U3
-	254	GND_IO	GND	GND
B9	255	I/O	AA21	W1
B9	256	I/O	AB21	T8
B9	257	I/O	R22	V2
-	258	CLK3p	R23	V1
B9	259	I/O	N20	U2
-	260	VCC_INT	VCC_INT	VCC_INT
-	261	NCONFIG (5)	M20	R4
-	262	CLKLK_ENA (5) (10)	R21	R6

-	263	CLK1p	P20	U1
-	264	MSEL1 (5)	N21	T3
-	265	MSEL0 (5)	N22	R5
B9	266	I/O	V19	R3
B9	267	I/O	W21	P5
B9	268	I/O	AB23	P4
B9	269	I/O	Y21	R7
B9	270	I/O	W20	R2
B9	271	VCCIO	VCCIO9	VCCIO9
B9	272	I/O	Y22	P3
B9	273	I/O	AA22	P6
B9	274	I/O	V20	R1
B9	275	I/O	Y23	P7
B9	276	I/O	AB24	P2
-	277	GND_INT	GND	GND
B9	278	I/O	AA23	P1
B9	279	I/O	AA24	N5
B9	280	I/O	V21	N4
B9	281	I/O	AC25	N6
B9	282	I/O	AC26	N3
-	283	GND_IO	GND	GND
B9	284	I/O	Y24	N2
B9	285	I/O	U20	N7
B9	286	I/O	W22	N1
B9	287	I/O	T20	M5
B9	288	I/O	V22	M4
-	289	VCC_INT	VCC_INT	VCC_INT
B9	290	VCCIO	VCCIO9	VCCIO9
B9	291	I/O	W24	M3
B9	292	I/O	U21	M6
B9	293	I/O	W23	L1
B9	294	I/O	V23	M7
B9	295	I/O	U22	L2
B9	296	VCCIO	VCCIO9	VCCIO9
B9	297	I/O	T21	L3
B3	298	I/O, DATA5 (1)	A18	L6
B3	299	I/O, DATA4 (1)	A20	L4
B3	300	I/O, DATA3 (1)	B22	L5
B3	301	I/O, DATA2 (1)	B18	J1
-	302	GND_INT	GND	GND
B3	303	I/O, DATA1 (1)	B20	K3
B3	304	I/O, CLKUSR (1)	B23	L7
B3	305	I/O, RDYnBSY (1)	A22	K4
B3	306	I/O, INIT_DONE (3)	A23	K7
B3	307	VCCIO	VCCIO3	VCCIO3
-	308	GND_IO	GND	GND
B3	309	VCCIO	VCCIO3	VCCIO3
-	310	BOOT_FLASH	C16	J5
B3	311	FAST2	A15	K5
B3	312	FAST1	A16	J2
-	313	DEBUG_EN	D14	K6
-	314	GND	C15	J3
-	315	TDO (5)	B15	J4

-	316	GND_INT	GND	GND
-	317	GND_INT	GND	GND
-	318	VCC_INT	VCC_INT	VCC_INT
-	319	GND_INT	GND	GND
-	320	nCEO (5)	D15	H3
-	321	TRST(5)	D16	J6
-	322	NRESET	B16	H4
-	323	JSELECT	C14	H5
B7	324	VCCIO	VCCIO7	VCCIO7
-	325	GND_IO	GND	GND
-	326	NPOR	J24	H1
-	327	CLK_REF	H24	H7
-	328	EN_SELECT(13)	J23	H2
-	329	PROC_TMS	E24	H6
-	330	PROC_TDO	G23	G2
-	331	PROC_TDI	H23	G7
-	332	PROC_TCK	F24	G3
-	333	PROC_TRST	G24	G6
B7	334	VCCIO	VCCIO7	VCCIO7
-	335	GND_IO	GND	GND
B7	336	UART_CTS_N	G22	F1
B7	337	UART_DSR_N	H22	G4
B7	338	UART_RXD	F21	F2
B7	339	UART_DCD_N	J22	F6
B7	340	UART_RI_N	J21	F3
B7	341	UART_TXD	G21	G5
B7	342	UART_RTS_N	H21	E2
B7	343	UART_DTR_N	J20	E6
B6	344	EBI_BE0	D22	D1
B6	345	EBI_BE1	K18	H9
B6	346	EBI_OE_N	C22	D2
B6	347	EBI_WE_N	E21	G8
B6	348	EBI_CS0	K17	C2
B6	349	EBI_CS1	H20	B3
B6	350	EBI_CS2	J19	D3
B6	351	EBI_CS3	G20	C4
B6	352	EBI_CLK	D21	C3
B6	353	EBI_ACK	K16	B4
-	354	GND_CK6 (2)	F23	F4
-	355	GND_CK6 (2)	F23	F5
-	356	VCC_CK6 (2)	E23	E4
-	357	GND_CK5 (2)	F22	D6
-	358	GND_CK5 (2)	F22	D5
-	359	VCC_CK5 (2)	E22	E5
B6	360	VCCIO	VCCIO6	VCCIO6
-	361	GND_IO	GND	GND
B6	362	INT_EXT_PIN_N	H19	B5
B6	363	EBI_A0	F20	C5
B6	364	EBI_A1	C21	A4
B6	365	EBI_A2	E20	D7
B6	366	EBI_A3	H18	A5
-	367	GND_INT	GND	GND
-	368	VCC_INT	VCC_INT	VCC_INT

B6	369	EBI_A4	G19	E7
B6	370	EBI_A5	J18	B6
B6	371	EBI_A6	J17	C7
B6	372	EBI_A7	G18	A6
B6	373	EBI_A8	D20	F8
B6	374	EBI_A9	F19	B7
B6	375	VCCIO	VCCIO6	VCCIO6
-	376	GND_IO	GND	GND
B6	377	EBI_A10	H17	D8
B6	378	EBI_A11	E19	C8
B6	379	EBI_A12	C20	E8
B6	380	EBI_A13	D19	A7
B6	381	EBI_A14	F18	G9
-	382	GND_INT	GND	GND
-	383	VCC_INT	VCC_INT	VCC_INT
B6	384	EBI_A15	C19	B8
B6	385	EBI_A16	G17	F9
B6	386	EBI_A17	K15	A8
B6	387	EBI_A18	D18	E9
B6	388	EBI_A19	E18	C9
B6	389	VCCIO	VCCIO6	VCCIO6
-	390	GND_IO	GND	GND
B6	391	EBI_A20	H16	D9
B6	392	EBI_A21	F17	B9
B6	393	EBI_A22	C18	H10
B6	394	EBI_A23	J16	A9
B6	395	EBI_A24	E17	G10
B6	396	EBI_DQ0	C17	D10
-	397	GND_INT	GND	GND
-	398	VCC_INT	VCC_INT	VCC_INT
B6	399	EBI_DQ1	G16	F10
B6	400	EBI_DQ2	D17	C10
B6	401	EBI_DQ3	E16	E10
B6	402	EBI_DQ4	J15	A10
B6	403	EBI_DQ5	F16	G11
B6	404	VCCIO	VCCIO6	VCCIO6
-	405	GND_IO	GND	GND
B6	406	EBI_DQ6	G15	B10
B6	407	EBI_DQ7	F15	F11
B6	408	EBI_DQ8	H15	D11
B6	409	EBI_DQ9	E15	E11
B6	410	EBI_DQ10	J14	C11
-	411	GND_INT	GND	GND
-	412	VCC_INT	VCC_INT	VCC_INT
B6	413	EBI_DQ11	E14	B11
B6	414	EBI_DQ12	K14	F12
B6	415	EBI_DQ13	G14	A12
B6	416	EBI_DQ14	F14	E12
B6	417	EBI_DQ15	H14	B12
B2	418	VCCIO	VCCIO2	VCCIO2
-	419	GND_IO	GND	GND
B2	420	SD_DQM_ECC(12)	D10	B13
B2	421	SD_DQS_ECC(12)	F10	G13



B2	422	SD_DQ_ECC0(12)	G10	D13
B2	423	VCCIO	VCCIO2	VCCIO2
-	424	GND_IO	GND	GND
-	425	GND_INT	GND	GND
-	426	VCC_INT	VCC_INT	VCC_INT
B2	427	SD_DQ_ECC1(12)	J11	A15
B2	428	SD_DQ_ECC2(12)	C10	F13
B2	429	SD_DQ_ECC3(12)	C11	C13
B2	430	VCCIO	VCCIO2	VCCIO2
-	431	GND_IO	GND	GND
B2	432	SD_DQ_ECC4(12)	E10	E13
B2	433	SD_DQ_ECC5(12)	D11	D14
B2	434	DDR_VS2	C8	B15
B2	435	VCCIO	VCCIO2	VCCIO2
-	436	GND_IO	GND	GND
B2	437	SD_WE_N	A5	F14
B2	438	SD_CAS_N	F8	A17
-	439	GND_INT	GND	GND
-	440	VCC_INT	VCC_INT	VCC_INT
B2	441	SD_RAS_N	J9	C14
B2	442	VCCIO	VCCIO2	VCCIO2
-	443	GND_IO	GND	GND
B2	444	SD_CS_N0	E7	G15
B2	445	SD_CS_N1	D6	B16
B2	446	SD_CLK_N	G7	J16
B2	447	VCCIO	VCCIO2	VCCIO2
-	448	GND_IO	GND	GND
B2	449	SD_CLK	B5	C15
B2	450	SD_CLKE	F7	E15
B2	451	SD_A0	K9	B17
B2	452	VCCIO	VCCIO2	VCCIO2
-	453	GND_INT	GND	GND
-	454	VCC_INT	VCC_INT	VCC_INT
-	455	GND_IO	GND	GND
B2	456	SD_A1	C5	G16
B2	457	SD_A2	E6	D16
B2	458	SD_A3	G6	F16
B2	459	VCCIO	VCCIO2	VCCIO2
-	460	GND_IO	GND	GND
B2	461	SD_A4	K8	A19
B2	462	SD_A5	A4	E16
B2	463	SD_A6	B4	B18
B2	464	VCCIO	VCCIO2	VCCIO2
-	465	GND_IO	GND	GND
B2	466	SD_A7	F5	F17
-	467	GND_INT	GND	GND
-	468	VCC_INT	VCC_INT	VCC_INT
B2	469	SD_A8	D5	C17
B2	470	SD_A9	G5	D17
B2	471	VCCIO	VCCIO2	VCCIO2
-	472	GND_IO	GND	GND
B2	473	SD_A10	K11	B19
B2	474	SD_A11	E5	D18

B9	475	I/O	U23	-
B9	476	I/O	R20	-
B9	477	I/O	T22	-
B9	478	I/O	U24	-
B9	479	I/O	T24	-
B9	480	I/O	V24	-
B8	481	I/O	M26	-
B8	482	I/O	L21	-
B8	483	I/O	M22	-
B8	484	I/O	M25	-
B8	485	VCCIO	VCCIO8	VCCIO8
B8	486	I/O	M24	-
B8	487	I/O	M21	-
B8	488	I/O	L20	-
B8	489	I/O	M19	-
B8	490	VCCIO	VCCIO8	VCCIO8
B8	491	I/O	L19	-
B8	492	I/O	N25	-
B8	493	I/O	M23	-
B8	494	I/O	K26	-
B8	495	I/O	N23	-
B8	496	I/O	L26	-
-	497	GND_IO	GND	GND
B8	498	I/O	L25	-
B8	499	I/O	R26	-
B8	500	I/O	K24	-
B8	501	I/O	R25	-
B8	502	I/O	L24	-
B8	503	I/O	K22	-
B8	504	VCCIO	VCCIO8	VCCIO8
B8	505	I/O	L23	-
B8	506	I/O	T25	-
B8	507	I/O	U26	-
B8	508	I/O	J26	-
-	509	GND_INT	GND	GND
-	510	VCC_INT	VCC_INT	VCC_INT
-	511	VCC_INT	VCC_INT	VCC_INT
-	512	GND_INT	GND	GND
B8	513	VCCIO	VCCIO8	VCCIO8
B8	514	I/O	U25	-
B8	515	I/O	P21	-
B8	516	I/O	J25	-
B8	517	I/O	L22	-
B8	518	I/O	K19	-
B8	519	I/O	W26	-
B8	520	I/O	K25	-
B8	521	I/O	R24	-
B8	522	I/O	H26	-
B8	523	I/O	H25	-
-	524	GND_IO	GND	GND
B8	525	VCCIO	VCCIO8	VCCIO8
B8	526	I/O	G25	-
B8	527	I/O	V26	-

B8	528	I/O	K21	-
B8	529	I/O	AA26	-
B8	530	I/O	F26	-
B8	531	I/O	K20	-
B8	532	I/O	V25	-
B8	533	I/O	F25	-
B8	534	I/O	T26	-
B8	535	I/O	E26	-
B8	536	VCCIO	VCCIO8	VCCIO8
B8	537	I/O	G26	-
B8	538	I/O	Y25	-
B8	539	I/O	E25	-
B8	540	I/O	W25	-
B8	541	I/O	AA25	-
B8	542	I/O	D26	-
B8	543	I/O	Y26	-
B8	544	I/O	AB25	-
B8	545	I/O	D25	-
B8	546	I/O	AB26	-
-	547	GND_IO	GND	GND
B2	549	SD_DQ_ECC6(12)	F11	-
B2	550	SD_DQM3	C6	-
B2	551	SD_DQS3	K10	-
B2	552	SD_DQ31	D7	-
B2	553	SD_DQ30	C7	-
B2	554	SD_DQ29	G8	-
B2	555	SD_DQ28	E8	-
B2	556	SD_DQ27	B7	-
B2	557	SD_DQ26	A7	-
B2	558	SD_DQ25	H9	-
B2	559	SD_DQ24	D8	-
B2	560	SD_DQM2	F9	-
B2	561	SD_DQS2	J10	-
B2	562	SD_DQ23	G9	-
B2	563	SD_DQ22	D9	-
B2	564	SD_DQ21	K12	-
B2	565	SD_DQ20	E9	-

Pin Name	672-Pin FineLine BGA	484-Pin FineLine BGA
MSEL0 (5)	N22	R5
MSEL1 (5)	N21	T3
NSTATUS (5)	AE12	AB12
NCONFIG (5)	M20	R4
DCLK (5)	R7	R16
CONF_DONE (5)	AD13	V12
INIT_DONE (3)	A23	K7
nCE (5)	P6	P19
nCEO (5)	D15	H3
nWS (1)	Y3	M21
nRS (1)	T6	P16
nCS (1)	Y4	N20
CS (1)	V7	P17
RDYnBSY (1)	A22	K4
CLKUSR (1)	B23	L7
DATA7 (1)	T7	M18
DATA6 (1)	V3	L22
DATA5 (1)	A18	L6
DATA4 (1)	A20	L4
DATA3 (1)	B22	L5
DATA2 (1)	B18	J1
DATA1 (1)	B20	K3
DATA0 (5), (6)	W7	P18
TDI (5)	P5	T20
TDO (5)	B15	J4
TCK (5)	AD14	Y11
TMS (5)	AE15	U11
TRST (5)	D16	J6
Dedicated Fast I/Os	A16,A15,AF15,AF12	J2,K5,V11,W12
CLK1p	P20	U1
CLK2p	W6	R21
CLK3p	R23	V1
CLK4p	Y5	P21
LOCK2 (9)	AB3	U17
LOCK4 (9)	AB4	Y22
CLKLK_ENA (5) (10)	R21	R6
CLKLK_OUT2p (8)	M4	U22
CLKLK_FB2p	N5	N21
DEV_CLRn (3)	V5	R20
DEV_OE (3)	AA3	U16
CLK_REF	H24	H7
NRESET	B16	H4
NPOR	J24	H1
BOOT_FLASH	C16	J5
DEBUG_EN	D14	K6
JSELECT	C14	H5
PROC_TDI	H23	G7
PROC_TD0	G23	G2
PROC_TCK	F24	G3
PROC_TMS	E24	H6
PROC_TRST	G24	G6
EN_SELECT	J23	H2
VCCINT	B17, B19, B24, C1, C2, C4, C23, C25, C26, D3, D24, L13, L15, M13, M16, N2, N10, N12, P15, P18, P24, P25, R10, R11, R14, T12, T17, U9, U14, U16, AC3, AC24, AD1, AD2, AD4, AD23, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24, A24, A3, B10, B3, B8	H12, H15, H8, J11, J13, J9, K10, K12, K14, L11, L13, L9, M10, M12, M14, N11, N13, N9, P10, P12, P14, P8, R15, R9
VCCIO2	B14, P11, U15	A14, A18, A20, C18, C22, D12, D15, E14, E19, F15, F22, G12, G17, G19, H13, H14, H21, J15, J18, J22

VCCIO3	P17, R18, U13	K1, L8
VCCIO6	L14, L12, A6	A13, A3, C1, F7
VCCIO7	N17, M14, A13	G1, J7
VCCIO8	L17, N15, A21	-
VCCIO9	R16, U18, N24	M1, M8, T1
VCCIO10	T15, V17, AF21, AE14	AB11, AB3, AB7, R11, U5, Y1
VCCIO11	V10, U11, AF13, R13	AB13, AB18, R12
VCCIO12	T10, AF6	AB20, T16, V22
VCCIO13	N3, P12, M11	K22, M15, T22
VCC_CCLK2 (2)	T8	R18
VCC_CCLK4 (2)	R9	N17
VCC_CCLK5 (2)	E22	E5
VCC_CCLK6 (2)	E23	E4
VCC_CKOUT2 (7)	U8	T19
GND	A2, A8, A10, A14, A17, A19, A25, B1, B2, B6, B13, B21, B25, B26, C3, C24, D4, D23, L11, L16, M12, M15, M17, N1, N4, N11, N13, N14, N16, N18, N26, P1, P2, P3, P13, P14, P16, P23, P26, R12, R15, R17, T11, T13, T14, T16, T18, U10, U12, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD24, AE1, AE2, AE6, AE13, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25	J3, A1, A11, A16, A2, A21, A22, AA1, AA11, AA13, AA18, AA2, AA21, AA22, AB1, AB2, AB21, AB22, B1, B14, B2, B21, B22, C12, C16, C6, D20, D4, E1, E17, E3, F21, G14, H11, H16, J10, J12, J14, J19, J21, J8, K11, K13, K16, K2, K8, K9, L10, L12, L14, M11, M13, M2, M9, N10, N12, N14, N15, N8, P11, P13, P15, P9, R14, R8, T2, T21, V21, W19, W4, W6
GND_CCLK2 (2)	T9	R17, R19
GND_CCLK4 (2)	R8	N19, N18
GND_CCLK5 (2)	F22	D6, D5
GND_CCLK6 (2)	F23	F5, F4
GND_CKOUT2 (7)	V8	T17
No Connect (N.C.)	AA4, AC5, AF7, G2, K7, M8, P9, T23, V12, Y7, AA5, AC6, AF22, H1, K23, M9, P19, U3, V13, Y8, AA6, AC7, AF23, H2, L6, M18, P22, U4, V14, Y9, AA7, AD5, D1, H6, L7, N6, R3, U5, W3, Y10, AA8, AD6, D2, H7, L8, N7, R4, U6, W4, Y11, AA9, AE4, E1, J1, L9, N8, R19, U7, W9, Y12, AB5, AE5, E2, J2, L10, N9, T3, U19, W10, Y13, AB6, AF4, F1, J6, L18, N19, T4, V4, W11, Y14, AB7, AF5, F2, J7, M6, P4, T5, V6, W12, P8, AC1, K6, G1, K1, M7, P7, T19, V11, W13, M10, P10	-
Total User I/O Pins (11)	246	186

Notes:

- (1) This pin can be used as a user I/O pin after configuration.
- (2) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC\_CKCLK has the same voltage specifications as the VCCINT and should be connected to a 1.8 -V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
- (3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
- (4) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.
- (5) This pin is a dedicated pin; it is not available as a user I/O pin.
- (6) This pin is tri-stated in user mode.
- (7) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock output. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.
- (8) The CLKCLK\_OUT pin is powered by the VCC\_CKOUT and GND\_CKOUT pins.
- (9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
- (10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.
- (11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.
- (12) This pin is reserved for future functionality. It should be left unconnected.
- (13) This pin is reserved for future functionality. It should be connected to ground.

Copyright © 1995, 1996, 1997, 1998, 1999 Altera Corporation, 101 Innovation Drive,  
San Jose, CA 95134, USA, all rights reserved.

By accessing this information, you agree to be bound by the terms of Altera's  
Legal Notice.