



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
B1	VREFB1N0	IO	DIFFIO_L1p				H6				DQ2L0	DQ1L0	DQ1L0
B1	VREFB1N0	IO	DIFFIO_L1n		F4		G6	B8_B1					
B1	VREFB1N0	IO	DIFFIO_L2p		E4		F5				DQ2L1	DQ1L1	DQ1L1
B1	VREFB1N0	IO	DIFFIO_L2n		E3		F4				DQ2L2	DQ1L2	DQ1L2
B1	VREFB1N0	IO	VREFB1N0		F3		J5						
B1	VREFB1N0	IO	DIFFIO_L3p		B2		D3	B8_B1					
B1	VREFB1N0	IO	DIFFIO_L3n		B1		D2						
B1	VREFB1N0	IO	DIFFIO_L4p		C2		C1		DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0
B1	VREFB1N0	IO	DIFFIO_L4n		C1		D1				DQ2L3	DQ1L3	DQ1L3
B1	VREFB1N0	IO	DIFFIO_L5p		D2		G5				DQ2L4	DQ1L4	DQ1L4
B1	VREFB1N0	IO	DIFFIO_L5n	DATA1,ASDO	D1		G4						
B1	VREFB1N0	IO					E2				DQ2L5	DQ1L5	DQ1L5
B1	VREFB1N0	IO	DIFFIO_L6p				E4	B8_B1					
B1	VREFB1N0	IO	DIFFIO_L6n				E3				DQ2L6	DQ1L6	DQ1L6
B1	VREFB1N0	IO	DIFFIO_L7p				E1				DQ2L7	DQ1L7	DQ1L7
B1	VREFB1N1	IO	DIFFIO_L7n				F1						
B1	VREFB1N1	IO	DIFFIO_L8p	FLASH_nCE,nCSO	E2		K6						
B1	VREFB1N1	IO	DIFFIO_L8n		E1		K5					DQ1L8	DQ1L8
B1	VREFB1N1	IO	DIFFIO_L9p		J4	B1	G2			DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0	
B1	VREFB1N1	IO	DIFFIO_L9n		J3	B1	G1						
B1	VREFB1N1	IO			H4	B1	J4						
B1	VREFB1N1	IO	VREFB1N1		F2		J3						
B1	VREFB1N1	IO	DIFFIO_L10p				J7				DQ0L0	DQ1L9	DQ1L9
B1	VREFB1N1	IO	DIFFIO_L10n				J6				DQ0L1	DQ1L10	DQ1L10
B1	VREFB1N1	nSTATUS		nSTATUS	F1		M1						
B1	VREFB1N1	IO	DIFFIO_L11p				L5				DQ0L2	DQ1L11	DQ1L11
B1	VREFB1N1	IO	DIFFIO_L11n				L4				DQ0L3	DQ1L12	DQ1L12
B1	VREFB1N1	IO	DIFFIO_L12p		H3		G3		DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0
B1	VREFB1N1	IO	DIFFIO_L12n				H3				DQ0L4	DQ1L13	DQ1L13
B1	VREFB1N1	IO	DIFFIO_L13p		L2	B1_B2	K2	B1	DQ1L0	DQ1L0			
B1	VREFB1N1	IO	DIFFIO_L13n		L1	B1_B2	K3	B1	DQ1L1	DQ1L1			
B1	VREFB1N1	IO	DIFFIO_L14p				J2	B1			DQ0L5	DQ1L14	DQ1L14
B1	VREFB1N2	IO	DIFFIO_L14n				J1	B1					
B1	VREFB1N2	IO	DIFFIO_L15p				M6						
B1	VREFB1N2	IO	DIFFIO_L15n				N6	B1					
B1	VREFB1N2	IO					L1	B1					
B1	VREFB1N2	IO	VREFB1N2		J2		K4						
B1	VREFB1N2	IO	DIFFIO_L16p				H2				DQ0L6	DQ1L15	DQ1L15
B1	VREFB1N2	IO	DIFFIO_L16n				H1				DQ0L7	DQ1L16	DQ1L16
B1	VREFB1N2	IO	DIFFIO_L17p				M5					DQ1L17	DQ1L17
B1	VREFB1N2	IO	DIFFIO_L17n				M4				DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1
B1	VREFB1N2	IO	DIFFIO_L18p				P4	B1					



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B1	VREFB1N2	IO	DIFFIO_L18n				P3						
B1	VREFB1N2	IO					P1						
B1	VREFB1N2	DCLK		DCLK	G2		L6						
B1	VREFB1N2	IO		DATA0	H5		K1						
B1	VREFB1N2	nCONFIG		nCONFIG	G1		M3						
B1	VREFB1N2	TDI		TDI	K4		P5						
B1	VREFB1N2	TCK		TCK	H1		P2						
B1	VREFB1N2	TMS		TMS	H2		N3						
B1	VREFB1N2	TDO		TDO	K5		P6						
B1	VREFB1N2	nCE		nCE	J1		M2						
B1	VREFB1N2	CLK0	DIFFCLK_0p		K2		N2						
B1	VREFB1N2	CLK1	DIFFCLK_0n		K1		N1						
B2	VREFB2N0	CLK2	DIFFCLK_1p		N2		T2						
B2	VREFB2N0	CLK3	DIFFCLK_1n		N1		T1						
B2	VREFB2N0	IO	DIFFIO_L19p				T3				DQ1L0	DQ3L0	DQ1L18
B2	VREFB2N0	IO	DIFFIO_L19n				T4				DQ1L1	DQ3L1	DQ1L19
B2	VREFB2N0	IO					U4				DQ1L2	DQ3L2	DQ1L20
B2	VREFB2N0	IO	DIFFIO_L20p		M2		T6	DQ1L2	DQ1L2	DQ1L3	DQ3L3	DQ1L21	DQ1L22
B2	VREFB2N0	IO	DIFFIO_L20n		M1		T5	DQ1L3	DQ1L3	DQ1L4	DQ3L4	DQ1L22	DQ1L23
B2	VREFB2N0	IO	DIFFIO_L21p		M4		U1	DQ1L4	DQ1L4	DQ1L5	DQ3L5	DQ1L23	
B2	VREFB2N0	IO	DIFFIO_L21n		M3		V1	DQ1L5	DQ1L5				
B2	VREFB2N0	IO	DIFFIO_L22p		P2		V4	DQ1L6	DQ1L6	DQ1L6	DQ3L6	DQ1L24	
B2	VREFB2N0	IO	DIFFIO_L22n		P1		W3	DQ1L7	DQ1L7	DQ1L7	DQ3L7	DQ1L25	
B2	VREFB2N0	IO					W1				DQ1L8	DQ3L8	DQ1L26
B2	VREFB2N0	IO	VREFB2N0		P3		U5						
B2	VREFB2N0	IO	DIFFIO_L23p		T2		Y2	DM1L/BWS#1L	DM1L0/BWS#1L0	DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2	
B2	VREFB2N0	IO	DIFFIO_L23n		R1		Y1	DQ1L8	DQ1L8				
B2	VREFB2N0	IO	DIFFIO_L24p		T1		U3						
B2	VREFB2N0	IO	DIFFIO_L24n		U1		U2	DQ3L0	DQ1L9				
B2	VREFB2N0	IO	DIFFIO_L25p				AA2						
B2	VREFB2N0	IO	DIFFIO_L25n				AA1						
B2	VREFB2N1	IO	DIFFIO_L26p		R3		W5	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	
B2	VREFB2N1	IO	DIFFIO_L26n		R2		W4	DQ3L1	DQ1L10				
B2	VREFB2N1	IO	DIFFIO_L27p		V2		AB1	DQ3L2	DQ1L11	DQ3L0	DQ3L9	DQ1L27	
B2	VREFB2N1	IO	DIFFIO_L27n		V1		AC1	DQ3L3	DQ1L12	DQ3L1	DQ3L10	DQ1L28	
B2	VREFB2N1	IO	DIFFIO_L28p		Y1		Y3	DQ3L4	DQ1L13				
B2	VREFB2N1	IO	DIFFIO_L28n		AA1		W2	DQ3L5	DQ1L14				
B2	VREFB2N1	IO	DIFFIO_L29p				AB3						
B2	VREFB2N1	IO	DIFFIO_L29n				AB2			DQ3L2	DQ3L11	DQ1L29	
B2	VREFB2N1	IO	DIFFIO_L30p				AD2			DQ3L3	DQ3L12	DQ1L30	
B2	VREFB2N1	IO	DIFFIO_L30n				AD1			DQ3L4	DQ3L13	DQ1L31	
B2	VREFB2N1	IO	DIFFIO_L31p		Y2	B2_B3	AB4	DQ3L6	DQ1L15				
B2	VREFB2N1	IO	DIFFIO_L31n		AA2	B2_B3	AC4	DM3L/BWS#3L	DM1L1/BWS#1L1				



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B2	VREFB2N1	IO	DIFFIO_L32p				AE2				DQ3L5	DQ3L14	DQ1L32
B2	VREFB2N1	IO	DIFFIO_L32n				AE1				DQ3L6	DQ3L15	DQ1L33
B2	VREFB2N1	IO					AF1	B2_B3					
B2	VREFB2N1	IO	VREFB2N1		U3		V5						
B2	VREFB2N2	IO	DIFFIO_L33p		V4	B2_B3	W7		DQ3L7	DQ1L16	DQ3L7	DQ3L16	DQ1L34
B2	VREFB2N2	IO	DIFFIO_L33n		W4	B2_B3	V6		DQ3L8	DQ1L17	DQ3L8	DQ3L17	DQ1L35
B2	VREFB2N2	IO	RUP1		W2		W6						
B2	VREFB2N2	IO	RDN1		W1		Y6						
B2	VREFB2N2	IO	DIFFIO_L34p				AD4	B2_B3					
B2	VREFB2N2	IO	DIFFIO_L34n				AE3	B2_B3					
B2	VREFB2N2	IO					AD3						
B2	VREFB2N2	IO	VREFB2N2		U2		AB5						
B2	VREFB2N2	IO	DIFFIO_L35p		U4		AA4		DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1
B2	VREFB2N2	IO	DIFFIO_L35n		V3		AA3						
B2	VREFB2N2	IO	DIFFIO_L36p				AA6						
B2	VREFB2N2	IO	DIFFIO_L36n				AA5				DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3
B2	VREFB2N2	IO					AE4	B2_B3					
B2	VREFB2N2	IO					AB6	B2_B3					
B3	VREFB3N2	IO	DIFFIO_B1p				AA8						
B3	VREFB3N2	IO	DIFFIO_B1n		AA3		AA9						
B3	VREFB3N2	IO	DIFFIO_B2p				AC6	B2_B3					
B3	VREFB3N2	IO	DIFFIO_B2n				AD6				DM1B		
B3	VREFB3N2	IO	DIFFIO_B3p		W5		AE5		DQ3B8	DQ3B17			
B3	VREFB3N2	IO	DIFFIO_B3n		Y5		AF5		DQ3B7	DQ3B16	DQ1B7		
B3	VREFB3N2	IO			Y4		AE6		DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2
B3	VREFB3N2	IO	PLL1_CLKOUTp		AB3		AF4						
B3	VREFB3N2	IO	PLL1_CLKOUTn		AB4		AG4						
B3	VREFB3N2	IO	DIFFIO_B4p				AD7				DQ1B6		
B3	VREFB3N2	IO	DIFFIO_B4n				AE7				DQ1B5		
B3	VREFB3N2	IO			AB2	B2_B3	AF6				DQ1B4		
B3	VREFB3N2	IO	VREFB3N2		Y7		AF8						
B3	VREFB3N2	IO	DIFFIO_B5p		AA5		AG2		DQ3B6	DQ3B15	DQ1B3		
B3	VREFB3N2	IO	DIFFIO_B5n		AB5		AH2		DM3B/BWS#3B	DM3B1/BWS#3B1	DQ1B2		
B3	VREFB3N2	IO	DIFFIO_B6p		AA6		AB9		DQ3B5	DQ3B14			
B3	VREFB3N2	IO	DIFFIO_B6n		AB6		AC9		DQ3B4	DQ3B13			
B3	VREFB3N2	IO	DIFFIO_B7p				AH3				DQ1B1		
B3	VREFB3N2	IO	DIFFIO_B7n				AH4				DQ1B0		
B3	VREFB3N2	IO	DIFFIO_B8p		V7		AD9						
B3	VREFB3N2	IO	DIFFIO_B8n		W7		AE8						
B3	VREFB3N2	IO					AG8						
B3	VREFB3N1	IO	DIFFIO_B9p				AG5				DQ3B8	DQ3B17	DQ5B35
B3	VREFB3N1	IO	DIFFIO_B9n				AH5				DQ3B7	DQ3B16	DQ5B34



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B3	VREFB3N1	IO	DIFFIO_B10p		AA7		AB10		DQ3B3	DQ3B12	DQ3B6	DQ3B15	DQ5B33
B3	VREFB3N1	IO	DIFFIO_B10n		AB7		AC10		DQ3B2	DQ3B11	DM3B/BWS#3B	DM3B1/BWS#3B1	DM5B3/BWS#5B3
B3	VREFB3N1	IO	DIFFIO_B11p		AA8		AD10						
B3	VREFB3N1	IO	DIFFIO_B11n				AE10						
B3	VREFB3N1	IO	DIFFIO_B12p				AG6				DQ3B5	DQ3B14	DQ5B32
B3	VREFB3N1	IO	DIFFIO_B12n				AH6				DQ3B4	DQ3B13	DQ5B31
B3	VREFB3N1	IO	DIFFIO_B13p				AB11						
B3	VREFB3N1	IO	DIFFIO_B13n				AB12						
B3	VREFB3N1	IO					AF11						
B3	VREFB3N1	IO	DIFFIO_B14p				AE9				DQ3B3	DQ3B12	DQ5B30
B3	VREFB3N1	IO	DIFFIO_B14n				AF9				DQ3B2	DQ3B11	DQ5B29
B3	VREFB3N1	IO					AG11						
B3	VREFB3N1	IO	VREFB3N1		W9		AE11						
B3	VREFB3N1	IO	DIFFIO_B15p		AB8		AH7		DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2
B3	VREFB3N1	IO	DIFFIO_B15n				AH8				DQ3B1	DQ3B10	DQ5B28
B3	VREFB3N1	IO	DIFFIO_B16p				AG9				DQ3B0	DQ3B9	DQ5B27
B3	VREFB3N0	IO	DIFFIO_B16n				AH9						
B3	VREFB3N0	IO	DIFFIO_B17p		AA9		AB13		DQ3B1	DQ3B10	DM5B/BWS#5B	DM3B0/BWS#3B0	DM5B2/BWS#5B2
B3	VREFB3N0	IO	DIFFIO_B17n		AB9		AC12		DQ3B0	DQ3B9	DQ5B8	DQ3B8	DQ5B26
B3	VREFB3N0	IO	DIFFIO_B18p		W11	B3_B4	AH10		DQ5B8	DQ3B8	DQ5B7	DQ3B7	DQ5B25
B3	VREFB3N0	IO	DIFFIO_B18n		Y11	B3_B4	AH11		DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3
B3	VREFB3N0	IO	DIFFIO_B19p		W6		AB14				DQ5B6	DQ3B6	DQ5B24
B3	VREFB3N0	IO	DIFFIO_B19n		Y6		AC14						
B3	VREFB3N0	IO	DIFFIO_B20p				AG12				DQ5B5	DQ3B5	DQ5B23
B3	VREFB3N0	IO	DIFFIO_B20n				AH12				DQ5B4	DQ3B4	DQ5B22
B3	VREFB3N0	IO	DIFFIO_B21p				AE12						
B3	VREFB3N0	IO	DIFFIO_B21n				AD12				DQ5B3	DQ3B3	DQ5B21
B3	VREFB3N0	IO	VREFB3N0		Y9		AF12						
B3	VREFB3N0	IO					AH14						
B3	VREFB3N0	IO	DIFFIO_B22p				AD14				DQ5B2	DQ3B2	DQ5B20
B3	VREFB3N0	IO	DIFFIO_B22n				AE14				DQ5B1	DQ3B1	DQ5B19
B3	VREFB3N0	IO	DIFFIO_B23p		AA11	B3_B4	AF13		DM5B/BWS#5B	DM3B0/BWS#3B0	DQ5B0	DQ3B0	DQ5B18
B3	VREFB3N0	IO	DIFFIO_B23n		AB11	B3_B4	AE13		DQ5B7	DQ3B7			
B3	VREFB3N0	CLK15	DIFFCLK_6p		AA10		AG13						
B3	VREFB3N0	CLK14	DIFFCLK_6n		AB10		AH13						
B4	VREFB4N2	CLK13	DIFFCLK_7p		AA13		AG16						
B4	VREFB4N2	CLK12	DIFFCLK_7n		AB13		AH16						
B4	VREFB4N2	IO	DIFFIO_B24p				AF16				DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1
B4	VREFB4N2	IO	DIFFIO_B24n				AE16					DQ5B17	DQ5B17
B4	VREFB4N2	IO	DIFFIO_B25p				AG15	B3_B4			DQ4B7	DQ5B16	DQ5B16
B4	VREFB4N2	IO	DIFFIO_B25n				AH15	B3_B4			DQ4B6	DQ5B15	DQ5B15
B4	VREFB4N2	IO	DIFFIO_B26p				AH17				DQ4B5	DQ5B14	DQ5B14



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B4	VREFB4N2	IO	DIFFIO_B26n				AH18				DQ4B4	DQ5B13	DQ5B13
B4	VREFB4N2	IO					AC16				DQ4B3	DQ5B12	DQ5B12
B4	VREFB4N2	IO	DIFFIO_B27p		AA12		AC15	B3_B4	DQ5B6	DQ3B6			
B4	VREFB4N2	IO	DIFFIO_B27n		AB12		AB16		DQ5B5	DQ3B5	DQ4B2	DQ5B11	DQ5B11
B4	VREFB4N2	IO	VREFB4N2		AA14		AD16						
B4	VREFB4N2	IO					AF15	B3_B4					
B4	VREFB4N2	IO	DIFFIO_B28p		W12		AG18		DQ5B4	DQ3B4	DQ4B1	DQ5B10	DQ5B10
B4	VREFB4N2	IO	DIFFIO_B28n		Y12		AH19		DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4
B4	VREFB4N2	IO	DIFFIO_B29p		AB14		AG20		DQ5B3	DQ3B3	DQ4B0	DQ5B9	DQ5B9
B4	VREFB4N2	IO	DIFFIO_B29n		AB15		AH20		DQ5B2	DQ3B2			
B4	VREFB4N2	IO	DIFFIO_B30p				AG21				DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0
B4	VREFB4N2	IO	DIFFIO_B30n				AH21				DQ2B7	DQ5B8	DQ5B8
B4	VREFB4N2	IO	DIFFIO_B31p		W14		AA17		DQ5B1	DQ3B1			
B4	VREFB4N2	IO	DIFFIO_B31n		Y14		AB17		DQ5B0	DQ3B0			
B4	VREFB4N1	IO	DIFFIO_B32p		AA15		AG22				DQ2B6	DQ5B7	DQ5B7
B4	VREFB4N1	IO	DIFFIO_B32n		AA16		AH22				DQ2B5	DQ5B6	DQ5B6
B4	VREFB4N1	IO	DIFFIO_B33p		AB16		AC17		DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5
B4	VREFB4N1	IO	DIFFIO_B33n		AB17		AD17						
B4	VREFB4N1	IO	DIFFIO_B34p		W17		AH23						
B4	VREFB4N1	IO	DIFFIO_B34n		Y17		AH24				DQ2B4	DQ5B5	DQ5B5
B4	VREFB4N1	IO	DIFFIO_B35p				AE17						
B4	VREFB4N1	IO	DIFFIO_B35n				AE18						
B4	VREFB4N1	IO	DIFFIO_B36p				AE19				DQ2B3	DQ5B4	DQ5B4
B4	VREFB4N1	IO	DIFFIO_B36n				AF18				DQ2B2	DQ5B3	DQ5B3
B4	VREFB4N1	IO	DIFFIO_B37p		AA18		AE21						
B4	VREFB4N1	IO	DIFFIO_B37n				AE22						
B4	VREFB4N1	IO	DIFFIO_B38p				AF20				DQ2B1	DQ5B2	DQ5B2
B4	VREFB4N1	IO	DIFFIO_B38n				AF21				DQ2B0	DQ5B1	DQ5B1
B4	VREFB4N1	IO			V17		AE20						
B4	VREFB4N1	IO	DIFFIO_B39p		AB20	B4_B5	AB18				DM0B	DQ5B0	DQ5B0
B4	VREFB4N1	IO	DIFFIO_B39n		AB21	B4_B5	AB19						
B4	VREFB4N1	IO	VREFB4N1		AA17		AD19						
B4	VREFB4N0	IO	RUP2		W16		AE23						
B4	VREFB4N0	IO	RDN2		Y16		AF22						
B4	VREFB4N0	IO	DIFFIO_B40p		W18		AF24				DQ0B7		
B4	VREFB4N0	IO	DIFFIO_B40n		Y19		AG24		DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3
B4	VREFB4N0	IO	DIFFIO_B41p				AG25				DQ0B6		
B4	VREFB4N0	IO	DIFFIO_B41n				AH25				DQ0B5		
B4	VREFB4N0	IO	DIFFIO_B42p				AB20				DQ0B4		
B4	VREFB4N0	IO	DIFFIO_B42n				AC19				DQ0B2		
B4	VREFB4N0	IO	DIFFIO_B43p				AE25	B4_B5					



Pin Information for the CycloneIII LS EP3CLS200 Device

Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
B4	VREFB4N0	IO	DIFFIO_B43n				AF25	B4_B5					
B4	VREFB4N0	IO	VREFB4N0		Y18		AE24						
B4	VREFB4N0	IO	DIFFIO_B44p				AH26				DQ0B3		
B4	VREFB4N0	IO	DIFFIO_B44n				AH27				DQ0B1		
B4	VREFB4N0	IO					AD25	B4_B5					
B4	VREFB4N0	IO	PLL4_CLKOUTp		AB18		AD22						
B4	VREFB4N0	IO	PLL4_CLKOUTn		AB19		AD21						
B4	VREFB4N0	IO					AD24	B4_B5					
B4	VREFB4N0	IO	DIFFIO_B45p				AC21						
B4	VREFB4N0	IO	DIFFIO_B45n				AC22				DQ0B0		
B5	VREFB5N2	IO	DIFFIO_R41n		V19	B4_B5	AA24				DM3R/BWS#3R	DM3R1/BWS#3R1	DM1R3/BWS#1R3
B5	VREFB5N2	IO	DIFFIO_R41p		W19	B4_B5	AA23				DQ3R8	DQ3R17	DQ1R35
B5	VREFB5N2	IO					AC24				DQ3R7	DQ3R16	DQ1R34
B5	VREFB5N2	IO	RUP3		W22		AB24						
B5	VREFB5N2	IO	RDN3		V22		AB25						
B5	VREFB5N2	IO			V20		AE27		DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4
B5	VREFB5N2	IO	VREFB5N2		V21		AC25						
B5	VREFB5N2	IO	DIFFIO_R40n		AA21		AE26		DM3R/BWS#3R	DM3R1/BWS#3R1	DQ3R6	DQ3R15	DQ1R33
B5	VREFB5N2	IO	DIFFIO_R40p		AA20	B4_B5	AF27				DQ3R5	DQ3R14	DQ1R32
B5	VREFB5N2	IO	DIFFIO_R39n				W23						
B5	VREFB5N2	IO	DIFFIO_R39p		T18		Y23						
B5	VREFB5N2	IO	DIFFIO_R38n				AE28				DQ3R4	DQ3R13	DQ1R31
B5	VREFB5N2	IO	DIFFIO_R38p				AF28				DQ3R3	DQ3R12	DQ1R30
B5	VREFB5N2	IO	DIFFIO_R37n		T21		W25		DQ3R8	DQ3R17	DQ3R2	DQ3R11	DQ1R29
B5	VREFB5N2	IO	DIFFIO_R37p		U20		W24		DQ3R7	DQ3R16			
B5	VREFB5N1	IO	DIFFIO_R36n				AD27				DQ3R1	DQ3R10	DQ1R28
B5	VREFB5N1	IO	DIFFIO_R36p				AD26				DQ3R0	DQ3R9	DQ1R27
B5	VREFB5N1	IO	DIFFIO_R35n				U24						
B5	VREFB5N1	IO	DIFFIO_R35p				U23						
B5	VREFB5N1	IO	DIFFIO_R34n		W21		AB26		DQ3R6	DQ3R15			
B5	VREFB5N1	IO	DIFFIO_R34p		Y21		AA25		DQ3R5	DQ3R14			
B5	VREFB5N1	IO	DIFFIO_R33n				AC28				DM1R/BWS#1R	DM3R0/BWS#3R0	DM1R2/BWS#1R2
B5	VREFB5N1	IO	DIFFIO_R33p				AD28				DQ1R8	DQ3R8	DQ1R26
B5	VREFB5N1	IO	DIFFIO_R32n		Y22		Y26		DQ3R4	DQ3R13	DQ1R7	DQ3R7	DQ1R25
B5	VREFB5N1	IO	DIFFIO_R32p		AA22		AA26		DQ3R3	DQ3R12			
B5	VREFB5N1	IO	DIFFIO_R31n				W26				DQ1R6	DQ3R6	DQ1R24
B5	VREFB5N1	IO	DIFFIO_R31p				V25						
B5	VREFB5N1	IO	DIFFIO_R30n				AB28				DQ1R5	DQ3R5	DQ1R23
B5	VREFB5N1	IO	DIFFIO_R30p				AB27				DQ1R4	DQ3R4	DQ1R22
B5	VREFB5N1	IO	DIFFIO_R29n		U22		V24		DQ3R2	DQ3R11	DQ1R3	DQ3R3	DQ1R21
B5	VREFB5N1	IO	DIFFIO_R29p		U21		V23				DQ1R2	DQ3R2	DQ1R20
B5	VREFB5N1	IO	VREFB5N1		R20		U27						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
B5	VREFB5N1	IO	DIFFIO_R28n				R24	B5_B6					
B5	VREFB5N1	IO	DIFFIO_R28p				R23	B5_B6					
B5	VREFB5N0	IO	DIFFIO_R27n		R22		AA28		DQ3R1	DQ3R10			
B5	VREFB5N0	IO	DIFFIO_R27p		T22		AA27		DQ3R0	DQ3R9			
B5	VREFB5N0	IO	DIFFIO_R26n				R28	B5_B6					
B5	VREFB5N0	IO	DIFFIO_R26p				R27	B5_B6					
B5	VREFB5N0	IO	DIFFIO_R25n				U26				DQ1R1	DQ3R1	DQ1R19
B5	VREFB5N0	IO	DIFFIO_R25p				U25						
B5	VREFB5N0	IO	VREFB5N0		P21		T23						
B5	VREFB5N0	IO	DIFFIO_R24n				Y28				DQ1R0	DQ3R0	DQ1R18
B5	VREFB5N0	IO	DIFFIO_R24p		P20		Y27		DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6
B5	VREFB5N0	IO	DIFFIO_R23n	DEV_OE	P22		W28						
B5	VREFB5N0	IO	DIFFIO_R23p	DEV_CLRn	R21		W27						
B5	VREFB5N0	IO	DIFFIO_R22n		M20		T26		DM1R/BWS#1R	DM3R0/BWS#3R0			
B5	VREFB5N0	IO	DIFFIO_R22p		M19		R25	B5_B6					
B5	VREFB5N0	IO	DIFFIO_R21n		M22		U28		DQ1R8	DQ3R8			
B5	VREFB5N0	IO	DIFFIO_R21p		M21		V28		DQ1R7	DQ3R7			
B5	VREFB5N0	IO					R26	B5_B6					
B5	VREFB5N0	CLK7	DIFFCLK_3n		N22		T28						
B5	VREFB5N0	CLK6	DIFFCLK_3p		N21		T27						
B6	VREFB6N2	CLK5	DIFFCLK_2n		K22		N28						
B6	VREFB6N2	CLK4	DIFFCLK_2p		K21		N27						
B6	VREFB6N2	CONF_DONE		CONF_DONE	J21		P22						
B6	VREFB6N2	MSEL0		MSEL0	J20		P25						
B6	VREFB6N2	MSEL1		MSEL1	J19		P23						
B6	VREFB6N2	MSEL2		MSEL2	J22		P24						
B6	VREFB6N2	MSEL3		MSEL3	K19		N22						
B6	VREFB6N2	IO	DIFFIO_R20n	INIT_DONE	H22		P27						
B6	VREFB6N2	IO	DIFFIO_R20p	CRC_ERROR	H21		P26						
B6	VREFB6N2	IO					P28						
B6	VREFB6N2	IO	VREFB6N2		K18		N23						
B6	VREFB6N2	IO	DIFFIO_R19n	nCEO	G22		L28						
B6	VREFB6N2	IO	DIFFIO_R19p	CLKUSR	G21		M28						
B6	VREFB6N2	IO	DIFFIO_R18n		L22	B5_B6	N26		DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7
B6	VREFB6N2	IO	DIFFIO_R18p		L21	B5_B6	M25			DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R1	DM1R1/BWS#1R1
B6	VREFB6N2	IO	DIFFIO_R17n				M27					DQ1R17	DQ1R17
B6	VREFB6N2	IO	DIFFIO_R17p				M26				DQ0R7	DQ1R16	DQ1R16
B6	VREFB6N2	IO	DIFFIO_R16n				L25				DQ0R6	DQ1R15	DQ1R15
B6	VREFB6N2	IO	DIFFIO_R16p				L24				DQ0R5	DQ1R14	DQ1R14
B6	VREFB6N2	IO	DIFFIO_R15n				K28				DQ0R4	DQ1R13	DQ1R13
B6	VREFB6N1	IO	DIFFIO_R15p				K27				DQ0R3	DQ1R12	DQ1R12



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
B6	VREFB6N1	IO	DIFFIO_R14n		F22		K26		DQ1R6	DQ3R6	DQ0R2	DQ1R11	DQ1R11
B6	VREFB6N1	IO	DIFFIO_R14p		F21		K25		DQ1R5	DQ3R5	DQ0R1	DQ1R10	DQ1R10
B6	VREFB6N1	IO	DIFFIO_R13n				J28				DQ0R0	DQ1R9	DQ1R9
B6	VREFB6N1	IO	DIFFIO_R13p				J27					DQ1R8	DQ1R8
B6	VREFB6N1	IO					H28				DM2R	DM1R0/BWS#1R0	DM1R0/BWS#1R0
B6	VREFB6N1	IO	DIFFIO_R12n				J26				DQ2R7	DQ1R7	DQ1R7
B6	VREFB6N1	IO	DIFFIO_R12p				J25				DQ2R6	DQ1R6	DQ1R6
B6	VREFB6N1	IO	DIFFIO_R11n		E22		G28		DQ1R4	DQ3R4	DQ2R5	DQ1R5	DQ1R5
B6	VREFB6N1	IO	DIFFIO_R11p		E21		G27		DQ1R3	DQ3R3	DQ2R4	DQ1R4	DQ1R4
B6	VREFB6N1	IO	VREFB6N1		F20		M24						
B6	VREFB6N1	IO					H27						
B6	VREFB6N1	IO	DIFFIO_R10n		C22		E28		DQ1R2	DQ3R2			
B6	VREFB6N1	IO	DIFFIO_R10p		D22		F28		DQ1R1	DQ3R1			
B6	VREFB6N1	IO	DIFFIO_R9n		H20		L23		DQ1R0	DQ3R0	DQ2R3	DQ1R3	DQ1R3
B6	VREFB6N1	IO	DIFFIO_R9p		H19		M23				DQ2R2	DQ1R2	DQ1R2
B6	VREFB6N1	IO	DIFFIO_R8n		B22		J24						
B6	VREFB6N1	IO	DIFFIO_R8p		B21	B6_B7	K24						
B6	VREFB6N0	IO	DIFFIO_R7n				C28	B6_B7					
B6	VREFB6N0	IO	DIFFIO_R7p				D28						
B6	VREFB6N0	IO	DIFFIO_R6n		C21	B6_B7	K23				DQ2R1	DQ1R1	DQ1R1
B6	VREFB6N0	IO	DIFFIO_R6p		D21		K22						
B6	VREFB6N0	IO	DIFFIO_R5n		D19	B6_B7	E26	B6_B7					
B6	VREFB6N0	IO	DIFFIO_R5p		E19		E27						
B6	VREFB6N0	IO	DIFFIO_R4n		F19		G26		DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5
B6	VREFB6N0	IO	DIFFIO_R4p				H26				DQ2R0	DQ1R0	DQ1R0
B6	VREFB6N0	IO	DIFFIO_R3n				F25	B6_B7					
B6	VREFB6N0	IO	DIFFIO_R3p				G25						
B6	VREFB6N0	IO	DIFFIO_R2n				D27						
B6	VREFB6N0	IO	DIFFIO_R2p				D26	B6_B7					
B6	VREFB6N0	IO	VREFB6N0		E20		J23						
B6	VREFB6N0	IO	DIFFIO_R1n				G24						
B6	VREFB6N0	IO	DIFFIO_R1p				G23	B6_B7					
B7	VREFB7N0	IO	DIFFIO_T47n				F22						
B7	VREFB7N0	IO	DIFFIO_T47p				F21				DQ0T0		
B7	VREFB7N0	IO	DIFFIO_T46n		A20		E24						
B7	VREFB7N0	IO	DIFFIO_T46p		A21	B6_B7	F24	B6_B7					
B7	VREFB7N0	IO	DIFFIO_T45n				E21				DQ0T1		
B7	VREFB7N0	IO	DIFFIO_T45p		C19		E22		DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6
B7	VREFB7N0	IO					E25						
B7	VREFB7N0	IO	DIFFIO_T44n				C25						
B7	VREFB7N0	IO	DIFFIO_T44p				D25						
B7	VREFB7N0	IO	VREFB7N0		B20		D24						



Pin Information for the CycloneIII LS EP3CLS200 Device

Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
B7	VREFB7N0	IO	DIFFIO_T43n				D22				DQ0T2		
B7	VREFB7N0	IO	DIFFIO_T43p				D23				DQ0T3		
B7	VREFB7N0	IO	DIFFIO_T42n				A27				DQ0T4		
B7	VREFB7N0	IO	DIFFIO_T42p				B27				DQ0T5		
B7	VREFB7N0	IO	PLL2_CLKOUTn		A18		C21						
B7	VREFB7N0	IO	PLL2_CLKOUTp		A19		D21						
B7	VREFB7N0	IO	DIFFIO_T41n				A25				DQ0T6		
B7	VREFB7N0	IO	DIFFIO_T41p				A26				DQ0T7		
B7	VREFB7N0	IO	DIFFIO_T40n				B25				DM0T		
B7	VREFB7N0	IO	DIFFIO_T40p				C24						
B7	VREFB7N1	IO	RUP4		C18		D20						
B7	VREFB7N1	IO	RDN4		B18		D19						
B7	VREFB7N1	IO					B24						
B7	VREFB7N1	IO	DIFFIO_T39n		A17		G19		DQ5T0	DQ5T0	DQ2T0	DQ5T0	DQ5T0
B7	VREFB7N1	IO	DIFFIO_T39p		B17		G20		DQ5T1	DQ5T1	DQ2T1	DQ5T1	DQ5T1
B7	VREFB7N1	IO	DIFFIO_T38n				B19				DQ2T2	DQ5T2	DQ5T2
B7	VREFB7N1	IO	DIFFIO_T38p				C19				DQ2T3	DQ5T3	DQ5T3
B7	VREFB7N1	IO	DIFFIO_T37n				D17						
B7	VREFB7N1	IO	DIFFIO_T37p				D18						
B7	VREFB7N1	IO	DIFFIO_T36n		A16		E19		DQ5T2	DQ5T2			
B7	VREFB7N1	IO	DIFFIO_T36p		B16		F19		DQ5T3	DQ5T3			
B7	VREFB7N1	IO	DIFFIO_T35n				B22				DQ2T4	DQ5T4	DQ5T4
B7	VREFB7N1	IO	DIFFIO_T35p				C22				DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5T0
B7	VREFB7N1	IO	DIFFIO_T34n				F17						
B7	VREFB7N1	IO	DIFFIO_T34p				E17						
B7	VREFB7N1	IO	VREFB7N1		C16		A24						
B7	VREFB7N1	IO	DIFFIO_T33n				B18				DQ2T5	DQ5T5	DQ5T5
B7	VREFB7N1	IO	DIFFIO_T33p		D14		C18		DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8
B7	VREFB7N1	IO	DIFFIO_T32n		A15		B21		DQ5T4	DQ5T4	DQ2T6	DQ5T6	DQ5T6
B7	VREFB7N1	IO	DIFFIO_T32p		B15		A21		DM5T/BWS#5T	DM5T0/BWS#5T0	DQ2T7	DQ5T7	DQ5T7
B7	VREFB7N2	IO	DIFFIO_T31n		A14		G17					DQ5T8	DQ5T8
B7	VREFB7N2	IO	DIFFIO_T31p		B14		G18		DQ5T5	DQ5T5			
B7	VREFB7N2	IO	DIFFIO_T30n				A22						
B7	VREFB7N2	IO	DIFFIO_T30p				A23						
B7	VREFB7N2	IO	DIFFIO_T29n				D16				DQ4T0	DQ5T9	DQ5T9
B7	VREFB7N2	IO	DIFFIO_T29p				E16				DQ4T1	DQ5T10	DQ5T10
B7	VREFB7N2	IO	DIFFIO_T28n		C17		A15	B7_B8					
B7	VREFB7N2	IO	DIFFIO_T28p		D17		B15	B7_B8			DQ4T2	DQ5T11	DQ5T11
B7	VREFB7N2	IO					C15	B7_B8			DQ4T3	DQ5T12	DQ5T12
B7	VREFB7N2	IO	VREFB7N2		C14		C16						
B7	VREFB7N2	IO	DIFFIO_T27n		C12		F16		DQ5T6	DQ5T6	DQ4T4	DQ5T13	DQ5T13
B7	VREFB7N2	IO	DIFFIO_T27p		D12		G16		DQ5T7	DQ5T7	DQ4T5	DQ5T14	DQ5T14
B7	VREFB7N2	IO	DIFFIO_T26n		A12		A19		DQ5T8	DQ5T8	DQ4T6	DQ5T15	DQ5T15



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
B7	VREFB7N2	IO	DIFFIO_T26p		B12		A20		DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9
B7	VREFB7N2	IO					D15	B7_B8			DQ4T7	DQ5T16	DQ5T16
B7	VREFB7N2	IO	DIFFIO_T25n				A17					DQ5T17	DQ5T17
B7	VREFB7N2	IO	DIFFIO_T25p				A18				DM4T	DM5T1/BWS#5T1	DM5T1/BWS#5T1
B7	VREFB7N2	CLK8	DIFFCLK_5n		A13		A16						
B7	VREFB7N2	CLK9	DIFFCLK_5p		B13		B16						
B8	VREFB8N0	CLK10	DIFFCLK_4n		A10		A13						
B8	VREFB8N0	CLK11	DIFFCLK_4p		B10		B13						
B8	VREFB8N0	IO	DIFFIO_T24n		E11	B7_B8	A12		DQ3T0	DQ5T9	DQ5T0	DQ3T0	DQ5T18
B8	VREFB8N0	IO	DIFFIO_T24p				B12				DQ5T1	DQ3T1	DQ5T19
B8	VREFB8N0	IO	DIFFIO_T23n		A11	B7_B8	D13		DQ3T1	DQ5T10	DQ5T2	DQ3T2	DQ5T20
B8	VREFB8N0	IO	DIFFIO_T23p		B11	B7_B8	E14		DQ3T2	DQ5T11	DQ5T3	DQ3T3	DQ5T21
B8	VREFB8N0	IO	DIFFIO_T22n		C11	B7_B8	A10				DQ5T4	DQ3T4	DQ5T22
B8	VREFB8N0	IO	DIFFIO_T22p		D11	B7_B8	A11		DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10
B8	VREFB8N0	IO	DIFFIO_T21n				F14				DQ5T5	DQ3T5	DQ5T23
B8	VREFB8N0	IO	DIFFIO_T21p				G14				DQ5T6	DQ3T6	DQ5T24
B8	VREFB8N0	IO	VREFB8N0		D9		A14						
B8	VREFB8N0	IO	DIFFIO_T20n				D14				DQ5T7	DQ3T7	DQ5T25
B8	VREFB8N0	IO	DIFFIO_T20p				C13				DQ5T8	DQ3T8	DQ5T26
B8	VREFB8N0	IO	DIFFIO_T19n	DATA2	A9		A9		DQ3T3	DQ5T12	DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2
B8	VREFB8N0	IO	DIFFIO_T19p	DATA3	B9		B9		DQ3T4	DQ5T13			
B8	VREFB8N0	IO	DIFFIO_T18n		A8		A8		DQ3T5	DQ5T14			
B8	VREFB8N0	IO	DIFFIO_T18p	DATA4	B8		B8		DQ3T6	DQ5T15			
B8	VREFB8N0	IO	DIFFIO_T17n		A7		F12		DQ3T7	DQ5T16			
B8	VREFB8N0	IO	DIFFIO_T17p		B7		E12		DQ3T8	DQ5T17			
B8	VREFB8N1	IO	DIFFIO_T16n				B11				DQ3T0	DQ3T9	DQ5T27
B8	VREFB8N1	IO	DIFFIO_T16p				C11				DQ3T1	DQ3T10	DQ5T28
B8	VREFB8N1	IO	DIFFIO_T15n		A6		G13		DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11
B8	VREFB8N1	IO	DIFFIO_T15p		B6		G12		DM3T/BWS#3T	DM5T1/BWS#5T1			
B8	VREFB8N1	IO	DIFFIO_T14n				C12				DQ3T2	DQ3T11	DQ5T29
B8	VREFB8N1	IO	DIFFIO_T14p				D12				DQ3T3	DQ3T12	DQ5T30
B8	VREFB8N1	IO	DIFFIO_T13n				A6				DQ3T4	DQ3T13	DQ5T31
B8	VREFB8N1	IO	DIFFIO_T13p	DATA5	C9		A7				DQ3T5	DQ3T14	DQ5T32
B8	VREFB8N1	IO	VREFB8N1		D7		G11						
B8	VREFB8N1	IO	DIFFIO_T12n				C9						
B8	VREFB8N1	IO	DIFFIO_T12p				D9						
B8	VREFB8N1	IO	DIFFIO_T11n				D10						
B8	VREFB8N1	IO	DIFFIO_T11p				D11						
B8	VREFB8N1	IO	DIFFIO_T10n	DATA6	A4		A3						
B8	VREFB8N1	IO	DIFFIO_T10p	DATA7	A5		A4						
B8	VREFB8N1	IO	DIFFIO_T9n		C6		F10				DQ3T6	DQ3T15	DQ5T33



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
B8	VREFB8N1	IO	DIFFIO_T9p		D6		G10				DQ3T7	DQ3T16	DQ5T34
B8	VREFB8N1	IO	DIFFIO_T8n		C7		C8				DQ3T8	DQ3T17	DQ5T35
B8	VREFB8N1	IO	DIFFIO_T8p				D8				DM3T/BWS#3T	DM3T1/BWS#3T1	DM5T3/BWS#5T3
B8	VREFB8N1	IO	DIFFIO_T7n		A2	B8_B1	F8				DQ1T0		
B8	VREFB8N2	IO	DIFFIO_T7p		A3	B8_B1	G9				DQ1T1		
B8	VREFB8N2	IO					A5						
B8	VREFB8N2	IO	VREFB8N2		E6		E10						
B8	VREFB8N2	IO	DIFFIO_T6n				C4						
B8	VREFB8N2	IO	DIFFIO_T6p				D4	B8_B1					
B8	VREFB8N2	IO	DIFFIO_T5n				E7				DQ1T2		
B8	VREFB8N2	IO	DIFFIO_T5p				F7						
B8	VREFB8N2	IO	DIFFIO_T4n				B7				DQ1T3		
B8	VREFB8N2	IO	DIFFIO_T4p				C7				DQ1T4		
B8	VREFB8N2	IO	DIFFIO_T3n		B3	B8_B1	D7				DQ1T5		
B8	VREFB8N2	IO	DIFFIO_T3p		C4		E8		DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7
B8	VREFB8N2	IO	DIFFIO_T2n		D4	B8_B1	B5				DQ1T6		
B8	VREFB8N2	IO	DIFFIO_T2p		D5	B8_B1	C5				DQ1T7		
B8	VREFB8N2	IO					B4				DM1T		
B8	VREFB8N2	IO	PLL3_CLKOUTn		B5		D6						
B8	VREFB8N2	IO	PLL3_CLKOUTp		C5		D5						
B8	VREFB8N2	IO	DIFFIO_T1n				B2	B8_B1					
B8	VREFB8N2	IO	DIFFIO_T1p				A2						
B8	VREFB8N2	IO					E5	B8_B1					
		GND			F10		AA11						
		GND			F13		AA13						
		GND			G6	B1	AA15						
		GND			G11		AA19						
		GND			G12		AA21						
		GND			G16		AB15	B3_B4					
		GND			G17		AB21	B4_B5					
		GND			H9		G21	B6_B7					
		GND			H10		H10						
		GND			H13		H12						
		GND			H14		H14						
		GND			J8		H16						
		GND			J15		H18						
		GND			K6		H20						
		GND			K8		H8						
		GND			K10		J11						
		GND			K11		J13						
		GND			K12		J15						
		GND			K13		J17						
		GND			K15		J19						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		GND			K17		J21						
		GND			L7		J9						
		GND			L10		K10						
		GND			L11		K12						
		GND			L12		K14						
		GND			L13		K16						
		GND			L16		K18						
		GND			M7		K20						
		GND			M10		K8						
		GND			M11		L11						
		GND			M12		L13						
		GND			M13		L15						
		GND			M16		L17						
		GND			N6		L19						
		GND			N8		L21						
		GND			N10		L7						
		GND			N11		L9						
		GND			N12		M10						
		GND			N13		M12						
		GND			N15		M14						
		GND			N17		M16						
		GND			P8		M18						
		GND			P15		M20						
		GND			R7		M22						
		GND			R9		M8						
		GND			R10		N11						
		GND			R13		N13						
		GND			R14		N15						
		GND			R16		N17						
		GND			T6		N19						
		GND			T11		N21						
		GND			T17		N7						
		GND			U10		N9						
		GND			U13		P10						
		GND			L4	B1_B2	P12						
		GND			L5		P14						
		GND			J6		P16						
		GND			H7		P18						
		GND			G7		P20						
		GND			G5	B1	P8						
		GND			M5		R11						
		GND			R5		R13						
		GND			P4		R15						
		GND			T5		R17						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		GND			U9		R19						
		GND			U8		R21						
		GND			V8		R5	B1_B2					
		GND			V11		R6	B1_B2					
		GND			T12		R7						
		GND			U14		R9						
		GND			U15		T10						
		GND			V15		T12						
		GND			V12		T14						
		GND			T16		T16						
		GND			P17		T18						
		GND			P19		T20						
		GND			R18		T22						
		GND			U19		T8						
		GND			M18	B5_B6	U11						
		GND			L18	B5_B6	U13						
		GND			J17		U15						
		GND			H16		U17						
		GND			H18		U19						
		GND			F14		U21						
		GND			E15		U7						
		GND			D16		U9						
		GND			F15		V10						
		GND			E17		V12						
		GND			E12		V14						
		GND			F9		V16						
		GND			E8		V18						
		GND			F8		V20						
		GND			A1	B8_B1	V22						
		GND			C3	B8_B1	V8						
		GND			G3		W11						
		GND			K3	B1	W13						
		GND			N3		W15						
		GND			T3		W17						
		GND			Y3	B2_B3	W19						
		GND			AB1	B2_B3	W21						
		GND			A22	B6_B7	W9						
		GND			AB22	B4_B5	Y10						
		GND			Y8		Y12						
		GND			Y10		Y14						
		GND			Y13		Y16						
		GND			Y15		Y18						
		GND			Y20	B4_B5	Y20						
		GND			T20		Y22						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		GND			N20		Y8						
		GND			K20		R2	B1_B2					
		GND			G20		B1	B8_B1					
		GND			C20	B6_B7	F2						
		GND			C15		H4						
		GND			C13		L2	B1					
		GND			C10		N4	B1					
		GND			C8		V2						
		GND					Y4						
		GND					AC2						
		GND					AG1	B2_B3					
		GND					AG3						
		GND					AD5	B2_B3					
		GND					AG7						
		GND					AD8						
		GND					AG10						
		GND					AD11						
		GND					AD13						
		GND					AG14						
		GND					AE15	B3_B4					
		GND					AG17						
		GND					AG19						
		GND					AD18						
		GND					AD20						
		GND					AD23	B4_B5					
		GND					AG23						
		GND					AG26	B4_B5					
		GND					AG28	B4_B5					
		GND					AC27						
		GND					Y25						
		GND					V27						
		GND					T25						
		GND					N25						
		GND					L27						
		GND					H25						
		GND					F27						
		GND					B28	B6_B7					
		GND					B17						
		GND					B20						
		GND					B23						
		GND					B26						
		GND					E15	B7_B8					
		GND					E18						
		GND					E20						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		GND					E23						
		GND					B3	B8_B1					
		GND					B6						
		GND					B10						
		GND					B14						
		GND					E6	B8_B1					
		GND					E9						
		GND					E11						
		GND					E13						
		GND A1			U5	B2_B3	AB7	B2_B3					
		GND A2			F18	B6_B7	H22						
		GND A3			F5	B8_B1	G7	B8_B1					
		GND A4			U18	B4_B5	AB22	B4_B5					
		VCCINT			F7		AA10						
		VCCINT			F16		AA12						
		VCCINT			G10		AA14						
		VCCINT			G13		AA16						
		VCCINT			G14		AA18						
		VCCINT			G15		AA20						
		VCCINT			H8		H11						
		VCCINT			H11		H13						
		VCCINT			H12		H15						
		VCCINT			H15		H17						
		VCCINT			J7		H19						
		VCCINT			J9		H21						
		VCCINT			J10		H9						
		VCCINT			J11		J10						
		VCCINT			J12		J12						
		VCCINT			J13		J14						
		VCCINT			J14		J16						
		VCCINT			J16		J18						
		VCCINT			K7		J20						
		VCCINT			K9		J22						
		VCCINT			K14		J8						
		VCCINT			K16		K11						
		VCCINT			L8		K13						
		VCCINT			L9		K15						
		VCCINT			L14		K17						
		VCCINT			L15		K19						
		VCCINT			M8		K21						
		VCCINT			M9		K7						
		VCCINT			M14		K9						
		VCCINT			M15		L10						
		VCCINT			M17		L12						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		VCCINT			N7		L14						
		VCCINT			N9		L16						
		VCCINT			N14		L18						
		VCCINT			N16		L20						
		VCCINT			P6		L22						
		VCCINT			P7		L8						
		VCCINT			P9		M11						
		VCCINT			P10		M13						
		VCCINT			P11		M15						
		VCCINT			P12		M17						
		VCCINT			P13		M19						
		VCCINT			P14		M21						
		VCCINT			P16		M7						
		VCCINT			R6		M9						
		VCCINT			R8		N10						
		VCCINT			R11		N12						
		VCCINT			R12		N14						
		VCCINT			R15		N16						
		VCCINT			T7		N18						
		VCCINT			T8		N20						
		VCCINT			T10		N8						
		VCCINT			U7		P11						
		VCCINT			U16		P13						
		VCCINT			J5		P15						
		VCCINT			H6		P17						
		VCCINT			N5		P19						
		VCCINT			P5		P21						
		VCCINT			L6		P7						
		VCCINT			R4		P9						
		VCCINT			M6		R10						
		VCCINT			V10		R12						
		VCCINT			T9		R14						
		VCCINT			U11		R16						
		VCCINT			V9		R18						
		VCCINT			V13		R20						
		VCCINT			T13		R22						
		VCCINT			T14		R8						
		VCCINT			V14		T11						
		VCCINT			U12		T13						
		VCCINT			T15		T15						
		VCCINT			V16		T17						
		VCCINT			N18		T19						
		VCCINT			P18		T21						
		VCCINT			R19		T7						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		VCCINT			R17		T9						
		VCCINT			L19	B5_B6	U10						
		VCCINT			L17		U12						
		VCCINT			J18		U14						
		VCCINT			H17		U16						
		VCCINT			E13		U18						
		VCCINT			E14		U20						
		VCCINT			F12		U22						
		VCCINT			E16		U6						
		VCCINT			E18	B6_B7	U8						
		VCCINT			D18	B6_B7	V11						
		VCCINT			F11		V13						
		VCCINT			E10		V15						
		VCCINT			E9		V17						
		VCCINT			G8		V19						
		VCCINT			G9		V21						
		VCCINT			E7		V7						
		VCCINT					V9						
		VCCINT					W10						
		VCCINT					W12						
		VCCINT					W14						
		VCCINT					W16						
		VCCINT					W18						
		VCCINT					W20						
		VCCINT					W22						
		VCCINT					W8						
		VCCINT					Y11						
		VCCINT					Y13						
		VCCINT					Y15						
		VCCINT					Y17						
		VCCINT					Y19						
		VCCINT					Y21						
		VCCINT					Y7						
		VCCINT					Y9						
		VCCIO1			D3	B8_B1	C2						
		VCCIO1			G4	B1	F3						
		VCCIO1			L3	B1_B2	H5						
		VCCIO1					L3						
		VCCIO1					N5	B1					
		VCCIO2			N4		AC3						
		VCCIO2			T4		AF2	B2_B3					
		VCCIO2			W3	B2_B3	R3	B1_B2					
		VCCIO2					V3						
		VCCIO2					Y5						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		VCCIO3			AA4		AC11						
		VCCIO3			W10		AC13						
		VCCIO3			W8		AC5	B2_B3					
		VCCIO3					AC8						
		VCCIO3					AF10						
		VCCIO3					AF14						
		VCCIO3					AF3	B2_B3					
		VCCIO3					AF7						
		VCCIO4			AA19		AC18						
		VCCIO4			W13		AC20						
		VCCIO4			W15		AC23	B4_B5					
		VCCIO4					AD15	B3_B4					
		VCCIO4					AF17						
		VCCIO4					AF19						
		VCCIO4					AF23						
		VCCIO4					AF26	B4_B5					
		VCCIO5			N19		AC26						
		VCCIO5			T19		AG27	B4_B5					
		VCCIO5			W20	B4_B5	T24						
		VCCIO5					V26						
		VCCIO5					Y24						
		VCCIO6			D20	B6_B7	C27	B6_B7					
		VCCIO6			G19		F26	B6_B7					
		VCCIO6			L20	B5_B6	H24						
		VCCIO6					L26						
		VCCIO6					N24						
		VCCIO7			B19		C17						
		VCCIO7			D13		C20						
		VCCIO7			D15		C23						
		VCCIO7					C26	B6_B7					
		VCCIO7					F15	B7_B8					
		VCCIO7					F18						
		VCCIO7					F20						
		VCCIO7					F23	B6_B7					
		VCCIO8			B4		C10						
		VCCIO8			D10		C14						
		VCCIO8			D8		C3	B8_B1					
		VCCIO8					C6						
		VCCIO8					F11						
		VCCIO8					F13						
		VCCIO8					F6	B8_B1					
		VCCIO8					F9						
		VCCA1			U6	B2_B3	AA7	B2_B3					
		VCCA2			G18		H23						



Pin Information for the CycloneIII LS EP3CLS200 Device
Version 1.1
Notes (1), (2)

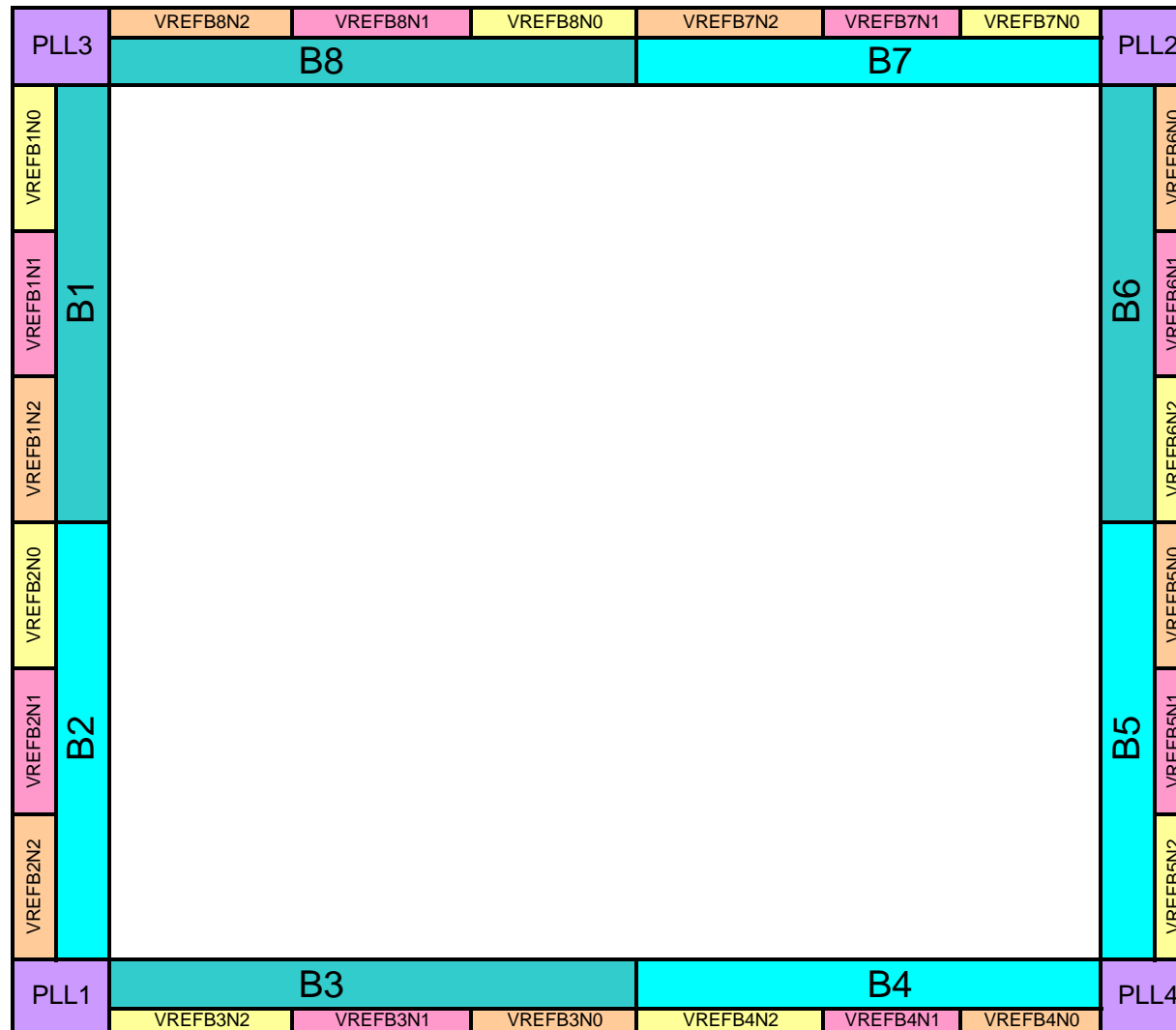
Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484	Pin Used for Bank Isolation F484	F780	Pin Used for Bank Isolation F780	DQS for x8/x9 in F484	DQS for x16/x18 in F484	DQS for x8/x9 in F780	DQS for x16/x18 in F780	DQS for x32/x36 in F780
		VCCA3			F6	B8_B1	H7						
		VCCA4			U17	B4_B5	AA22						
		VCCD_PLL1			V5	B2_B3	AB8						
		VCCD_PLL2			F17	B6_B7	G22	B6_B7					
		VCCD_PLL3			E5	B8_B1	G8	B8_B1					
		VCCD_PLL4			V18	B4_B5	AB23	B4_B5					
		VCCBAT			V6		AC7						
		NC					R1	B1_B2					
		NC					R4	B1_B2					
		NC					G15	B7_B8					

Notes:

- (1) If the p pin or n pin of the particular differential pair is not available for that package, this means that the particular differential pair is not supported.
- (2) For DQS pins that do not have associated DQ pins, the particular DQS is not supported.

Notes for isolation columns

Note	Details
B1	Pins used for setting up the security boundary for TDI, TDO and UDATA0
B1_B2	Physical Pins that used to turn on the security boundary between Bank B1 and Bank B2.
B2_B3	Physical Pins that used to turn on the security boundary between Bank B2 and Bank B3.
B3_B4	Physical Pins that used to turn on the security boundary between Bank B3 and Bank B4.
B4_B5	Physical Pins that used to turn on the security boundary between Bank B4 and Bank B5.
B5_B6	Physical Pins that used to turn on the security boundary between Bank B5 and Bank B6.
B6_B7	Physical Pins that used to turn on the security boundary between Bank B6 and Bank B7.
B7_B8	Physical Pins that used to turn on the security boundary between Bank B7 and Bank B8.
B8_B1	Physical Pins that used to turn on the security boundary between Bank B8 and Bank B1.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to provide an idea of placement on the device.
Refer to the pin list and the Quartus[®] II software for exact locations.



**Pin Information for the Cyclone III LS EP3CLS200 Device
Version 1.1**

Version Number	Date	Changes Made
1.0	6/26/2009	Initial release
1.1	10/10/2013	Removed Pin Definitions table.