Pin Information for the Cyclone® III EP3C5 Device
Version 1.4
Notes (1), (2)

Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (3)	M164	F256/ U256	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X16/X18 in F256/U256
B1	VREFB1N0	IO			1	B2	D4			
B1	VREFB1N0	IO			2	B1	E5			
B1	VREFB1N0	IO			3	A1	F5			
B1	VREFB1N0	IO			4	C1	B1			DQS2L/CQ3L
B1	VREFB1N0	VCCINT			5					
B1	VREFB1N0	IO	DIFFIO_L1p				C2			
B1	VREFB1N0	IO	DIFFIO_L1n	DATA1, ASDO	6	D2	C1			
B1	VREFB1N0	IO	VREFB1N0		7	D1	F3			
B1	VREFB1N0	IO	DIFFIO_L2p	FLASH_nCE, nCSO	8	E1	D2			
B1	VREFB1N0	IO	DIFFIO_L2n				D1			
B1	VREFB1N0	nSTATUS		nSTATUS	9	E2	F4			
B1	VREFB1N0	IO					G5			
B1	VREFB1N0	IO	DIFFIO_L3p				F2			
B1	VREFB1N0	IO	DIFFIO_L3n				F1			
B1	VREFB1N0	IO	DIFFIO_L4p		10	F2	G2	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0
B1	VREFB1N0	IO	DIFFIO_L4n		11	F1	G1			
B1	VREFB1N0	DCLK		DCLK	12	F3	H1			
B1	VREFB1N0	IO		DATA0	13	G1	H2			
B1	VREFB1N0	nCONFIG		nCONFIG	14	G2	H5			
B1	VREFB1N0	TDI		TDI	15	G3	H4			
B1	VREFB1N0	TCK		TCK	16	H2	H3			
B1	VREFB1N0	VCCIO1			17					
B1	VREFB1N0	TMS		TMS	18	H1	J5			
B1	VREFB1N0	GND			19					
B1	VREFB1N0	TDO		TDO	20	H3	J4			
B1	VREFB1N0	nCE		nCE	21	H4	J3			
B1	VREFB1N0	CLK0	DIFFCLK_0p		22	J2	E2			
B1	VREFB1N0	CLK1	DIFFCLK_0n		23	J1	E1			
B2	VREFB2N0	CLK2	DIFFCLK_1p		24	K3	M2			
B2	VREFB2N0	CLK3	DIFFCLK_1n		25	J3	M1			
B2	VREFB2N0	IO	DIFFIO_L5p				J2			
B2	VREFB2N0	IO	DIFFIO_L5n				J1			
B2	VREFB2N0	IO					J6			
B2	VREFB2N0	VCCIO2			26					
B2	VREFB2N0	IO	DIFFIO_L6p				K6			
B2	VREFB2N0	GND			27					
B2	VREFB2N0	IO	DIFFIO_L6n		28	K1	L6			
B2	VREFB2N0	VCCINT			29					
B2	VREFB2N0	IO	DIFFIO_L7p				K2			
B2	VREFB2N0	IO	DIFFIO_L7n				K1			
B2	VREFB2N0	IO	DIFFIO_L8p		30	L2	L2	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1
B2	VREFB2N0	IO	DIFFIO_L8n			K2	L1			
B2	VREFB2N0	IO	VREFB2N0		31	L1	L3			
B2	VREFB2N0	IO	DIFFIO_L9p			L3	N2			
B2	VREFB2N0	IO	DIFFIO_L9n				N1			

Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (3)	M164	F256/ U256	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X16/X18 in F256/U256
B2	VREFB2N0	IO	RUP1		32	M1	K5			
B2	VREFB2N0	IO	RDN1		33	M2	L4			
B2	VREFB2N0	IO			34	M3				
B2	VREFB2N0	IO					R1			DQS3L/CQ3L#
B2	VREFB2N0	IO	DIFFIO_L10p				P2			
B2	VREFB2N0	IO	DIFFIO_L10n				P1			
B2	VREFB2N0	VCCA1			35	R1	L5			
B2	VREFB2N0	GNDA1			36	P1	M5			
B2	VREFB2N0	VCCD_PLL1			37	P2	N4			
B3	VREFB3N0	IO	DIFFIO_B1p		38	R2	N3			
B3	VREFB3N0	IO	DIFFIO_B1n		39	R3	P3			DM5B1/BWS#5B1
B3	VREFB3N0	IO	DIFFIO_B2p			P3	R3			DQ5B
B3	VREFB3N0	IO	DIFFIO_B2n				T3			
B3	VREFB3N0	VCCIO3			40					
B3	VREFB3N0	GND			41					
B3	VREFB3N0	IO			42	R4	T2	DQS1B/CQ1B#, DPCLK2	DQS1B/CQ1B#, DPCLK2	DQS1B/CQ1B#, DPCLK2
B3	VREFB3N0	IO	PLL1_CLKOUTp		43	P5	R4			
B3	VREFB3N0	IO	PLL1_CLKOUTn		44	R5	T4			
B3	VREFB3N0	VCCINT			45					
B3	VREFB3N0	IO	DIFFIO_B4p				N5			DQ5B
B3	VREFB3N0	IO	DIFFIO_B4n				N6			DQ5B
B3	VREFB3N0	IO				P6	M6			DQ5B
B3	VREFB3N0	IO	VREFB3N0		46	N5	P6			
B3	VREFB3N0	VCCIO3			47					
B3	VREFB3N0	IO	DIFFIO_B5p				M7			DQS3B/CQ3B#
B3	VREFB3N0	GND			48					
B3	VREFB3N0	IO	DIFFIO_B5n				K8			
B3	VREFB3N0	IO	DIFFIO_B6p				R5			DQ5B
B3	VREFB3N0	IO	DIFFIO_B6n				T5			
B3	VREFB3N0	IO	DIFFIO_B7p				R6			DQ5B
B3	VREFB3N0	IO	DIFFIO_B7n				T6			
B3	VREFB3N0	IO					L7			DQ5B
B3	VREFB3N0	IO	DIFFIO_B8p				R7			DQ5B
B3	VREFB3N0	IO	DIFFIO_B8n				T7			DQS5B/CQ5B#
B3	VREFB3N0	IO	DIFFIO_B9p		49	R6	L8	DQ1B	DQ1B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B9n		50	R7	M8	DQ1B	DQ1B	DM5B0/BWS#5B0
B3	VREFB3N0	IO	DIFFIO_B10p		51	P7	N8	DQ1B	DQ1B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B10n				P8			DQ5B
B3	VREFB3N0	IO	DIFFIO_B11p		52	N6	R8			
B3	VREFB3N0	IO	DIFFIO_B11n		53	N7	T8			
B4	VREFB4N0	IO	DIFFIO_B12p		54	P8	R9			
B4	VREFB4N0	IO	DIFFIO_B12n		55	R8	T9			
B4	VREFB4N0	IO	DIFFIO_B13p				K9			
B4	VREFB4N0	IO	DIFFIO_B13n				L9			
B4	VREFB4N0	IO	DIFFIO_B14p				M9			
B4	VREFB4N0	VCCIO4			56					

Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (3)	M164	F256/ U256	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X16/X18 in F256/U256
B4	VREFB4N0	IO	DIFFIO_B14n				N9			DQ5B
B4	VREFB4N0	GND			57					
B4	VREFB4N0	IO	DIFFIO_B15p		58	R9	R10	DQ1B	DQ1B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B15n				T10			DQS4B/CQ5B
B4	VREFB4N0	IO	DIFFIO_B16p		59	N8	R11	DQ1B	DQ1B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B16n		60	P9	T11	DQ1B	DQ1B	
B4	VREFB4N0	VCCINT			61					
B4	VREFB4N0	IO	DIFFIO_B17p				R12			DQ5B
B4	VREFB4N0	IO	DIFFIO_B17n				T12			DQ5B
B4	VREFB4N0	VCCIO4			62					
B4	VREFB4N0	IO	DIFFIO_B18p				K10			
B4	VREFB4N0	GND			63					
B4	VREFB4N0	IO	DIFFIO_B18n				L10			
B4	VREFB4N0	IO			64	P10	P9			DQS2B/CQ3B
B4	VREFB4N0	IO	VREFB4N0		65	R10	P11			
B4	VREFB4N0	IO	DIFFIO_B19p			N11	R13			
B4	VREFB4N0	IO	DIFFIO_B19n			P11	T13			DQ5B
B4	VREFB4N0	IO	RUP2		66	N12	M10	DQ1B	DQ1B	
B4	VREFB4N0	IO	RDN2		67	P12	N11	DQ1B	DQ1B	
B4	VREFB4N0	IO	DIFFIO_B20p				T14			DQ5B
B4	VREFB4N0	IO	DIFFIO_B20n		68	R11	T15	DQS0B/CQ1B, DPCLK3	DQS0B/CQ1B, DPCLK3	DQS0B/CQ1B, DPCLK3
B4	VREFB4N0	IO			69	R12	R14			
B4	VREFB4N0	IO	DIFFIO_B21p		70	N10	P14			
B4	VREFB4N0	IO	DIFFIO_B21n		71		L11			
B4	VREFB4N0	IO	DIFFIO_B22p		72	R14	M11			
B4	VREFB4N0	IO	DIFFIO_B22n			R13	N12			
B5	VREFB5N0	IO			73	P14	N13			
B5	VREFB5N0	IO			74	P15	M12			
B5	VREFB5N0	IO			75	R15	L12			
B5	VREFB5N0	IO					K12			
B5	VREFB5N0	IO	RUP3		76	N15	N14			
B5	VREFB5N0	IO	RDN3		77	M14	P15			
B5	VREFB5N0	IO	DIFFIO_R11n				P16			DQS3R/CQ3R#
B5	VREFB5N0	IO	DIFFIO_R11p				R16			
B5	VREFB5N0	VCCINT			78					
B5	VREFB5N0	IO					K11			
B5	VREFB5N0	IO	DIFFIO_R10n		79	M15	N16			
B5	VREFB5N0	IO	DIFFIO_R10p			L14	N15			
B5	VREFB5N0	IO	VREFB5N0		80	L15	L14			
B5	VREFB5N0	IO					L13			
B5	VREFB5N0	IO	DIFFIO_R9n				L16			
B5	VREFB5N0	VCCIO5			81					
B5	VREFB5N0	IO	DIFFIO_R9p			K12	L15			
B5	VREFB5N0	GND			82					
B5	VREFB5N0	IO			83	K13	J11			
B5	VREFB5N0	IO	DIFFIO_R8n		84	J12	K16			

Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (3)	M164	F256/ U256	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X16/X18 in F256/U256
B5	VREFB5N0	IO	DIFFIO_R8p		85	K14	K15	DQS1R/CQ1R#, DPCLK4	DQS1R/CQ1R#, DPCLK4	DQS1R/CQ1R#, DPCLK4
B5	VREFB5N0	IO	DIFFIO_R7n	DEV_OE	86	K15	J16			
B5	VREFB5N0	IO	DIFFIO_R7p	DEV_CLRn	87	J13	J15			
B5	VREFB5N0	IO	DIFFIO_R6n				J14			
B5	VREFB5N0	IO	DIFFIO_R6p				J12			
B5	VREFB5N0	IO					J13			
B5	VREFB5N0	CLK7	DIFFCLK_3n		88	J15	M16			
B5	VREFB5N0	CLK6	DIFFCLK_3p		89	J14	M15			
B6	VREFB6N0	CLK5	DIFFCLK_2n		90	H15	E16			
B6	VREFB6N0	CLK4	DIFFCLK_2p		91	H14	E15			
B6	VREFB6N0	CONF_DONE		CONF_DONE	92	H13	H14			
B6	VREFB6N0	VCCIO6			93					
B6	VREFB6N0	MSEL0		MSEL0	94	G13	H13			
B6	VREFB6N0	GND			95					
B6	VREFB6N0	MSEL1		MSEL1	96	G14	H12			
B6	VREFB6N0	MSEL2		MSEL2	97	G15	G12			
B6	VREFB6N0	IO	DIFFIO_R5n				H16			
B6	VREFB6N0	IO	DIFFIO_R5p				H15			
B6	VREFB6N0	IO	DIFFIO_R4n	INIT_DONE	98	F13	G16			
B6	VREFB6N0	IO	DIFFIO_R4p	CRC_ERROR	99	F14	G15			
B6	VREFB6N0	IO			100	F15	F13			
B6	VREFB6N0	IO	DIFFIO_R3n	nCEO	101	E14	F16			
B6	VREFB6N0	VCCINT			102					
B6	VREFB6N0	IO	DIFFIO_R3p	CLKUSR	103	E15	F15			
B6	VREFB6N0	IO			104	D14	B16	DQS0R/CQ1R, DPCLK5	DQS0R/CQ1R, DPCLK5	DQS0R/CQ1R, DPCLK5
B6	VREFB6N0	IO	VREFB6N0		105	D15	F14			
B6	VREFB6N0	IO	DIFFIO_R2n				D16			
B6	VREFB6N0	IO	DIFFIO_R2p				D15			
B6	VREFB6N0	IO					G11			
B6	VREFB6N0	IO	DIFFIO_R1n		106	C15	C16			DQS2R/CQ3R
B6	VREFB6N0	IO	DIFFIO_R1p				C15			
B6	VREFB6N0	VCCA2			107	A15	F12			
B6	VREFB6N0	GNDA2			108	B15	E12			
B6	VREFB6N0	VCCD_PLL2			109	B14	D13			
B7	VREFB7N0	IO	DIFFIO_T21n				C14			
B7	VREFB7N0	IO	DIFFIO_T21p				D14			DQ5T
B7	VREFB7N0	IO	DIFFIO_T20n			B13	D11			
B7	VREFB7N0	IO	DIFFIO_T20p		110	A14	D12	DQS0T/CQ1T, DPCLK6	DQS0T/CQ1T, DPCLK6	DQS0T/CQ1T, DPCLK6
B7	VREFB7N0	IO	DIFFIO_T19n				A13			
B7	VREFB7N0	IO	DIFFIO_T19p		111	A13	B13			DQ5T
B7	VREFB7N0	IO	PLL2_CLKOUTn		112	B12	A14			
B7	VREFB7N0	IO	PLL2_CLKOUTp		113	A12	B14			
B7	VREFB7N0	IO	RUP4		114	B11	E11	DQ1T	DQ1T	
B7	VREFB7N0	IO	RDN4		115	A11	E10	DQ1T	DQ1T	

Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (3)	M164	F256/ U256	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X16/X18 in F256/U256
B7	VREFB7N0	VCCINT			116					
B7	VREFB7N0	IO	DIFFIO_T18n				A12			DQ5T
B7	VREFB7N0	IO	DIFFIO_T18p				B12			DQ5T
B7	VREFB7N0	VCCIO7			117					
B7	VREFB7N0	IO	DIFFIO_T17n				A11			DQ5T
B7	VREFB7N0	GND			118					
B7	VREFB7N0	IO	DIFFIO_T17p				B11			DQ5T
B7	VREFB7N0	IO	VREFB7N0		119	B10	C11			
B7	VREFB7N0	IO	DIFFIO_T16n		120	A10	F10	DQ1T	DQ1T	
B7	VREFB7N0	IO	DIFFIO_T16p		121	C9	F9			DQS2T/CQ3T
B7	VREFB7N0	IO	DIFFIO_T15n				F11			
B7	VREFB7N0	IO	DIFFIO_T15p				A15			
B7	VREFB7N0	IO	DIFFIO_T14n				A10			DQ5T
B7	VREFB7N0	VCCIO7			122					
B7	VREFB7N0	IO	DIFFIO_T14p				B10			DQ5T
B7	VREFB7N0	GND			123					
B7	VREFB7N0	IO	DIFFIO_T13n			D9	C9			DQ5T
B7	VREFB7N0	IO	DIFFIO_T13p		124	D8	D9			DM5T0/BWS#5T0
B7	VREFB7N0	IO			125	A9	E9			DQS4T/CQ5T
B7	VREFB7N0	IO	DIFFIO_T12n		126	B9	A9			
B7	VREFB7N0	IO	DIFFIO_T12p		127	A8	B9			
B8	VREFB8N0	IO	DIFFIO_T11n		128	B8	A8			
B8	VREFB8N0	IO	DIFFIO_T11p		129	A7	B8			
B8	VREFB8N0	VCCIO8			130					
B8	VREFB8N0	IO					C8			DQS5T/CQ5T#
B8	VREFB8N0	GND			131					
B8	VREFB8N0	IO					D8			DQ5T
B8	VREFB8N0	IO	DIFFIO_T10n	DATA2	132	C7	E8	DQ1T	DQ1T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T10p	DATA3	133	B7	F8	DQ1T	DQ1T	
B8	VREFB8N0	IO	DIFFIO_T9n			B6	A7			DQ5T
B8	VREFB8N0	IO	DIFFIO_T9p	DATA4		A6	B7		DQ1T	DQ5T
B8	VREFB8N0	VCCINT			134					
B8	VREFB8N0	IO	DIFFIO_T8n		135		F6	DQ1T		
B8	VREFB8N0	IO	DIFFIO_T8p				F7			
B8	VREFB8N0	IO	VREFB8N0		136	C6	C6			
B8	VREFB8N0	IO	DIFFIO_T7n				A6			DQS3T/CQ3T#
B8	VREFB8N0	IO	DIFFIO_T7p				B6			DQ5T
B8	VREFB8N0	IO		DATA5	137	A5	E7	DQ1T	DQ1T	DQ5T
B8	VREFB8N0	IO		DATA6	138	B4	E6			DQ5T
B8	VREFB8N0	IO	DIFFIO_T6n	DATA7		A4	A5			DQ5T
B8	VREFB8N0	VCCIO8			139					
B8	VREFB8N0	GND			140					
B8	VREFB8N0	IO	DIFFIO_T5n				A2			
B8	VREFB8N0	IO	DIFFIO_T5p		141	C4	B5			DQ5T
B8	VREFB8N0	IO	DIFFIO_T4n				A4			DM5T1/BWS#5T1
B8	VREFB8N0	IO	DIFFIO_T4p				B4			
B8	VREFB8N0	IO	DIFFIO_T3n				D5			

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B8	VREFB8N0	IO	DIFFIO_T3p				D6			
B8	VREFB8N0	IO	DIFFIO_T2n				A3			
B8	VREFB8N0	IO	DIFFIO_T2p		142	A3	B3	DQS1T/CQ1T#, DPCLK7	DQS1T/CQ1T#, DPCLK7	DQS1T/CQ1T#, DPCLK7
B8	VREFB8N0	IO	DIFFIO_T1n		143	A2	C3	DQ1T	DQ1T	
B8	VREFB8N0	IO	DIFFIO_T1p		144	B3	D3	DM1T	DM1T	
		VCCINT				D3	G6			
		VCCINT				D6	G7			
		VCCINT				N2	G8			
		VCCINT				D10	G9			
		VCCINT				F12	G10			
		VCCINT				H12	H6			
		VCCINT				M8	H11			
		VCCINT				M11	K7			
		VCCIO1				F4	E3			
		VCCIO1					G3			
		VCCIO2				J4	K3			
		VCCIO2					M3			
		VCCIO3				M5	P4			
		VCCIO3				M6	P7			
		VCCIO3					T1			
		VCCIO4				M9	P10			
		VCCIO4				N9	P13			
		VCCIO4					T16			
		VCCIO5				L13	K14			
		VCCIO5					M14			
		VCCIO6				D13	E14			
		VCCIO6					G14			
		VCCIO7				C10	A16			
		VCCIO7				C11	C10			
		VCCIO7					C13			
		VCCIO8				B5	A1			
		VCCIO8				C5	C4			
		VCCIO8					C7			
		GND				E3	H7			
		GND				G12	H8			
		GND				D7	H9			
		GND				N14	H10			
		GND				M7	J7			
		GND				N1	J8			
		GND				P13	J9			
		GND				P4	J10			
		GND				K4	B2			
		GND				N4	B15			
		GND				G4	C5			
		GND				D5	C12			
		GND				C12	D7			

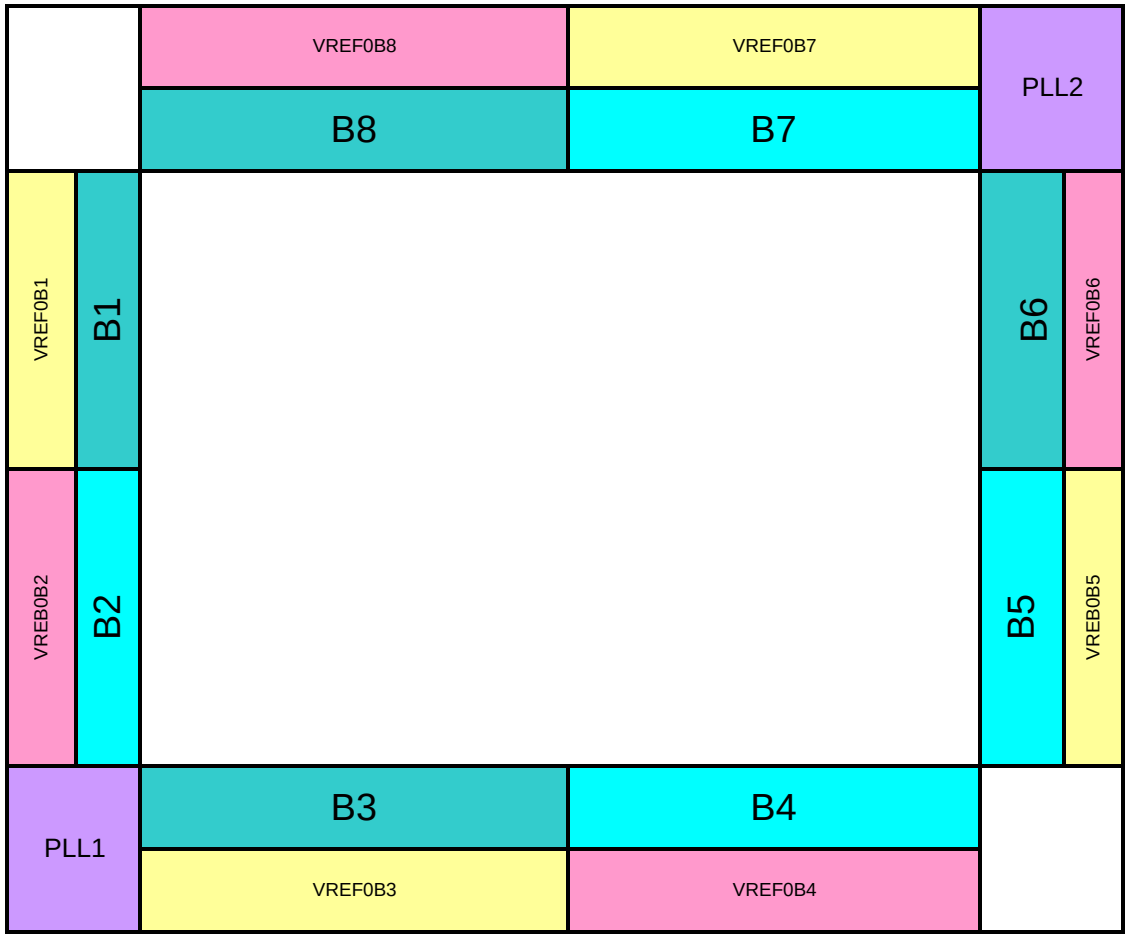
Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (3)	M164	F256/ U256	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X16/X18 in F256/U256
		GND				D11	D10			
		GND				C14	E4			
		GND				M13	E13			
		GND				M10	G4			
		GND				C2	G13			
		GND				C8	K4			
		GND				E13	K13			
		GND					M4			
		GND					M13			
		GND					N7			
		GND					N10			
		GND					P5			
		GND					P12			
		GND					R2			
		GND					R15			

Notes:

(1) If the p pin or n pin is not available for the package, this means that the particular differential pair is not supported.

(2) DQS pins that do not have the associated DQ pins are not supported.

(3) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. This exposed pad is used for electrical connectivity, and not for thermal purposes.



Notes:

(1) This is a top view of the silicon die.

(2) This is only a pictorial representation to get an idea of placement on the device.
Refer to the pin list and the Quartus® II software for exact locations.

Pin Information for the Cyclone® III EP3C5 Device
Version 1.4

Version Number	Changes Made	Date
1.0	Initial release.	5/24/2007
1.1	Added support for M164 package.	11/23/2007
1.2	- Updated pin function for CRC_ERROR pin. - Updated DQ/DQS support for UBGA package. - Updated pin function for PLL[1..4]_CLKOUT[p,n] pin. - Remove RDY from Pin Definitions worksheet. - Incorporated pin connection guideline into Pin Definitions worksheet. - Incorporated VCCA and VCCD Decoupling recommendations.	5/9/2008
1.3	- Removed Pin Connection Guideline from Pin Definitions worksheet. - Removed VCCA and VCCD Decoupling recommendations. - Removed PKG notes from Pin List Worksheet. - Updated pin function for DCLK pin.	10/7/2009
1.4	Removed Pin Definitions table.	10/10/2013