Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
B1	VREF0B1	GND						
B1	VREF0B1	IO	LVDS31p	INIT_DONE	C3	C3		
B1	VREF0B1	IO	LVDS31n	CRC_ERROR	C2	C2		
B1	VREF0B1	IO	LVDS30p	CLKUSR	D3	D3		
B1	VREF0B1	IO	LVDS30n		D2	D2		
B1	VREF0B1	IO	VREF0B1		D4	D4		
B1	VREF0B1	IO			D1	D1		
B1	VREF0B1	IO	LVDS29p		E3	E4	DQ0L0	DQ0L0
B1	VREF0B1	VCCIO1						
B1	VREF0B1	IO	LVDS29n		E2	E5	DQ0L1	DQ0L1
B1	VREF0B1	IO	DPCLK1		F1	F3	DQS0L	DQS0L
B1	VREF0B1	IO	LVDS28p		E4	E3	DQ0L2	DQ0L2
B1	VREF0B1	IO	LVDS28n		E5	E2	DQ0L3	DQ0L3
B1	VREF0B1	IO	LVDS27p		F2	F4		
B1	VREF0B1	IO	LVDS27n		F3	F5		
B1	VREF0B1	IO	LVDS26p		F4	F2		
B1	VREF0B1	IO	LVDS26n		F5	F1		
B1	VREF0B1	IO	LVDS25n		G2	G5		
B1	VREF0B1	IO	LVDS25p		G1	F6		
B1	VREF0B1	IO	LVDS24p		F6	G1		
B1	VREF0B1	GND						
B1	VREF0B1	IO	LVDS24n		F7	G2		
B1	VREF0B1	IO	LVDS23n		G4	G7	DQ0L4	DQ0L4
B1	VREF0B1	IO	LVDS23p		G3	G6		
B1	VREF0B1	VCCIO1						
B1	VREF0B1	IO	LVDS22p		G5	G3	DQ0L5	DQ0L5
B1	VREF0B1	IO	LVDS22n		G6	G4	DQ0L6	DQ0L6
B1	VREF0B1	IO			H1	H7	DQ0L7	DQ0L7
B1	VREF1B1	IO	LVDS21p		H2	H1		
B1	VREF1B1	IO	LVDS21n		H3	H2		
B1	VREF1B1	IO	LVDS20p		H4	H3		
B1	VREF1B1	IO	LVDS20n		H5	H4	DM0L	DM0L
B1	VREF1B1	IO	LVDS19p			J1		
B1	VREF1B1	IO	LVDS19n			J2		
B1	VREF1B1	IO	LVDS18n			H6		
B1	VREF1B1	IO	LVDS18p			H5		
B1	VREF1B1	GND						
B1	VREF1B1	IO	LVDS17p			J3		
B1	VREF1B1	IO	LVDS17n			J4		
B1	VREF1B1	IO	LVDS16p			J5		
B1	VREF1B1	VCCIO1						
B1	VREF1B1	IO	LVDS16n			J6		
B1	VREF1B1	IO				J7		
B1	VREF1B1	IO	VREF1B1		H6	J8		
	VREF1B1	VCCA_PLL1			J5	K4		
B1	VREF1B1	DATA0		DATA0	H7	K3		
B1	VREF1B1	nCONFIG		nCONFIG	J2	K1		
B1	VREF1B1	IO		nCSO	J1	K2		
B1	VREF1B1	nCEO		nCEO	K2	L2		
B1	VREF1B1	nCE		nCE	J7	L5		
B1	VREF1B1	CLK0	LVDSCLK1p		J3	K5		
B1	VREF1B1	MSEL0		MSEL0	K3	L1		
	VREF1B1	GNDA_PLL1			K1	K7		
B1	VREF1B1	MSEL1		MSEL1	K7	L6		
B1	VREF1B1	CLK1	LVDSCLK1n		J4	K6		
B1	VREF1B1	DCLK		DCLK	L1	L3		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
	VREF1B1	GNDG_PLL1			J6	L7		
B1	VREF1B1	IO		ASDO	K6	L4		
B1	VREF1B1	IO	PLL1_OUTp		K4	L8		
B1	VREF1B1	IO	PLL1_OUTn		K5	M8		
B1	VREF1B1	IO	LVDS15p			M2		
B1	VREF1B1	IO	LVDS15n			M1		
B1	VREF1B1	IO	LVDS14n			M6		
B1	VREF1B1	IO	LVDS14p			M5		
B1	VREF1B1	GND						
B1	VREF1B1	IO	LVDS13p			M4		
B1	VREF1B1	IO	LVDS13n			M3		
B1	VREF1B1	IO	LVDS12n		L6	N6		
B1	VREF1B1	VCCIO1						
B1	VREF1B1	IO	LVDS12p		L7	M7	DM1L	DM1L
B1	VREF1B1	IO	LVDS11p		L2	N1		
B1	VREF1B1	IO	LVDS11n		L3	N2		
B1	VREF1B1	IO	LVDS10p		L5	N4		
B1	VREF1B1	IO	LVDS10n		L4	N3		
B1	VREF2B1	IO			M1	N5	DQ1L0	DQ1L0
B1	VREF2B1	IO	LVDS9p			N7		
B1	VREF2B1	IO	LVDS9n			P7		
B1	VREF2B1	IO	LVDS8p		M3	P2	DQ1L1	DQ1L1
B1	VREF2B1	IO	LVDS8n		M2	P1	DQ1L2	DQ1L2
B1	VREF2B1	IO	LVDS7p		M5	P6	DQ1L3	DQ1L3
B1	VREF2B1	GND						
B1	VREF2B1	IO	LVDS7n		M4	P5		
B1	VREF2B1	IO	LVDS6p		N1	P3		
B1	VREF2B1	IO	LVDS6n		N2	P4		
B1	VREF2B1	VCCIO1						
B1	VREF2B1	IO	LVDS5p		M6	R1		
B1	VREF2B1	IO	LVDS5n		N7	R2		
B1	VREF2B1	IO	LVDS4p		N5	R6		
B1	VREF2B1	IO	LVDS4n		N6	R5		
B1	VREF2B1	IO	LVDS3p		N3	R3	DQ1L4	DQ1L4
B1	VREF2B1	IO	LVDS3n		N4	R4	DQ1L5	DQ1L5
B1	VREF2B1	IO	DPCLK0		P5	T4	DQS1L	DQS1L
B1	VREF2B1	IO	LVDS2p		P2	T2	DQ1L6	DQ1L6
B1	VREF2B1	IO	LVDS2n		P3	T3	DQ1L7	DQ1L7
B1	VREF2B1	IO	VREF2B1		R1	U1		
B1	VREF2B1	IO			P4	U4		
B1	VREF2B1	IO	LVDS1p		R2	U2		
B1	VREF2B1	IO	LVDS1n		R3	U3		
B1	VREF2B1	IO	LVDS0p		T2	V2		
B1	VREF2B1	IO	LVDS0n		T3	V3		
B1	VREF2B1	GND						
B1	VREF2B1	VCCIO1						
B4	VREF2B4	IO	LVDS128p		U3	W3		
B4	VREF2B4	IO	LVDS128n		V4	Y4		
B4	VREF2B4	IO	LVDS127p		T4	V4		
B4	VREF2B4	IO	LVDS127n		U4	W4		
B4	VREF2B4	VCCIO4						
B4	VREF2B4	IO	LVDS126p		T5	T5	DQ1B7	DQ1B7
B4	VREF2B4	IO	LVDS126n		U5	U5	DQ1B6	DQ1B6
B4	VREF2B4	IO	LVDS125p		M8	V5		
B4	VREF2B4	GND						
B4	VREF2B4	IO	LVDS125n		N8	W5		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
B4	VREF2B4	IO	DPCLK7		R4	T6	DQS1B	DQS1B
B4	VREF2B4	IO	VREF2B4		R5	T7		
B4	VREF2B4	IO	LVDS124p		V6	W6		
B4	VREF2B4	IO	LVDS124n		U6	Y6	DQ1B5	DQ1B5
B4	VREF2B4	IO	LVDS123p		P6	U6	DQ1B4	DQ1B4
	VREF2B4	GND						
B4	VREF2B4	IO	LVDS123n		P7	V6		
B4	VREF2B4	IO	LVDS122p		T6	W7		
B4	VREF2B4	IO	LVDS122n		R6	Y7		
B4	VREF2B4	IO	LVDS121p		U7	R7	DQ1B3	DQ1B3
B4	VREF2B4	IO	LVDS121n		V7	T8	DQ1B2	DQ1B2
B4	VREF2B4	IO	LVDS120p		T7	V7	DQ1B1	DQ1B1
B4	VREF2B4	VCCIO4						
B4	VREF2B4	IO	LVDS120n		R7	U7	DQ1B0	DQ1B0
B4	VREF1B4	IO	LVDS119p		U8	V8		
B4	VREF1B4	IO	LVDS119n		V8	U8		
B4	VREF1B4	GND						
B4	VREF1B4	IO	LVDS118p		T8	W8		
B4	VREF1B4	IO	LVDS118n		R8	Y8		
B4	VREF1B4	IO	LVDS117p		U9	U9		
	VREF1B4	GND						
B4	VREF1B4	IO	LVDS117n		V9	V9		
B4	VREF1B4	IO	LVDS116p		R9	T9	DM1B	DM1B
B4	VREF1B4	IO	LVDS116n		T9	R9		
B4	VREF1B4	IO	LVDS115p		M9	Y9		
B4	VREF1B4	IO	LVDS115n		N9	W9		
B4	VREF1B4	IO	LVDS114p			T10		
B4	VREF1B4	IO	LVDS114n			U10		
B4	VREF1B4	IO	VREF1B4		P9	V10		
B4	VREF1B4	IO	LVDS113p			W10		
B4	VREF1B4	IO	LVDS113n			Y10		
B4	VREF1B4	VCCIO4						
B4	VREF1B4	IO	LVDS112p		U10	V11		
B4	VREF1B4	IO	LVDS112n		V10	U11		
B4	VREF1B4	IO	LVDS111p		T10	W11		
B4	VREF1B4	GND						
B4	VREF1B4	IO	LVDS111n		R10	Y11		
B4	VREF1B4	IO				R11		
B4	VREF1B4	IO	LVDS110p			Y12		
	VREF1B4	GND						
B4	VREF1B4	IO	LVDS110n		P10	W12		
B4	VREF1B4	IO	LVDS109p		R11	T11		
B4	VREF1B4	IO	LVDS109n		T11	T12		
B4	VREF1B4	IO	LVDS108p		U11	U12	DM0B	DM0B
B4	VREF1B4	IO	LVDS108n		V11	V12		
B4	VREF1B4	IO	LVDS107p		V12	T13		
	VREF1B4	GND						
B4	VREF1B4	IO	LVDS107n		U12	R13		
B4	VREF0B4	IO	LVDS106p		T12	Y13	DQ0B7	DQ0B7
B4	VREF0B4	IO	LVDS106n		R12	W13	DQ0B6	DQ0B6
B4	VREF0B4	VCCIO4						
B4	VREF0B4	IO	LVDS105p		V13	U13	DQ0B5	DQ0B5
B4	VREF0B4	IO	LVDS105n		U13	V13	DQ0B4	DQ0B4
B4	VREF0B4	IO	LVDS104p		T13	R14		
B4	VREF0B4	GND						
B4	VREF0B4	IO	LVDS104n		R13	T14		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
B4	VREF0B4	IO	LVDS103p		N10	W14		
B4	VREF0B4	IO	LVDS103n		M10	Y14		
B4	VREF0B4	IO	LVDS102p			U14		
B4	VREF0B4	IO	LVDS102n			V14		
B4	VREF0B4	IO	LVDS101p			V15		
	VREF0B4	GND						
B4	VREF0B4	IO	LVDS101n		P12	U15		
B4	VREF0B4	IO	VREF0B4		P13	Y15		
B4	VREF0B4	IO	DPCLK6		U14	W15	DQS0B	DQS0B
B4	VREF0B4	IO	LVDS100p		N11	T15		
B4	VREF0B4	IO	LVDS100n		M11	T16		
B4	VREF0B4	IO	LVDS99p		T14	W16	DQ0B3	DQ0B3
B4	VREF0B4	VCCIO4						
B4	VREF0B4	IO	LVDS99n		R14	V16	DQ0B2	DQ0B2
B4	VREF0B4	IO	LVDS98p		V15	V17	DQ0B1	DQ0B1
B4	VREF0B4	IO	LVDS98n		U15	U16	DQ0B0	DQ0B0
B4	VREF0B4	GND						
B4	VREF0B4	IO	LVDS97p		U16	Y17		
B4	VREF0B4	IO	LVDS97n		T15	W17		
	VREF0B4	GND						
B3	VREF2B3	GND						
B3	VREF2B3	IO	LVDS96n		T16	W18		
B3	VREF2B3	IO	LVDS96p		T17	V18		
B3	VREF2B3	IO	LVDS95n		R17	V19		
B3	VREF2B3	IO	LVDS95p		R18	U20		
B3	VREF2B3	IO	LVDS94n		R15	U18	DQ1R7	DQ1R7
B3	VREF2B3	IO	LVDS94p		R16	U19		
B3	VREF2B3	IO	VREF2B3		P16	U17		
B3	VREF2B3	VCCIO3						
B3	VREF2B3	IO			P17	T18	DQ1R6	DQ1R6
B3	VREF2B3	IO	DPCLK5		P15	T19	DQS1R	DQS1R
B3	VREF2B3	IO	LVDS93n		P14	T17	DQ1R5	DQ1R5
B3	VREF2B3	IO	LVDS93p		N14	R16	DQ1R4	DQ1R4
B3	VREF2B3	IO	LVDS92n		N18	R19		
B3	VREF2B3	IO	LVDS92p		N17	R20		
B3	VREF2B3	IO	LVDS91n		N13	R17		
B3	VREF2B3	IO	LVDS91p		N12	R18		
B3	VREF2B3	IO	LVDS90n		N16	R15		
B3	VREF2B3	IO	LVDS90p		N15	P14		
B3	VREF2B3	IO	LVDS89n		M18	P18		
B3	VREF2B3	GND						
B3	VREF2B3	IO	LVDS89p		M17	P17	DQ1R3	DQ1R3
B3	VREF2B3	IO	LVDS88p		M15	P15	DQ1R1	DQ1R1
B3	VREF2B3	IO	LVDS88n		M14	P16	DQ1R2	DQ1R2
B3	VREF2B3	VCCIO3						
B3	VREF2B3	IO	LVDS87n			P19		
B3	VREF2B3	IO	LVDS87p			P20		
B3	VREF2B3	IO			M16	N14	DQ1R0	DQ1R0
B3	VREF1B3	IO	LVDS86n		L18	N18		
B3	VREF1B3	IO	LVDS86p		L17	N17		
B3	VREF1B3	IO	LVDS85n		M13	N19		
B3	VREF1B3	IO	LVDS85p		L13	N20		
B3	VREF1B3	IO	LVDS84p		L15	N15		
B3	VREF1B3	IO	LVDS84n		L16	N16	DM1R	DM1R
B3	VREF1B3	IO	LVDS83n			M18		
B3	VREF1B3	IO	LVDS83p			M17		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
B3	VREF1B3	GND						
B3	VREF1B3	IO	LVDS82p			M16		
B3	VREF1B3	IO	LVDS82n			M15		
B3	VREF1B3	IO	LVDS81n			M20		
B3	VREF1B3	VCCIO3						
B3	VREF1B3	IO	LVDS81p			M19		
B3	VREF1B3	IO			L14	M14		
B3	VREF1B3	IO	PLL2_OUTp		K15	L13		
	VREF1B3	GNDG_PLL2			J18	L15		
B3	VREF1B3	IO	PLL2_OUTn		K16	M13		
B3	VREF1B3	CLK3	LVDSCLK2n		J16	K14		
B3	VREF1B3	CONF_DONE		CONF_DONE	K17	L18		
	VREF1B3	GNDA_PLL2			K12	K20		
B3	VREF1B3	nSTATUS		nSTATUS	L12	L17		
B3	VREF1B3	CLK2	LVDSCLK2p		J15	L14		
B3	VREF1B3	TCK		TCK	K18	L19		
B3	VREF1B3	TMS		TMS	K14	L16		
B3	VREF1B3	IO	VREF1B3		J14	K19		
B3	VREF1B3	TDO		TDO	K13	L20		
B3	VREF1B3	TDI		TDI	J17	K18		
	VREF1B3	VCCA_PLL2			J12	K17		
B3	VREF1B3	IO				J13		
B3	VREF1B3	IO	LVDS80p			K15		
B3	VREF1B3	IO	LVDS80n			K16		
B3	VREF1B3	IO	LVDS79n			J18		
B3	VREF1B3	IO	LVDS79p			J17		
B3	VREF1B3	IO	LVDS78n			J14		
B3	VREF1B3	IO	LVDS78p			H14		
B3	VREF1B3	GND						
B3	VREF1B3	IO	LVDS77n			J20		
B3	VREF1B3	IO	LVDS77p			J19		
B3	VREF1B3	IO	LVDS76n		J13	J15		
B3	VREF1B3	VCCIO3						
B3	VREF1B3	IO	LVDS76p		H13	J16	DM0R	DM0R
B3	VREF1B3	IO	LVDS75n		H14	H20		
B3	VREF1B3	IO	LVDS75p		H15	H19		
B3	VREF1B3	IO	LVDS74n		H16	H17		
B3	VREF1B3	IO	LVDS74p		H17	H18		
B3	VREF0B3	IO			H18	H16	DQ0R7	DQ0R7
B3	VREF0B3	IO	LVDS73n		G18	G17	DQ0R6	DQ0R6
B3	VREF0B3	IO	LVDS73p		G17	G18	DQ0R5	DQ0R5
B3	VREF0B3	IO	LVDS72n		G13	H15	DQ0R4	DQ0R4
B3	VREF0B3	IO	LVDS72p		G14	G14		
B3	VREF0B3	IO	LVDS71n		G15	G19		
B3	VREF0B3	GND						
B3	VREF0B3	IO	LVDS71p		G16	G20		
B3	VREF0B3	IO	LVDS70n		G12	G15		
B3	VREF0B3	IO	LVDS70p		F12	G16		
B3	VREF0B3	VCCIO3						
B3	VREF0B3	IO	LVDS69p		F17	F19		
B3	VREF0B3	IO	LVDS69n		F18	F20		
B3	VREF0B3	IO	LVDS68p		F14	F16		
B3	VREF0B3	IO	LVDS68n		F13	F15		
B3	VREF0B3	IO	LVDS67n		F16	E19		
B3	VREF0B3	IO	LVDS67p		F15	E18	DQ0R3	DQ0R3
B3	VREF0B3	IO	DPCLK4		E17	F18	DQS0R	DQS0R

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
B3	VREF0B3	IO	LVDS66n		E16	F17	DQ0R2	DQ0R2
B3	VREF0B3	IO	LVDS66p		E15	E17	DQ0R1	DQ0R1
B3	VREF0B3	IO			D18	D20	DQ0R0	DQ0R0
B3	VREF0B3	IO	VREF0B3		E14	D17		
B3	VREF0B3	IO	LVDS65n		D16	D19		
B3	VREF0B3	IO	LVDS65p		D15	D18		
B3	VREF0B3	IO	LVDS64n		C17	C19		
B3	VREF0B3	IO	LVDS64p		D17	C18		
B3	VREF0B3	GND						
B3	VREF0B3	VCCIO3						
	VREF0B2	GND						
B2	VREF0B2	IO	LVDS63n		C16	C17		
B2	VREF0B2	IO	LVDS63p		B16	B18		
B2	VREF0B2	VCCIO2						
B2	VREF0B2	IO	LVDS62n		B15	B17	DQ0T0	DQ0T0
B2	VREF0B2	IO	LVDS62p		A15	A17	DQ0T1	DQ0T1
B2	VREF0B2	IO	LVDS61n		C15	C16	DQ0T2	DQ0T2
B2	VREF0B2	GND						
B2	VREF0B2	IO	LVDS61p		D14	B16	DQ0T3	DQ0T3
B2	VREF0B2	IO	LVDS60n		G11	D16		
B2	VREF0B2	IO	LVDS60p		F11	E16		
B2	VREF0B2	IO	DPCLK3		B14	C15	DQS0T	DQS0T
B2	VREF0B2	IO	VREF0B2		C14	D15		
B2	VREF0B2	IO	LVDS59n		E13	B15		
	VREF0B2	GND						
B2	VREF0B2	IO	LVDS59p			A15		
B2	VREF0B2	IO	LVDS58n		G10	E15		
B2	VREF0B2	IO	LVDS58p		F10	F14		
B2	VREF0B2	IO	LVDS57n			A14		
B2	VREF0B2	IO	LVDS57p			B14		
B2	VREF0B2	IO	LVDS56n		B13	E14		
B2	VREF0B2	VCCIO2						
B2	VREF0B2	IO	LVDS56p		A13	E13		
B2	VREF0B2	IO	LVDS55n		D13	C14	DQ0T4	DQ0T4
B2	VREF0B2	IO	LVDS55p		C13	D14	DQ0T5	DQ0T5
B2	VREF0B2	GND						
B2	VREF0B2	IO	LVDS54n		D12	A13	DQ0T6	DQ0T6
B2	VREF0B2	IO	LVDS54p		C12	B13	DQ0T7	DQ0T7
B2	VREF1B2	IO	LVDS53n		B12	C13		
	VREF1B2	GND						
B2	VREF1B2	IO	LVDS53p		A12	D13		
B2	VREF1B2	IO	LVDS52n		C11	E12		
B2	VREF1B2	IO	LVDS52p		D11	F12		
B2	VREF1B2	IO	LVDS51n		B11	A12		
B2	VREF1B2	IO	LVDS51p		A11	B12	DM0T	DM0T
B2	VREF1B2	IO	LVDS50n		E11	D12		
	VREF1B2	GND						
B2	VREF1B2	IO	LVDS50p			C12		
B2	VREF1B2	IO				E11		
B2	VREF1B2	IO	LVDS49n		C10	A11		
B2	VREF1B2	VCCIO2						
B2	VREF1B2	IO	LVDS49p		D10	B11		
B2	VREF1B2	IO	LVDS48n		B10	D11		
B2	VREF1B2	IO	LVDS48p		A10	C11		
B2	VREF1B2	GND						
B2	VREF1B2	IO	LVDS47n			D10		

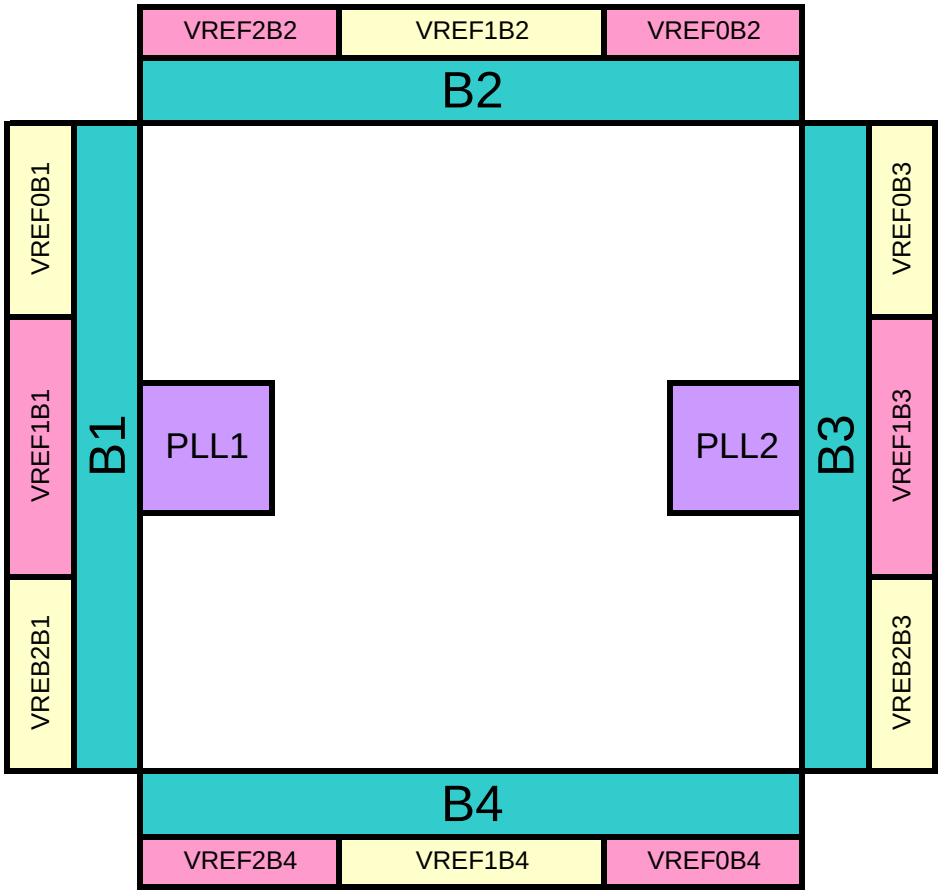
Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
B2	VREF1B2	IO	LVDS47p			C10		
B2	VREF1B2	IO	VREF1B2		E10	F10		
B2	VREF1B2	IO	LVDS46n		G9	A10		
B2	VREF1B2	IO	LVDS46p		F9	B10		
B2	VREF1B2	IO	LVDS45n			E10		
B2	VREF1B2	IO	LVDS45p			E9		
B2	VREF1B2	IO	LVDS44n		D9	C9	DM1T	DM1T
B2	VREF1B2	IO	LVDS44p		C9	D9		
B2	VREF1B2	IO	LVDS43n		A9	A9		
	VREF1B2	GND						
B2	VREF1B2	IO	LVDS43p		B9	B9		
B2	VREF1B2	IO	LVDS42n		D8	C8		
B2	VREF1B2	IO	LVDS42p		C8	D8		
B2	VREF1B2	VCCIO2						
B2	VREF1B2	IO	LVDS41n		A8	A8		
B2	VREF1B2	IO	LVDS41p		B8	B8		
B2	VREF2B2	IO	LVDS40n		E8	E8	DQ1T0	DQ1T0
B2	VREF2B2	GND						
B2	VREF2B2	IO	LVDS40p		E7	F8	DQ1T1	DQ1T1
B2	VREF2B2	IO	LVDS39n		A7	C7	DQ1T2	DQ1T2
B2	VREF2B2	IO	LVDS39p		B7	D7	DQ1T3	DQ1T3
B2	VREF2B2	IO	LVDS38n		D7	A7		
B2	VREF2B2	IO	LVDS38p		C7	B7		
B2	VREF2B2	IO	LVDS37n		E6	E7		
	VREF2B2	GND						
B2	VREF2B2	IO	LVDS37p		D6	F7		
B2	VREF2B2	IO	LVDS36n		B6	A6		
B2	VREF2B2	IO	LVDS36p		C6	B6		
B2	VREF2B2	IO	VREF2B2		A6	E6		
B2	VREF2B2	IO	DPCLK2		B5	C6	DQS1T	DQS1T
B2	VREF2B2	IO	LVDS35n		F8	B5		
B2	VREF2B2	VCCIO2						
B2	VREF2B2	IO	LVDS35p		G8	C5		
B2	VREF2B2	IO	LVDS34n		C5	D6	DQ1T4	DQ1T4
B2	VREF2B2	IO	LVDS34p		D5	D5	DQ1T5	DQ1T5
B2	VREF2B2	GND						
B2	VREF2B2	IO	LVDS33n		A4	A4	DQ1T6	DQ1T6
B2	VREF2B2	IO	LVDS33p		B4	B4	DQ1T7	DQ1T7
B2	VREF2B2	IO	LVDS32n	DEV_OE	B3	B3		
B2	VREF2B2	IO	LVDS32p	DEV_CLRn	C4	C4		
		VCCINT			A17	A19		
		VCCINT			A2	A2		
		VCCINT			B1	B1		
		VCCINT			B18	B20		
		VCCINT				H10		
		VCCINT				H12		
		VCCINT				J11		
		VCCINT				J9		
		VCCINT			H10	K10		
		VCCINT			J9	K12		
		VCCINT			K10	L11		
		VCCINT			L9	L9		
		VCCINT				M10		
		VCCINT				M12		
		VCCINT				N11		
		VCCINT				N9		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
		VCCINT			U1	W1		
		VCCINT			U18	W20		
		VCCINT			V17	Y19		
		VCCINT			V2	Y2		
		VCCIO1				E1		
		VCCIO1			E1	H8		
		VCCIO1			G7	K8		
		VCCIO1			M7	N8		
		VCCIO1			P1	T1		
		VCCIO4				R10		
		VCCIO4			P11	R12		
		VCCIO4			P8	R8		
		VCCIO4			V14	Y16		
		VCCIO4			V5	Y5		
		VCCIO3				E20		
		VCCIO3			E18	H13		
		VCCIO3			H12	K13		
		VCCIO3			M12	N13		
		VCCIO3			P18	T20		
		VCCIO2				A16		
		VCCIO2			A14	A5		
		VCCIO2			A5	F11		
		VCCIO2			E12	F13		
		VCCIO2			E9	F9		
		GND			A1	A1		
		GND			A16	A18		
		GND			A18	A20		
		GND			A3	A3		
		GND			B17	B19		
		GND			B2	B2		
		GND			C1	C1		
		GND			C18	C20		
		GND				G10		
		GND				G11		
		GND				G12		
		GND				G13		
		GND			H11	G8		
		GND			H8	G9		
		GND			H9	H11		
		GND			J10	H9		
		GND			J11	J10		
		GND			J8	J12		
		GND			K11	K11		
		GND			K8	K9		
		GND			K9	L10		
		GND			L10	L12		
		GND			L11	M11		
		GND			L8	M9		
		GND				N10		
		GND				N12		
		GND				P10		
		GND				P11		
		GND			T1	P12		
		GND			T18	P13		
		GND			U17	P8		
		GND			U2	P9		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F324	F400	DQS for x8 in the F324	DQS for x8 in the F400
		GND			V1	V1		
		GND			V16	V20		
		GND			V18	W19		
		GND			V3	W2		
		GND				Y1		
		GND				Y18		
		GND				Y20		
		GND				Y3		

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
		Configuration and JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.
		Clock and PLL Pins
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin.
PLL2_OUTp	I/O, Output	External clock output from PLL 2. This pin can be used with differential or single ended I/O standards. If clock output from PLL2 is not used, this pin is available as a user I/O pin.
PLL2_OUTn	I/O, Output	Negative terminal for external clock output from PLL2. If the clock output is single ended, this pin is available as a user I/O pin.
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..128]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 128. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDS[0..128]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 128. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin.
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.



Notes:

1.This is a top view of the silicon die.

2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II software for exact locations.

Bank & PLL Diagram

Version Number	Date	Changes Made
1.3	3/6/2006	Added CRC_ERROR pin in Pin List and Pin Definitions