Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GXB_L2		GXB_TX_L8n					H3								
GXB_L2		GXB_TX_L8p					H4								
GXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					J2								
GXB_L2		GXB_RX_L8n,GXB_REFCLK_L8n					J1								
GXB_L2		GXB_TX_L7n					K3								
GXB_L2		GXB_TX_L7p					K4								
GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					L2								
GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n					L1								
GXB_L2		GXB_TX_L6n					M3								
GXB_L2		GXB_TX_L6p					M4								
GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					N2								
GXB_L2		GXB_RX_L6n,GXB_REFCLK_L6n					N1								
GXB_L2		REFCLK2Lp					P9								
GXB_L2		REFCLK2Ln					P8								
GXB_L1		REFCLK1Ln					T8								
GXB_L1		REFCLK1Lp					T9								
GXB_L1		GXB_TX_L5n					P3								
GXB_L1		GXB_TX_L5p					P4								
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					R2								
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					R1								
GXB_L1		GXB_TX_L4n					T3								
GXB_L1		GXB_TX_L4p					T4								
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					U2								
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					U1								
GXB_L1		GXB_TX_L3n					V3								
GXB_L1		GXB_TX_L3p					V4								
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					W2								
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					W1								
GXB_L0		GXB_TX_L2n					Y3								
GXB_L0		GXB_TX_L2p					Y4								
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AA2								
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AA1								
GXB_L0		GXB_TX_L1n					AB3								
GXB_L0		GXB_TX_L1p					AB4								
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AC2								
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AC1								
GXB_L0		GXB_TX_L0n					AD3								
GXB_L0		GXB_TX_L0p					AD4								
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AE2								
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AE1								
GXB_L0		REFCLK0Lp					W8								
GXB_L0		REFCLK0Ln					W7								
3A		TDO		TDO			AB9								
3A		nCSO		DATA4			AB8								
3A		TMS		TMS			V9								
3A		AS_DATA3		DATA3			AC7								
3A		TCK		TCK			AC5								
3A		AS_DATA2		DATA2			AE8								
3A		TDI		TDI			U8								
3A		AS_DATA1		DATA1			AE5								
3A		DCLK		DCLK			U7								
3A		AS_DATA0,ASDO		DATA0			AE6								
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AE12	DQ1B							
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AE9								
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AD11	DQ1B							
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD9	DQ1B							
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	AD10	DQSn1B							
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AF10	DQ1B							
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AC9	DQS1B							
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AE11								
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AE7	DQ1B							
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AH4	DQ1B							
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AD7	DQ1B							
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AG3	DQ1B							
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AF5								
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AG8	DQ1B							
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	AF4								
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AF9	DQ1B							
3A	VREFB3AN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AG7								
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AH2	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AF8	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	AG1	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AB12	DQSn2B							
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AG6	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AA12	DQS2B							
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AF6								
3A	VREFB3AN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AH5	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AJ2	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AG5	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AJ1	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AD12								
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AH3	DQ2B							
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AC12								
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AG2	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AH9								
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AG11	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AG10	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AF11	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AB13	DQSn3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AK3	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AA13	DQS3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AK2								
3B	VREFB3BN0	IO			DIFFIO_TX_B21n	DIFFOUT_B21n	AK4	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AF13	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_TX_B21p	DIFFOUT_B21p	AJ4	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AE13	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AE14								
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AK6	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AD14								
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AJ5	DQ3B	DQ1B						
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	AJ7			GND	GND				
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AG13	DQ4B	DQ1B	B_A_15					
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AJ6	DQ4B	DQ1B	B_WE#					
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AG12	DQ4B	DQ1B	B_A_14					
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AC14	DQSn4B	DQSn1B	B_CS#_1	B_CS#_1				
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AK8	DQ4B	DQ1B	B_A_13					
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AB15	DQS4B	DQS1B	B_CS#_0	B_CS#_0				
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AK7			B_A_12					
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AK9	DQ4B	DQ1B	B_A_11					
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AH14	DQ4B	DQ1B	B_A_9	B_CA_9				
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AJ9	DQ4B	DQ1B	B_A_10					
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AH13	DQ4B	DQ1B	B_A_8	B_CA_8				
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B31n	DIFFOUT_B31n	AF15								
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AH8	DQ4B	DQ1B	B_RAS#					
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B31p	DIFFOUT_B31p	AF14								
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AH7	DQ4B	DQ1B	B_CAS#					
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AJ10			GND	GND				
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AK11	DQ5B		B_BA_2					
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AH10	DQ5B		B_BA_0					
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AJ11	DQ5B		B_BA_1					
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AA15	DQSn5B		B_CK#	B_CK#				

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AK13	DQ5B		B_A_7	B_CA_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	AA14	DQS5B		B_CK	B_CK				
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AK12			B_A_6	B_CA_6				
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AJ12	DQ5B		B_A_3	B_CA_3				
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AH15	DQ5B		B_A_5	B_CA_5				
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AH12	DQ5B		B_A_2	B_CA_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AG15	DQ5B		B_A_4	B_CA_4				
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	Y16								
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AK14	DQ5B		B_A_1	B_CA_1				
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	W15								
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AJ14	DQ5B		B_A_0	B_CA_0				
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AG17								
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AF18	DQ6B		B_DQ_0	B_DQ_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AG16	DQ6B		B_DQ_2	B_DQ_2				
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AE17	DQ6B		B_DQ_1	B_DQ_1				
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	W16	DQSn6B		B_DQS#_0	B_DQS#_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AF16	DQ6B		B_DQ_3	B_DQ_3				
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	V16	DQS6B		B_DQS_0	B_DQS_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AE16			B_ODT_0	B_ODT_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AK16	DQ6B		B_ODT_1	B_ODT_1				
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AH20	DQ6B		B_DQ_4	B_DQ_4				
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AJ16	DQ6B		B_DQ_6	B_DQ_6				
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AG21	DQ6B		B_DQ_5	B_DQ_5				
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	AB17								
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AH18	DQ6B		B_DQ_7	B_DQ_7				
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	AA16								
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AH17	DQ6B		B_DM_0	B_DM_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AH19			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AK18	DQ7B	DQ2B	B_DQ_8	B_DQ_8				
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AG18	DQ7B	DQ2B	B_DQ_10	B_DQ_10				
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AJ17	DQ7B	DQ2B	B_DQ_9	B_DQ_9				
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	W17	DQSn7B	DQ2B	B_DQS#_1	B_DQS#_1				
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AK19	DQ7B	DQ2B	B_DQ_11	B_DQ_11				
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	V17	DQS7B	DQ2B	B_DQS_1	B_DQS_1				
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AJ19			B_CKE_1	B_CKE_1				
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AJ21	DQ7B	DQ2B	B_CKE_0	B_CKE_0				
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AG20	DQ7B	DQ2B	B_DQ_12	B_DQ_12				
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AJ20	DQ7B	DQ2B	B_DQ_14	B_DQ_14				
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AF19	DQ7B	DQ2B	B_DQ_13	B_DQ_13				
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	AD17								
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AH24	DQ7B	DQ2B	B_DQ_15	B_DQ_15				
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	AC18								
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AG23	DQ7B	DQ2B	B_DM_1	B_DM_1				
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AH22			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AE19	DQ8B	DQ2B	B_DQ_16	B_DQ_16				
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AG22	DQ8B	DQ2B	B_DQ_18	B_DQ_18				
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AE18	DQ8B	DQ2B	B_DQ_17	B_DQ_17				
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AA18	DQSn8B	DQSn2B	B_DQS#_2	B_DQS#_2				
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AK22	DQ8B	DQ2B	B_DQ_19	B_DQ_19				
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	Y17	DQS8B	DQS2B	B_DQS_2	B_DQS_2				
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AK21			B_RESET#	B_RESET#				
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AJ22	DQ8B	DQ2B	GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AF21	DQ8B	DQ2B	B_DQ_20	B_DQ_20				
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AH23	DQ8B	DQ2B	B_DQ_22	B_DQ_22				
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AF20	DQ8B	DQ2B	B_DQ_21	B_DQ_21				
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	AA19			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AK24	DQ8B	DQ2B	B_DQ_23	B_DQ_23				
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	Y18			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AK23	DQ8B	DQ2B	B_DM_2	B_DM_2				
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AJ25			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AF24	DQ9B	DQ3B	B_DQ_24	B_DQ_24				
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AJ24	DQ9B	DQ3B	B_DQ_26	B_DQ_26				
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AF23	DQ9B	DQ3B	B_DQ_25	B_DQ_25				
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AD19	DQSn9B	DQ3B	B_DQS#_3	B_DQS#_3				
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AK26	DQ9B	DQ3B	B_DQ_27	B_DQ_27				
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AC20	DQS9B	DQ3B	B_DQS_3	B_DQS_3				
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AJ26			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AH25	DQ9B	DQ3B	GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AE23	DQ9B	DQ3B	B_DQ_28	B_DQ_28				
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AG25	DQ9B	DQ3B	B_DQ_30	B_DQ_30				
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AE22	DQ9B	DQ3B	B_DQ_29	B_DQ_29				
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	W19			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AK27	DQ9B	DQ3B	B_DQ_31	B_DQ_31				
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	V18			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AJ27	DQ9B	DQ3B	B_DM_3	B_DM_3				
4A	VREFB4AN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AK29			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AD21	DQ10B	DQ3B	B_DQ_32	B_DQ_32				
4A	VREFB4AN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AK28	DQ10B	DQ3B	B_DQ_34	B_DQ_34				
4A	VREFB4AN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AD20	DQ10B	DQ3B	B_DQ_33	B_DQ_33				
4A	VREFB4AN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AA20	DQSn10B	DQSn3B	B_DQS#_4	B_DQS#_4				
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AH27	DQ10B	DQ3B	B_DQ_35	B_DQ_35				
4A	VREFB4AN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	Y19	DQS10B	DQS3B	B_DQS_4	B_DQS_4				
4A	VREFB4AN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AG26			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AF26	DQ10B	DQ3B	GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AC23	DQ10B	DQ3B	B_DQ_36	B_DQ_36				
4A	VREFB4AN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AF25	DQ10B	DQ3B	B_DQ_38	B_DQ_38				
4A	VREFB4AN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AC22	DQ10B	DQ3B	B_DQ_37	B_DQ_37				
4A	VREFB4AN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AB21			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AE24	DQ10B	DQ3B	B_DQ_39	B_DQ_39				
4A	VREFB4AN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AA21			GND	GND				
4A	VREFB4AN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AD24	DQ10B	DQ3B	B_DM_4	B_DM_4				
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AG27	DQ1R							
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AD25								
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AH28	DQ1R							
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	AC25								
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AJ29	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	W20	DQ1R							
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AH29	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	Y21	DQ1R							
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AE26								
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	W21	DQS1R							
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AD27	DQ1R							
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	W22	DQSn1R							
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AA25	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	AB22	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AB26								
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	AB23	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	AA24								
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	AE27	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	AB25								
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	AE28	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	Y23	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	AG28	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	Y24	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	AF28	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	V23	DQS2R							
5A	VREFB5AN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	AF29								
5A	VREFB5AN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	W24	DQSn2R							
5A	VREFB5AN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AF30	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	AD26	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	AH30	DQ2R							

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
5A	VREFB5AN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	AC27	DQ2R							
5A	VREFB5AN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	AG30								
5B	VREFB5BN0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	W25								
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	AC28	DQ3R							
5B	VREFB5BN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	V25								
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	AC29	DQ3R							
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	AB30	DQ3R							
5B	VREFB5BN0	IO			DIFFIO_TX_R20p	DIFFOUT_R20p	AB28	DQ3R							
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	AA30	DQ3R							
5B	VREFB5BN0	IO			DIFFIO_TX_R20n	DIFFOUT_R20n	AA28	DQ3R							
5B	VREFB5BN0	IO	CLK5p		DIFFIO_RX_R21p	DIFFOUT_R21p	AA26	DQS3R							
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R22p	DIFFOUT_R22p	AE29								
5B	VREFB5BN0	IO	CLK5n		DIFFIO_RX_R21n	DIFFOUT_R21n	AB27	DQSn3R							
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R22n	DIFFOUT_R22n	AD29	DQ3R							
5B	VREFB5BN0	IO	CLK4p,FPLL_BR_FBp		DIFFIO_RX_R23p	DIFFOUT_R23p	Y26	DQ3R							
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	AD30	DQ3R							
5B	VREFB5BN0	IO	CLK4n,FPLL_BR_FBn		DIFFIO_RX_R23n	DIFFOUT_R23n	Y27	DQ3R							
5B	VREFB5BN0	IO	RZQ_2		DIFFIO_TX_R24n	DIFFOUT_R24n	AC30								
6B	VREFB6BN0 H	HPS_DDR					W27			HPS_DM_4	HPS_DM_4				
6B	VREFB6BN0 H	HPS_DDR					Y29			HPS_DQ_39	HPS_DQ_39				
6B	VREFB6BN0 H	HPS_DDR					U25			HPS_DQ_37	HPS_DQ_37				
6B	VREFB6BN0 H	HPS_DDR					V27			HPS_DQ_38	HPS_DQ_38				
6B	VREFB6BN0 H	HPS_DDR					T25			HPS_DQ_36	HPS_DQ_36				
6B	VREFB6BN0 H	HPS_DDR					T24			HPS_DQS_4	HPS_DQS_4				
6B	VREFB6BN0 H	HPS_GPI13					Y28								
6B	VREFB6BN0 H	HPS_DDR					T23			HPS_DQS#_4	HPS_DQS#_4				
6B	VREFB6BN0 H	HPS_DDR					V28			HPS_DQ_35	HPS_DQ_35				
6B	VREFB6BN0 H	HPS_DDR					R24			HPS_DQ_33	HPS_DQ_33				
6B	VREFB6BN0 H	HPS_DDR					U27			HPS_DQ_34	HPS_DQ_34				
6B	VREFB6BN0 H	HPS_DDR					W26			HPS_DQ_32	HPS_DQ_32				
6B	VREFB6BN0 H	HPS_GPI12					V29								
6B	VREFB6BN0 H	HPS_GPI11					U20								
6B	VREFB6BN0 H	HPS_DDR					W30			HPS_DM_3	HPS_DM_3				
6B	VREFB6BN0 H	HPS_GPI10					T21								
6B	VREFB6BN0 H	HPS_DDR					W29			HPS_DQ_31	HPS_DQ_31				
6B	VREFB6BN0 H	HPS_DDR					R26			HPS_DQ_29	HPS_DQ_29				
6B	VREFB6BN0 H	HPS_DDR					V30			HPS_DQ_30	HPS_DQ_30				
6B	VREFB6BN0 H	HPS_DDR					R27			HPS_DQ_28	HPS_DQ_28				
6B	VREFB6BN0 H	VREFB6BN0_HPS					U30								
6B	VREFB6BN0 H	HPS_DDR					R22			HPS_DQS_3	HPS_DQS_3				
6B	VREFB6BN0 H	HPS_GPI9					U28								
6B	VREFB6BN0 H	HPS_DDR					R21			HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6BN0 H	HPS_DDR					T28			HPS_DQ_27	HPS_DQ_27				
6B	VREFB6BN0 H	HPS_DDR					P25			HPS_DQ_25	HPS_DQ_25				
6B	VREFB6BN0 H	HPS_DDR					T29			HPS_DQ_26	HPS_DQ_26				
6B	VREFB6BN0 H	HPS_DDR					P24			HPS_DQ_24	HPS_DQ_24				
6B	VREFB6BN0 H	HPS_GPI8					T30								
6B	VREFB6BN0 H	HPS_GPI7					V20								
6B	VREFB6BN0 H	HPS_DDR					R28			HPS_DM_2	HPS_DM_2				
6B	VREFB6BN0 H	HPS_GPI6					P22								
6B	VREFB6BN0 H	HPS_DDR					R29			HPS_DQ_23	HPS_DQ_23				
6B	VREFB6BN0 H	HPS_DDR					P27			HPS_DQ_21	HPS_DQ_21				
6B	VREFB6BN0 H	HPS_DDR					N27			HPS_DQ_22	HPS_DQ_22				
6B	VREFB6BN0 H	HPS_DDR					P26			HPS_DQ_20	HPS_DQ_20				
6B	VREFB6BN0 H	HPS_GPI5					P29								
6B	VREFB6BN0 H	HPS_DDR					R19			HPS_DQS_2	HPS_DQS_2				
6B	VREFB6BN0 H	HPS_DDR					P30			HPS_RESET#	HPS_RESET#				
6B	VREFB6BN0 H	HPS_DDR					R18			HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6BN0 H	HPS_DDR					N28			HPS_DQ_19	HPS_DQ_19				
6B	VREFB6BN0 H	HPS_DDR					T26			HPS_DQ_17	HPS_DQ_17				
6B	VREFB6BN0 H	HPS_DDR					N29			HPS_DQ_18	HPS_DQ_18				
6B	VREFB6BN0 H	HPS_DDR					U26			HPS_DQ_16	HPS_DQ_16				
6B	VREFB6BN0 H	HPS_GPI4					N30								
6A	VREFB6AN0 H	HPS_GPI3					M22								
6A	VREFB6AN0 H	HPS_DDR					M28			HPS_DM_1	HPS_DM_1				
6A	VREFB6AN0 H	HPS_GPI2					N23								
6A	VREFB6AN0 H	HPS_DDR					M30			HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AN0 H	HPS_DDR					M27			HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AN0 H	HPS_DDR					L28			HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AN0 H	HPS_DDR					M26			HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AN0 H	HPS_DDR					L29			HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AN0 H	HPS_DDR					N25			HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AN0 H	HPS_DDR					L30			HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AN0 H	HPS_DDR					N24			HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AN0 H	HPS_DDR					K27			HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AN0 H	HPS_DDR					L26			HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AN0 H	HPS_DDR					K29			HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AN0 H	HPS_DDR					K26			HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AN0 H	HPS_GPI1					J26								
6A	VREFB6AN0 H	HPS_GPI0					M25								
6A	VREFB6AN0 H	HPS_DDR					K28			HPS_DM_0	HPS_DM_0				
6A	VREFB6AN0 H	HPS_DDR					J29			HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AN0 H	HPS_DDR					L24			HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AN0 H	HPS_DDR					J30			HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AN0 H	HPS_DDR					L25			HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AN0 H	HPS_DDR					H29			HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AN0 H	HPS_DDR					N18			HPS_DQS_0	HPS_DQS_0				
6A	VREFB6AN0 H	HPS_DDR					H28			HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AN0 H	HPS_DDR					M19			HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB6AN0 H	HPS_DDR					G28			HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AN0 H	HPS_DDR					K22			HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AN0 H	HPS_DDR					H30			HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AN0 H	HPS_DDR					K23			HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AN0 H	VREFB6AN0_HPS					G27								
6A	VREFB6AN0 H	HPS_DDR					F26			HPS_A_0	HPS_CA_0				
6A	VREFB6AN0 H	HPS_DDR					G30			HPS_A_1	HPS_CA_1				
6A	VREFB6AN0 H	HPS_DDR					J25			HPS_A_4	HPS_CA_4				
6A	VREFB6AN0 H	HPS_DDR					F28			HPS_A_2	HPS_CA_2				
6A	VREFB6AN0 H	HPS_DDR					J27			HPS_A_5	HPS_CA_5				
6A	VREFB6AN0 H	HPS_DDR					F30			HPS_A_3	HPS_CA_3				
6A	VREFB6AN0 H	HPS_DDR					M23			HPS_CK	HPS_CK				
6A	VREFB6AN0 H	HPS_DDR					F29			HPS_A_6	HPS_CA_6				
6A	VREFB6AN0 H	HPS_DDR					L23			HPS_CK#	HPS_CK#				
6A	VREFB6AN0 H	HPS_DDR					E28			HPS_A_7	HPS_CA_7				
6A	VREFB6AN0 H	HPS_DDR					J24			HPS_BA_1					
6A	VREFB6AN0 H	HPS_DDR					E29			HPS_BA_0					
6A	VREFB6AN0 H	HPS_DDR					J23			HPS_BA_2					
6A	VREFB6AN0 H	HPS_DDR					E27			HPS_CAS#					
6A	VREFB6AN0 H	HPS_DDR					D30			HPS_RAS#					
6A	VREFB6AN0 H	HPS_DDR					H27			HPS_A_8	HPS_CA_8				
6A	VREFB6AN0 H	HPS_DDR					D29			HPS_A_10					
6A	VREFB6AN0 H	HPS_DDR					G26			HPS_A_9	HPS_CA_9				
6A	VREFB6AN0 H	HPS_DDR					C30			HPS_A_11					
6A	VREFB6AN0 H	HPS_DDR					H24			HPS_CS#_0	HPS_CS#_0				
6A	VREFB6AN0 H	HPS_DDR					B30			HPS_A_12					
6A	VREFB6AN0 H	HPS_DDR					K21			HPS_CS#_1	HPS_CS#_1				
6A	VREFB6AN0 H	HPS_DDR					C29			HPS_A_13					
6A	VREFB6AN0 H	HPS_DDR					H25			HPS_A_14					
6A	VREFB6AN0 H	HPS_DDR					C28			HPS_WE#					
6A	VREFB6AN0 H	HPS_DDR					G25			HPS_A_15					
6A	VREFB6AN0 H	HPS_RZQ_0					D27								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					J22								
		GND					D26								
7A		HPS_nRST					C27								
7A		HPS_nPOR					F23								
7A		HPS_TDO					B28								
		VCCRSTCLK_HPS					G23								
7A		HPS_TMS					A29								
7A		HPS_TCK					H22								
7A		HPS_TRST					A28								
7A		HPS_TDI					B27								
		GND					A26								
7A		HPS_PORSEL					F24								
7A		HPS_CLK1					D25								
7A		HPS_CLK2					F25								
7A	VREFB7A7B7C	TRACE_CLK					B26					TRACE_CLK			HPS_GPIO48
7A	VREFB7A7B7C	TRACE_D0					B25					TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7B7C	TRACE_D1					C25					TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7B7C	TRACE_D2					A25					TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPIO51
7A	VREFB7A7B7C	TRACE_D3					H23					TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPIO52
7A	VREFB7A7B7C	TRACE_D4					A24					TRACE_D4	SPIS1_CLK	CAN1_RX	HPS_GPIO53
7A	VREFB7A7B7C	TRACE_D5					G21					TRACE_D5	SPIS1_MOSI	CAN1_TX	HPS_GPIO54
7A	VREFB7A7B7C	TRACE_D6					C24					TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPIO55
7A	VREFB7A7B7C	TRACE_D7					E23					TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPIO56
7A	VREFB7A7B7C	SPIM0_CLK					A23					SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7B7C	SPIM0_MOSI					C22					SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7B7C	SPIM0_MISO					B23					SPIM0_MISO	CAN1_RX	UART1_CTS	HPS_GPIO59
7A	VREFB7A7B7C	SPIM0_SS0,BOOTSEL0					H20					SPIM0_SS0	CAN1_TX	UART1_RTS	HPS_GPIO60
7A	VREFB7A7B7C	UART0_RX					B22					UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GPIO61
7A	VREFB7A7B7C	UART0_TX,CLKSEL1					G22					UART0_TX	CAN0_TX	SPIM1_SS1	HPS_GPIO62
7A	VREFB7A7B7C	I2C0_SDA					C23					I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A7B7C	I2C0_SCL					D22					I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A7B7C	CAN0_RX					E24					CAN0_RX	UART0_RX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A7B7C	CAN0_TX,CLKSEL0					D24					CAN0_TX	UART0_TX	SPIM1_SS0	HPS_GPIO66
7B	VREFB7A7B7C	NAND_ALE					H19					NAND_ALE	RGMII1_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C	NAND_CE					F20					NAND_CE	RGMII1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A7B7C	NAND_CLE					J19					NAND_CLE	RGMII1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7B7C	NAND_RE					F21					NAND_RE	RGMII1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7B7C	NAND_RB					F19					NAND_RB	RGMII1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7B7C	NAND_DQ0					A21					NAND_DQ0	RGMII1_RXD0		HPS_GPIO19
7B	VREFB7A7B7C	NAND_DQ1					E21					NAND_DQ1	RGMII1_MDIO	I2C3_SDA	HPS_GPIO20
7B	VREFB7A7B7C	NAND_DQ2					B21					NAND_DQ2	RGMII1_MDC	I2C3_SCL	HPS_GPIO21
7B	VREFB7A7B7C	NAND_DQ3					K17					NAND_DQ3	RGMII1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7B7C	NAND_DQ4					A20					NAND_DQ4	RGMII1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7B7C	NAND_DQ5					G20					NAND_DQ5	RGMII1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7B7C	NAND_DQ6					B20					NAND_DQ6	RGMII1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7B7C	NAND_DQ7					B18					NAND_DQ7	RGMII1_RXD2		HPS_GPIO26
7B	VREFB7A7B7C	NAND_WP					D21					NAND_WP	RGMII1_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C	NAND_WE,BOOTSEL2					D20					NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C	QSPI_IO0					C20					QSPI_IO0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7B7C	QSPI_IO1					H18					QSPI_IO1		USB1_STP	HPS_GPIO30
7B	VREFB7A7B7C	QSPI_IO2					A19					QSPI_IO2		USB1_DIR	HPS_GPIO31
7B	VREFB7A7B7C	QSPI_IO3					E19					QSPI_IO3		USB1_NXT	HPS_GPIO32
7B	VREFB7A7B7C	QSPI_SS0,BOOTSEL1					A18					QSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C	QSPI_CLK					D19					QSPI_CLK			HPS_GPIO34
7B	VREFB7A7B7C	QSPI_SS1					C19					QSPI_SS1			HPS_GPIO35
7C	VREFB7A7B7C	SDMMC_CMD					F18					SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A7B7C	SDMMC_PWREN					B17					SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A7B7C	SDMMC_D0					G18					SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A7B7C	SDMMC_D1					C17					SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A7B7C	SDMMC_D4					H17					SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A7B7C	SDMMC_D5					C18					SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A7B7C	SDMMC_D6					G17					SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A7B7C	SDMMC_D7					E18					SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A7B7C	HPS_GPIO44					E17						USB0_CLK		HPS_GPIO44
7C	VREFB7A7B7C	SDMMC_CCLK_OUT					A16					SDMMC_CCLK_OUT	USB0_STP		HPS_GPIO45
7C	VREFB7A7B7C	SDMMC_D2					D17					SDMMC_D2	USB0_DIR		HPS_GPIO46
7C	VREFB7A7B7C	SDMMC_D3					B16					SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A7B7C	RGMII0_TX_CLK					F16					RGMII0_TX_CLK			HPS_GPIO0
7D	VREFB7A7B7C	RGMII0_TXD0					E16					RGMII0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A7B7C	RGMII0_TXD1					G16					RGMII0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A7B7C	RGMII0_TXD2					D16					RGMII0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A7B7C	RGMII0_TXD3					D14					RGMII0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A7B7C	RGMII0_RXD0					A15					RGMII0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A7B7C	RGMII0_MDIO					C14					RGMII0_MDIO	USB1_D5	I2C2_SDA	HPS_GPIO6
7D	VREFB7A7B7C	RGMII0_MDC					D15					RGMII0_MDC	USB1_D6	I2C2_SCL	HPS_GPIO7
7D	VREFB7A7B7C	RGMII0_RX_CTL					M17					RGMII0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A7B7C	RGMII0_TX_CTL					B15					RGMII0_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C	RGMII0_RX_CLK					N16					RGMII0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A7B7C	RGMII0_RXD1					C15					RGMII0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A7B7C	RGMII0_RXD2					E14					RGMII0_RXD2	USB1_DIR		HPS_GPIO12
7D	VREFB7A7B7C	RGMII0_RXD3					A14					RGMII0_RXD3	USB1_NXT		HPS_GPIO13
8A	VREFB8AN0	IO	CLK7p		DIFFIO_RX_T1p	DIFFOUT_T1p	H15								
8A	VREFB8AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	B13	DQ1T							
8A	VREFB8AN0	IO	CLK7n		DIFFIO_RX_T1n	DIFFOUT_T1n	G15								
8A	VREFB8AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	A13	DQ1T							
8A	VREFB8AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	C13	DQ1T							
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T4p	DIFFOUT_T4p	A11	DQ1T							
8A	VREFB8AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	B12	DQ1T							
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T4n	DIFFOUT_T4n	A10	DQ1T							
8A	VREFB8AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	F15	DQS1T							
8A	VREFB8AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	C12								
8A	VREFB8AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	F14	DQSn1T							
8A	VREFB8AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	B11	DQ1T							
8A	VREFB8AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	D11	DQ1T							
8A	VREFB8AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	A9	DQ1T							
8A	VREFB8AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	D10	DQ1T							
8A	VREFB8AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	A8								
8A	VREFB8AN0	IO	CLK6p,FPLL_TL_FBp		DIFFIO_RX_T9p	DIFFOUT_T9p	K14								
8A	VREFB8AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	C7	DQ2T	DQ1T						
8A	VREFB8AN0	IO	CLK6n,FPLL_TL_FBn		DIFFIO_RX_T9n	DIFFOUT_T9n	J14								
8A	VREFB8AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	B7	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	E9	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C8	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	D9	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	B8	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	H14	DQS2T	DQS1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	C10								
8A	VREFB8AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	G13	DQSn2T	DQSn1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	C9	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	F13	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A6	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	E13	DQ2T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A5								
8A	VREFB8AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H8								
8A	VREFB8AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	A4	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	G8								
8A	VREFB8AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	A3	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	E12	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	D6	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	D12	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	C5	DQ3T	DQ1T						

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
8A	VREFB8AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	H13	DQS3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	D5								
8A	VREFB8AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	H12	DQSn3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	C4	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	F11	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	E8	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	E11	DQ3T	DQ1T						
8A	VREFB8AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	D7								
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	J7								
8A	VREFB8AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	B2	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	H7								
8A	VREFB8AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	B1	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	B6	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	C3	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	B5	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B3	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	K12	DQS4T	DQS2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	D2								
8A	VREFB8AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J12	DQSn4T	DQSn2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C2	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	G12	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	E4	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	G11	DQ4T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	D4								
8A	VREFB8AN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	K7								
8A	VREFB8AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	E3	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	K8								
8A	VREFB8AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	E2	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	G10	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	E1	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F10	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D1	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	J10	DQS5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	E7								
8A	VREFB8AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	J9	DQSn5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	E6	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	F9	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	G7	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	F8	DQ5T	DQ2T						
8A	VREFB8AN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	F6								
9A		MSEL0		MSEL0			L8								
9A		CONF_DONE		CONF_DONE			F3								
9A		MSEL1		MSEL1			K6								
9A		nSTATUS		nSTATUS			F4								
9A		nCE		nCE			G5								
9A		MSEL2		MSEL2			G6								
9A		MSEL3		MSEL3			L7								
9A		nCONFIG		nCONFIG			J5								
9A		MSEL4		MSEL4			L9								
		GND					J6								
		GND					A12								
		GND					A17								
		GND					A2								
		GND					A22								
		GND					A27								
		GND					AA11								
		GND					AA22								
		GND					AA3								
		GND					AA4								
		GND					AA6								
		GND					AA9								
		GND					AB1								
		GND					AB19								
		GND					AB2								
		GND					AB29								
		GND					AB5								
		GND					AB7								
		GND					AC16								
		GND					AC26								
		GND					AC3								
		GND					AC4								
		GND					AC6								
		GND					AC8								
		GND					AD1								
		GND					AD2								
		GND					AD23								
		GND					AD5								
		GND					AE10								
		GND					AE20								
		GND					AE3								
		GND					AE4								
		GND					AF1								
		GND					AF12								
		GND					AF17								
		GND					AF2								
		GND					AF27								
		GND					AF3								
		GND					AG14								
		GND					AG24								
		GND					AG9								
		GND					AH1								
		GND					AH11								
		GND					AH21								
		GND					AH6								
		GND					AJ18								
		GND					AJ28								
		GND					AJ3								
		GND					AJ30								
		GND					AK15								
		GND					AK25								
		GND					AK5								
		GND					B14								
		GND					B19								
		GND					B24								
		GND					B29								
		GND					B9								
		GND					C1								
		GND					C16								
		GND					C21								
		GND					C26								
		GND					C6								
		GND					D13								
		GND					D23								
		GND					D3								
		GND					E10								
		GND					E25								
		GND					E30								
		GND					F17								
		GND					F2								
		GND					F27								
		GND					F5								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					F7								
		GND					G24								
		GND					G3								
		GND					G4								
		GND					H1								
		GND					H11								
		GND					H2								
		GND					H5								
		GND					J18								
		GND					J28								
		GND					J3								
		GND					J4								
		GND					J8								
		GND					K1								
		GND					K10								
		GND					K15								
		GND					K2								
		GND					K20								
		GND					K25								
		GND					K5								
		GND					L11								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L22								
		GND					L3								
		GND					L4								
		GND					L6								
		GND					M1								
		GND					M10								
		GND					M12								
		GND					M14								
		GND					M16								
		GND					M18								
		GND					M2								
		GND					M20								
		GND					M29								
		GND					M5								
		GND					M7								
		GND					M8								
		GND					N11								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N26								
		GND					N3								
		GND					N4								
		GND					N6								
		GND					N8								
		GND					N9								
		GND					P1								
		GND					P10								
		GND					P12								
		GND					P14								
		GND					P16								
		GND					P18								
		GND					P2								
		GND					P20								
		GND					P5								
		GND					P7								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R17								
		GND					R3								
		GND					R30								
		GND					R4								
		GND					R6								
		GND					R8								
		GND					R9								
		GND					T1								
		GND					T10								
		GND					T12								
		GND					T14								
		GND					T15								
		GND					T16								
		GND					T2								
		GND					T20								
		GND					T27								
		GND					T5								
		GND					T7								
		GND					U11								
		GND					U13								
		GND					U15								
		GND					U17								
		GND					U24								
		GND					U29								
		GND					U3								
		GND					U4								
		GND					U6								
		GND					U9								
		GND					V1								
		GND					V10								
		GND					V12								
		GND					V14								
		GND					V19								
		GND					V2								
		GND					V21								
		GND					V5								
		GND					V7								
		GND					W11								
		GND					W13								
		GND					W18								
		GND					W28								
		GND					W3								
		GND					W4								
		GND					W6								
		GND					W9								
		GND					Y1								
		GND					Y10								
		GND					Y12								
		GND					Y14								
		GND					Y15								
		GND					Y2								
		GND					Y20								
		GND					Y25								
		GND					Y30								
		GND					Y5								
		GND					Y7								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					Y8								
		GND					U22								
		GND					T18								
		VCC					M11								
		VCC					M13								
		VCC					M9								
		VCC					N10								
		VCC					N12								
		VCC					N14								
		VCC					P11								
		VCC					P13								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					T11								
		VCC					T13								
		VCC					U10								
		VCC					U12								
		VCC					U14								
		VCC					V11								
		VCC					V13								
		VCC					V15								
		VCC					W10								
		VCC					W12								
		VCC					W14								
		VCC					Y11								
		VCC					Y13								
		VCC					Y9								
		VCC					U21								
		DNU					F1								
		DNU					G2								
		DNU					AA7								
		DNU					AD15								
		DNU					E26								
		DNU					J15								
		VCCPGM					AB10								
		VCCPGM					AA23								
		VCCPGM					J11								
		VCCBAT					H9								
		VCCIO3A					AC11								
		VCCIO3A					AD8								
		VCCIO3A					AF7								
		VCCIO3A					AG4								
		VCCIO3B					AB14								
		VCCIO3B					AD13								
		VCCIO3B					AE15								
		VCCIO3B					AJ13								
		VCCIO3B					AJ8								
		VCCIO3B					AK10								
		VCCIO4A					AA17								
		VCCIO4A					AC21								
		VCCIO4A					AD18								
		VCCIO4A					AE25								
		VCCIO4A					AF22								
		VCCIO4A					AG19								
		VCCIO4A					AH16								
		VCCIO4A					AH26								
		VCCIO4A					AJ23								
		VCCIO4A					AK20								
		VCCIO5A					AB24								
		VCCIO5A					AD28								
		VCCIO5A					AG29								
		VCCIO5A					W23								
		VCCIO5B					AA27								
		VCCIO5B					AE30								
		VCCIO6A_HPS					D28								
		VCCIO6A_HPS					G29								
		VCCIO6A_HPS					H26								
		VCCIO6A_HPS					K24								
		VCCIO6A_HPS					K30								
		VCCIO6A_HPS					L27								
		VCCIO6A_HPS					M24								
		VCCIO6A_HPS					N21								
		VCCIO6B_HPS					P23								
		VCCIO6B_HPS					P28								
		VCCIO6B_HPS					R25								
		VCCIO6B_HPS					T22								
		VCCIO6B_HPS					U19								
		VCCIO6B_HPS					V26								
		VCCIO7A_HPS					F22								
		VCCIO7A_HPS					H21								
		VCCIO7B_HPS					E20								
		VCCIO7B_HPS					G19								
		VCCIO7C_HPS					D18								
		VCCIO7D_HPS					E15								
		VCCIO7D_HPS					H16								
		VCCIO8A					A7								
		VCCIO8A					B4								
		VCCIO8A					C11								
		VCCIO8A					D8								
		VCCIO8A					E5								
		VCCIO8A					F12								
		VCCIO8A					G14								
		VCCIO8A					G9								
		VCCIO8A					H6								
		VCCIO8A					J13								
		VCCPD3A					AA10								
		VCCPD3A					AC10								
		VCCPD3B4A					AB18								
		VCCPD3B4A					AB20								
		VCCPD3B4A					AC13								
		VCCPD3B4A					AC15								
		VCCPD3B4A					AC17								
		VCCPD3B4A					AC19								
		VCCPD3B4A					AD16								
		VCCPD3B4A					AE21								
		VCCPD5A					V22								
		VCCPD5A					V24								
		VCCPD5B					U23								
		VCCPD6A6B_HPS					M21								
		VCCPD6A6B_HPS					N22								
		VCCPD6A6B_HPS					P21								
		VCCPD6A6B_HPS					R20								
		VCCPD6A6B_HPS					R23								
		VCCPD7A_HPS					K19								
		VCCPD7B_HPS					K18								
		VCCPD7C_HPS					J17								
		VCCPD7D_HPS					K16								
		VCCPD8A					K11								
		VCCPD8A					K13								
		VCCPD8A					L10								

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPD8A					L12								
		VCCPD8A					L14								
3A	VREFB3AN0	VREFB3AN0					AD6								
3B	VREFB3BN0	VREFB3BN0					AJ15								
4A	VREFB4AN0	VREFB4AN0					AK17								
5A	VREFB5AN0	VREFB5AN0					AC24								
5B	VREFB5BN0	VREFB5BN0					AA29								
	VREFB7A7B7	VREFB7A7B7C7DN0_HPS					E22								
8A	VREFB8AN0	VREFB8AN0					B10								
		VCCH_GXBL					AB6								
		VCCH_GXBL					P6								
		VCCH_GXBL					V6								
		VCCL_GXBL					L5								
		VCCL_GXBL					R5								
		VCCL_GXBL					W5								
		VCCRSTCLK_HPS					J20								
		RREF_TL					G1								
		VCCA_FPLL					N7								
		VCCA_FPLL					R7								
		VCCA_FPLL					V8								
		VCCA_FPLL					AA8								
		VCCA_FPLL					K9								
		VCCA_FPLL					Y22								
		VCC_AUX					AB11								
		VCC_AUX					AB16								
		VCC_AUX					AD22								
		VCC_AUX					H10								
		VCC_AUX					J16								
		VCC_AUX_SHARED					J21								
		VCCE_GXBL					AA5								
		VCCE_GXBL					M6								
		VCCE_GXBL					N5								
		VCCE_GXBL					T6								
		VCCE_GXBL					U5								
		VCCE_GXBL					Y6								
		VCCPLL_HPS					L21								
		VCC_HPS					U18								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					L20								
		VCC_HPS					M15								
		VCC_HPS					N20								
		VCC_HPS					P15								
		VCC_HPS					P17								
		VCC_HPS					P19								
		VCC_HPS					R16								
		VCC_HPS					T17								
		VCC_HPS					T19								
		VCC_HPS					U16								

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.
(2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
(3) RESET pin is only applicable for DDR3 device.

Pin Information for the Cyclone® V 5CSTFD6 Device
Version 1.4

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.