



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					I17								
		GND					I2								
		GND					I20								
		GND					I24								
		GND					I27								
		GND					I8								
		GND					I8								
		GND					I14								
		GND					I3								
		GND					I8								
		GND					I9								
		GND					I01								
		GND					I16								
		GND					I18								
		GND					I22								
		GND					I25								
		GND					I24								
		GND					I25								
		GND					I26								
		GND					I26								
		GND					I21								
		GND					I21								
		VCC					K13								
		VCC					K16								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M16								
		VCC					M8								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N8								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P16								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T13								
		VCC					T9								
		VCC					L4								
		VCC					T4								
		VCC					M5								
		VCC					M5								
		VCC					R5								
		VCC					T5								
		VCC					L26								
		DNU					A2								
		DNU					B2								
		DNU					D1								
		DNU					D2								
		DNU					H1								
		DNU					H2								
		DNU					M1								
		DNU					M2								
		DNU					T1								
		DNU					T2								
		DNU					Y1								
		DNU					Y2								
		DNU					AD1								
		DNU					AD2								
		DNU					CD1								
		DNU					E12								
		DNU					U8								
		DNU					AE14								
		DNU					V10								
		VCCPGM					AD24								
		VCCPGM					H10								
		VCCPGM					D7								
		VCCBAT					AA5								
		VCCIO3A					H5								
		VCCIO3A					AA12								
		VCCIO3B					AE10								
		VCCIO3B					AE13								
		VCCIO3B					AG4								
		VCCIO4A					AA16								
		VCCIO4A					AE1								
		VCCIO4A					AF14								
		VCCIO4A					AF19								
		VCCIO4A					AG13								
		VCCIO4A					AG22								
		VCCIO4A					AH15								
		VCCIO4A					AK25								
		VCCIO4A					W13								
		VCCIO5A					AC25								
		VCCIO5A					W17								
		VCCIO6A_HPS					C26								
		VCCIO6A_HPS					C27								
		VCCIO6A_HPS					F27								
		VCCIO6A_HPS					E24								
		VCCIO6A_HPS					H21								
		VCCIO6A_HPS					H26								
		VCCIO6A_HPS					L26								
		VCCIO6A_HPS					M21								
		VCCIO6B_HPS					AD27								
		VCCIO6B_HPS					P27								
		VCCIO6B_HPS					I21								
		VCCIO6B_HPS					T26								
		VCCIO6B_HPS					U18								
		VCCIO6B_HPS					W27								
		VCCIO7A_HPS					CD1								
		VCCIO7A_HPS					D18								
		VCCIO7B_HPS					B13								
		VCCIO7B_HPS					H14								
		VCCIO7C_HPS					B10								
		VCCIO7D_HPS					D6								
		VCCIO7D_HPS					S8								
		VCCIO8A					E7								
		VCCPD3A					AD10								
		VCCPD3A					AA14								
		VCCPD3A					AD13								
		VCCPD3A					AD16								
		VCCPD3A					AD18								
		VCCPD3A					AD21								
		VCCPD3A					AD8								
		VCCPD3A					Y21								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U072	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPD6MB_HPS					K21								
		VCCPD6MB_HPS					K24								
		VCCPD6MB_HPS					U04								
		VCCPD6MB_HPS					P21								
		VCCPD6MB_HPS					P24								
		VCCPD7A_HPS					E21								
		VCCPD7B_HPS					E17								
		VCCPD7C_HPS					E14								
		VCCPD7D_HPS					E18								
		VCCPD8A					E10								
3A	VREFB3AND	VREFB3AND					A65								
3B	VREFB3BND	VREFB3BND					AF12								
4A	VREFB4AND	VREFB4AND					AF16								
5A	VREFB5AND	VREFB5AND					AC26								
		VREFB7A/B/C/D/E/HPS					D19								
8A	VREFB8AND	VREFB8AND					D6								
		NC					W25								
		NC					AK25								
		NC					W35								
		NC					W39								
		VCCRSTCLK_HPS					F29								
		RREF_TL					B1								
		VCCA_FPLL					HS								
		VCCA_FPLL					P4								
		VCCA_FPLL					Q4								
		VCCA_FPLL					U5								
		VCCA_FPLL					J4								
		VCCA_FPLL					AK21								
		VCCA_FPLL					M2								
		VCCA_FPLL					R4								
		VCC_AUX					AC24								
		VCC_AUX					AC3								
		VCC_AUX					AD15								
		VCC_AUX					E15								
		VCC_AUX					F8								
		VCC_AUX_SHARED					F21								
		VCCRLL_HPS					HC3								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M15								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N15								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:

(1) For more information about pin definitions and pin connection guidelines, refer to the

[Cyclone V Device Family Pin Connection Guidelines](#).

(2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.

(3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSEMA2 Device
Version 1.2

Version Number	Date	Changes Made
1.0	7/8/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.