



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BA	VREFBSA0	IO	CLK6p,FPLL_TL_FBp		DIFFIO_RX_T9p	DIFFOUT_T9p	C6							
BA	VREFBSA0	IO	CLK6p,FPLL_TL_FBn		DIFFIO_RX_T9n	DIFFOUT_T9n	C5							
BA		MSEL0		MSEL0			R4							
BA		CONF_DONE		CONF_DONE			A3							
BA		MSEL1		MSEL1			E4							
BA		STATUS		STATUS			B3							
BA		HCE		HCE			A2							
BA		MSEL2		MSEL2			A1							
BA		MSEL3		MSEL3			C4							
BA		KCONFIG		KCONFIG			B2							
BA		MSEL4		MSEL4			C2							
		GND					C1							
		GND					A14							
		GND					A4							
		GND					AA14							
		GND					AA4							
		GND					AB1							
		GND					AB11							
		GND					AB21							
		GND					B1							
		GND					B11							
		GND					B21							
		GND					B6							
		GND					C16							
		GND					C3							
		GND					C8							
		GND					D1							
		GND					D16							
		GND					E1							
		GND					E12							
		GND					E2							
		GND					E22							
		GND					E3							
		GND					F14							
		GND					F19							
		GND					F2							
		GND					F3							
		GND					F4							
		GND					F9							
		GND					G1							
		GND					G16							
		GND					G2							
		GND					G4							
		GND					G5							
		GND					G8							
		GND					H13							
		GND					H2							
		GND					H4							
		GND					H5							
		GND					J10							
		GND					J20							
		GND					J3							
		GND					J5							
		GND					J7							
		GND					K1							
		GND					K11							
		GND					K13							
		GND					K17							
		GND					K2							
		GND					K4							
		GND					K6							
		GND					K8							
		GND					K9							
		GND					L10							
		GND					L12							
		GND					L14							
		GND					L2							
		GND					L3							
		GND					L5							
		GND					L7							
		GND					L8							
		GND					M1							
		GND					M11							
		GND					M2							
		GND					M21							
		GND					M4							
		GND					M8							
		GND					M9							
		GND					N1							
		GND					N10							
		GND					N12							
		GND					N16							
		GND					N2							
		GND					N3							
		GND					N5							
		GND					N6							
		GND					N7							
		GND					N8							
		GND					P11							
		GND					P15							
		GND					P2							
		GND					P4							
		GND					P6							
		GND					P9							
		GND					R1							
		GND					R12							
		GND					R14							
		GND					R2							
		GND					R22							
		GND					R3							
		GND					R5							
		GND					R7							
		GND					R9							
		GND					T1							
		GND					T13							
		GND					T15							
		GND					T19							
		GND					T2							
		GND					T4							
		GND					T6							
		GND					T8							
		GND					U11							
		GND					U12							
		GND					U13							
		GND					U14							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3DDR2 (9)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U15							
		GND					U16							
		GND					U17							
		GND					U3							
		GND					U5							
		GND					U6							
		GND					U9							
		GND					V1							
		GND					V13							
		GND					V3							
		GND					V8							
		GND					W10							
		GND					W15							
		GND					W20							
		GND					Y1							
		GND					Y17							
		GND					Y2							
		GND					Y7							
		GND					R16							
		GND					P13							
		VCC					R8							
		VCC					J4							
		VCC					J6							
		VCC					J8							
		VCC					R3							
		VCC					R5							
		VCC					R7							
		VCC					L4							
		VCC					L6							
		VCC					M3							
		VCC					M5							
		VCC					M7							
		VCC					M8							
		VCC					M4							
		VCC					M6							
		VCC					P3							
		VCC					P5							
		VCC					P7							
		VCC					P9							
		VCC					R4							
		VCC					R8							
		VCC					R8							
		VCC					T3							
		VCC					T5							
		VCC					T7							
		VCC					PT7							
		DNU					J2							
		DNU					H1							
		DNU					W2							
		DNU					Y3							
		DNU					C17							
		DNU					G8							
		VCCPGM					Y4							
		VCCPGM					Y18							
		VCCPGM					D4							
		VCCBAT					D2							
		VCCD3A					AB6							
		VCCD3A					W5							
		VCCD3B					AA9							
		VCCD4A					AB18							
		VCCD4A					Y12							
		VCCD6A					V18							
		VCCD6A					Y22							
		VCCD6A_HPS					D20							
		VCCD6A_HPS					E17							
		VCCD6A_HPS					G21							
		VCCD6A_HPS					H18							
		VCCD6A_HPS					J15							
		VCCD6A_HPS					K22							
		VCCD6A_HPS					L13							
		VCCD6A_HPS					L19							
		VCCD6B_HPS					M16							
		VCCD6B_HPS					N13							
		VCCD6B_HPS					P20							
		VCCD6B_HPS					R17							
		VCCD6B_HPS					T14							
		VCCD6B_HPS					U21							
		VCCD7A_HPS					A19							
		VCCD7A_HPS					B16							
		VCCD7B_HPS					C13							
		VCCD7B_HPS					G11							
		VCCD7C_HPS					D10							
		VCCD7D_HPS					A9							
		VCCD7D_HPS					E7							
		VCCD8A					D5							
		VCCPD3A					Y6							
		VCCPD3B4A					AA12							
		VCCPD3B4A					V12							
		VCCPD3B4A					V14							
		VCCPD3B4A					W13							
		VCCPD3B4A					W8							
		VCCPD5A					T16							
		VCCPD6AB_HPS					H16							
		VCCPD6AB_HPS					J17							
		VCCPD6AB_HPS					L17							
		VCCPD6AB_HPS					M16							
		VCCPD7A_HPS					G13							
		VCCPD7B_HPS					F12							
		VCCPD7C_HPS					E10							
		VCCPD7D_HPS					C9							
		VCCPD8A					D8							
3A	VREFB3AN0	VREFB3AN0					AB4							
3B	VREFB3BN0	VREFB3BN0					AA10							
4A	VREFB4AN0	VREFB4AN0					AA20							
5A	VREFB5AN0	VREFB5AN0					AB16							
	VREFB7A7B7C7DNO_HPS	VREFB7A7B7C7DNO_HPS					B17							
8A	VREFB8AN0	VREFB8AN0					B5							
		NC					G3							
		NC					H3							
		NC					R10							
		NC					R11							
		NC					T10							
		NC					T11							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		NC					T12							
		NC					T9							
		VCCRSTCLK_HPS					D16							
		RREF_TL					J1							
		VCCA_FPLL					L1							
		VCCA_FPLL					P1							
		VCCA_FPLL					U1							
		VCCA_FPLL					W1							
		VCCA_FPLL					F1							
		VCCA_FPLL					P17							
		VCC_ALIX					AA17							
		VCC_ALIX					AA3							
		VCC_ALIX					D3							
		VCC_ALIX					D9							
		VCC_ALIX					Y10							
		VCC_ALIX_SHARED					E16							
		VCCPLL_HPS					F16							
		VCC_HPS					R13							
		VCC_HPS					R10							
		VCC_HPS					R12							
		VCC_HPS					L11							
		VCC_HPS					L9							
		VCC_HPS					M10							
		VCC_HPS					M12							
		VCC_HPS					N11							
		VCC_HPS					N9							
		VCC_HPS					P10							
		VCC_HPS					P12							

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
- (2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
- (3) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (Z)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD25								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE18								
		GND					AE2								
		GND					AE3								
		GND					AF24								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH20								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B25								
		GND					B27								
		GND					B3								
		GND					B5								
		GND					B7								
		GND					C1								
		GND					C11								
		GND					C3								
		GND					D10								
		GND					D15								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					G1								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H18								
		GND					H20								
		GND					H24								
		GND					H27								
		GND					H3								
		GND					H4								
		GND					H5								
		GND					H6								
		GND					J1								
		GND					J2								
		GND					J3								
		GND					J5								
		GND					J9								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K4								
		GND					K6								
		GND					L1								
		GND					L10								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								
		GND					L3								
		GND					L5								
		GND					L8								
		GND					L9								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M5								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N4								
		GND					P10								
		GND					P12								
		GND					P15								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P9								
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R2								
		GND					R3								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U2								



Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (Z)	HMC Pin Assignment for LPDDR2	HPS Pin Max Select 3	HPS Pin Max Select 2	HPS Pin Max Select 1	HPS Pin Max Select 0
		GND					U17								
		GND					U2								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U3								
		GND					U8								
		GND					V14								
		GND					V3								
		GND					V8								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W18								
		GND					W2								
		GND					W3								
		GND					W4								
		GND					Y12								
		GND					Y4								
		GND					Y20								
		GND					Y25								
		GND					Y5								
		GND					Y6								
		GND					Y21								
		VCC					J1								
		VCC					K13								
		VCC					K15								
		VCC					L1								
		VCC					L12								
		VCC					L16								
		VCC					M12								
		VCC					M13								
		VCC					M16								
		VCC					M8								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N6								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P15								
		VCC					R10								
		VCC					R13								
		VCC					R14								
		VCC					R9								
		VCC					T13								
		VCC					T3								
		VCC					L4								
		VCC					T4								
		VCC					U5								
		VCC					N5								
		VCC					R5								
		VCC					T5								
		VCC					U26								
		DNV					A2								
		DNV					B2								
		DNV					D1								
		DNV					D2								
		DNV					H1								
		DNV					H2								
		DNV					M1								
		DNV					M2								
		DNV					T1								
		DNV					T2								
		DNV					Y1								
		DNV					Y2								
		DNV					AD1								
		DNV					AD2								
		DNV					U8								
		DNV					AE14								
		DNV					D23								
		DNV					E12								
		VCCP6M					Y10								
		VCCP6M					AD24								
		VCCP6M					H10								
		VCCBAT					D7								
		VCCIO3A					AA5								
		VCCIO3A					W9								
		VCCIO3B					AA12								
		VCCIO3B					AE10								
		VCCIO3B					AE13								
		VCCIO3B					AE4								
		VCCIO3A					AA16								
		VCCIO3A					AE21								
		VCCIO3A					AF14								
		VCCIO3A					AF19								
		VCCIO3A					AG12								
		VCCIO3A					AG22								
		VCCIO3A					AH15								
		VCCIO3A					AH25								
		VCCIO3A					W13								
		VCCIO3A					AC26								
		VCCIO3A					H17								
		VCCIO3B					W25								
		VCCIO3A_HPS					C25								
		VCCIO3A_HPS					C27								
		VCCIO3A_HPS					F27								
		VCCIO3A_HPS					G24								
		VCCIO3A_HPS					H21								
		VCCIO3A_HPS					H26								
		VCCIO3A_HPS					L26								
		VCCIO3A_HPS					M21								
		VCCIO3B_HPS					AD27								
		VCCIO3B_HPS					P27								
		VCCIO3B_HPS					T21								
		VCCIO3B_HPS					T26								
		VCCIO3B_HPS					U19								
		VCCIO3B_HPS					W27								
		VCCIO3A_HPS					C20								
		VCCIO3A_HPS					D19								
		VCCIO3B_HPS					B13								
		VCCIO3B_HPS					H14								
		VCCIO3C_HPS					B10								
		VCCIO3D_HPS					D8								
		VCCIO3D_HPS					G5								
		VCCIO3A					E7								
		VCCPD3A					AA10								
		VCCPD3B4A					AA14								
		VCCPD3B4A					AD13								
		VCCPD3B4A					AD16								
		VCCPD3B4A					AD18								
		VCCPD3B4A					AD21								
		VCCPD3B4A					AD9								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		WCCPD6A					V21								
		WCCPD6B					W19								
		WCCPD6AMB_HPS					K21								
		WCCPD6AMB_HPS					K20								
		WCCPD6AMB_HPS					M24								
		WCCPD6AMB_HPS					P21								
		WCCPD6AMB_HPS					P20								
		WCCPD7A_HPS					E21								
		WCCPD7B_HPS					E17								
		WCCPD7C_HPS					E14								
		WCCPD7D_HPS					E13								
		WCCPD8A					E10								
		WCCPD9A					A65								
3A	VREFB3AND	VREFB3AND					AF12								
3B	VREFB3BND	VREFB3BND					AF12								
4A	VREFB4AND	VREFB4AND					AF16								
5A	VREFB5AND	VREFB5AND					AC06								
6B	VREFB6BND	VREFB6BND					AA25								
	VREFB7A/B/C/DND_HPS	VREFB7A/B/C/DND_HPS					D19								
8A	VREFB8AND	VREFB8AND					D8								
		WCCRSTCLK_HPS					F22								
		RREF_TL					B1								
		WCCA_FPLL					K5								
		WCCA_FPLL					P4								
		WCCA_FPLL					U4								
		WCCA_FPLL					W5								
		WCCA_FPLL					J6								
		WCCA_FPLL					AA21								
		WCCA_FPLL					M6								
		WCCA_FPLL					R4								
		WCC_AUX					AC21								
		WCC_AUX					AC8								
		WCC_AUX					AD15								
		WCC_AUX					E16								
		WCC_AUX					F8								
		WCC_AUX_SHARED					F21								
		WCCPLL_HPS					K23								
		WCC_HPS					U21								
		WCC_HPS					K17								
		WCC_HPS					L16								
		WCC_HPS					L16								
		WCC_HPS					M17								
		WCC_HPS					M18								
		WCC_HPS					M19								
		WCC_HPS					N16								
		WCC_HPS					N18								
		WCC_HPS					P17								
		WCC_HPS					P19								

Notes:

(1) For more information about pin definitions and pin connection guidelines, refer to the

[Cyclone V Device Family Pin Connection Guidelines](#).

(2) HPS, DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.

(3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSEBA5 Device
Version 1.5

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS.
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	1/4/2016	Removed the USB0 pin from Pin List U19.
1.5	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.