Pin Information for the Cyclone® V 5CGXFC4 Device
Version 1.3
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
GXB_L1		REFCLK1Ln					E20	
GXB_L1		REFCLK1Lp					E21	
GXB_L1		GXB_TX_L5n					G21	
GXB_L1		GXB_TX_L5p					H21	
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					F18	
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					G18	
GXB_L0		GXB_TX_L2n					K21	
GXB_L0		GXB_TX_L2p					L21	
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					J18	
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					K18	
GXB_L0		GXB_TX_L1n					N21	
GXB_L0		GXB_TX_L1p					P21	
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					M18	
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					N18	
GXB_L0		GXB_TX_L0n					T21	
GXB_L0		GXB_TX_L0p					U21	
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					R18	
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					T18	
GXB_L0		REFCLK0Lp					U19	
GXB_L0		REFCLK0Ln					V20	
3A		TDO		TDO			Y21	
3A		nCSO		DATA4			W19	
3A		TMS		TMS			Y20	
3A		AS_DATA3		DATA3			W20	
3A		TCK		TCK			V19	
3A		AS_DATA2		DATA2			Y19	
3A		TDI		TDI			AA21	
3A		AS_DATA1		DATA1			W21	
3A		DCLK		DCLK			AA20	
3A		AS_DATA0,ASDO		DATA0			AA19	
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AA18	DQ1B
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	V17	
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AA17	DQ1B
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V16	DQ1B
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	Y16	DQSn1B
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	V15	DQ1B
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AA16	DQS1B
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W16	
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	Y15	DQ1B
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	V9	DQ1B
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AA15	DQ1B
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V10	DQ1B
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	W14	
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	V11	DQ1B
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	Y14	
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	V12	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	Y13	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	W13	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AA13	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	AA12	
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AA11	DQ3B
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	W4	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AA10	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	Y10	DQSn3B
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	V5	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	Y11	DQS3B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	U5	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	W6	DQ3B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	V4	DQ3B
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	V6	DQ3B
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	U4	
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	V7	DQ3B
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	U3	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	W7	DQ3B
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	T2	
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	R3	
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	T3	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	R4	
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	Y8	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	Y9	
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AA8	
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AA7	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	AA6	
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y6	
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AA5	
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	Y5	
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	Y4	
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	Y3	
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AA3	
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	AA2	
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AA1	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	Y1	
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	W1	
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	W2	
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	V1	
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	V2	
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	M4	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	R1	
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	M3	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	P2	
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	J4	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	M2	
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	J3	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	L2	
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	G3	
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	N1	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	H4	
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	N2	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	K4	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	P3	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	K3	
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	N4	
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L1	
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	E4	
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	K1	
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	E3	
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	H1	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	F3	
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	J2	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	G4	
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	H2	
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	G2	
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	E5	
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	F1	
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	E1	
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	F2	
		GND					D2	
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	C1	
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	C2	
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	A1	
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	B2	
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	A2	
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	A3	
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	B3	
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C4	
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	A5	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	B4	
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	C5	
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	D6	
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	B5	
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C6	
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	A6	
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D7	
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	A7	
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	B7	
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	D9	
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	A8	
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C7	
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	B8	
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D8	
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	C12	
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	D14	DQ6T
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	D11	
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	D13	DQ6T
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	C10	DQ6T
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	C17	DQ6T
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	B11	DQ6T
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	D17	DQ6T
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	A10	DQS6T
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	B10	DQSn6T
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	D16	DQ6T
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	B12	DQ6T
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C16	DQ6T
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	A13	DQ6T
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	A11	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	A12	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	B13	
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	B14	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	A15	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	B15	
9A		MSEL0		MSEL0			A17	
9A		CONF_DONE		CONF_DONE			A16	
9A		MSEL1		MSEL1			A19	
9A		nSTATUS		nSTATUS			A18	
9A		nCE		nCE			A20	
9A		MSEL2		MSEL2			A21	
9A		MSEL3		MSEL3			B20	
9A		nCONFIG		nCONFIG			D19	
9A		MSEL4		MSEL4			B19	
		GND					C19	
		GND					M21	
		GND					M9	
		GND					A9	
		GND					D10	
		GND					J19	
		GND					K13	
		GND					J10	
		GND					M11	
		GND					G20	
		GND					F19	
		GND					A4	
		GND					J12	
		GND					W5	
		GND					U18	
		GND					H20	
		GND					P18	
		GND					V13	
		GND					N12	
		GND					M1	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
		GND					R19	
		GND					L4	
		GND					K11	
		GND					P20	
		GND					D15	
		GND					N10	
		GND					L18	
		GND					F4	
		GND					M13	
		GND					B16	
		GND					W10	
		GND					E2	
		GND					U20	
		GND					L20	
		GND					H18	
		GND					B1	
		GND					K9	
		GND					E18	
		GND					D21	
		GND					H3	
		GND					R21	
		GND					K19	
		GND					G19	
		GND					F21	
		GND					U1	
		GND					J21	
		GND					T19	
		GND					M19	
		GND					D5	
		GND					V21	
		GND					T4	
		GND					V8	
		GND					C18	
		GND					AA14	
		GND					T20	
		GND					V3	
		GND					N20	
		GND					N19	
		GND					K20	
		GND					B21	
		VCC					L9	
		VCC					N11	
		VCC					L13	
		VCC					J9	
		VCC					J11	
		VCC					M10	
		VCC					L12	
		VCC					M12	
		VCC					K10	
		VCC					N13	
		VCC					L10	
		VCC					K12	
		VCC					N9	
		VCC					L11	
		VCC					J13	
		DNU					C20	
		DNU					D20	
		DNU					D4	
		DNU					D12	
		VCCPGM					Y18	
		VCCPGM					T1	
		VCCPGM					B17	
		VCCBAT					D18	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M301	DQS for X8
		VCCIO3A					W15	
		VCCIO3A					Y17	
		VCCIO3B					AA9	
		VCCIO3B					Y12	
		VCCIO4A					Y2	
		VCCIO4A					AA4	
		VCCIO4A					Y7	
		VCCIO5A					R2	
		VCCIO5A					N3	
		VCCIO5B					G1	
		VCCIO5B					K2	
		VCCIO7A					C8	
		VCCIO7A					B6	
		VCCIO7A					C3	
		VCCIO8A					A14	
		VCCIO8A					C13	
		VCCPD3A					W17	
		VCCPD3B4A					V14	
		VCCPD3B4A					W9	
		VCCPD5A					P1	
		VCCPD5B					J1	
		VCCPD7A8A					C14	
		VCCPD7A8A					B9	
3A	VREFB3AN0	VREFB3AN0					V18	
3B	VREFB3BN0	VREFB3BN0					W12	
4A	VREFB4AN0	VREFB4AN0					W8	
5A	VREFB5AN0	VREFB5AN0					P4	
5B	VREFB5BN0	VREFB5BN0					L3	
7A	VREFB7AN0	VREFB7AN0					C9	
8A	VREFB8AN0	VREFB8AN0					C15	
		VCCH_GXBL					M20	
		VCCH_GXBL					E19	
		VCCL_GXBL					J20	
		VCCL_GXBL					R20	
		RREF_TL					C21	
		VCCA_FPLL					U17	
		VCCA_FPLL					E17	
		VCCA_FPLL					U2	
		VCCA_FPLL					D1	
		VCC_AUX					B18	
		VCC_AUX					W18	
		VCC_AUX					C11	
		VCC_AUX					W11	
		VCC_AUX					D3	
		VCC_AUX					W3	
		VCCE_GXBL					P19	
		VCCE_GXBL					L19	
		VCCE_GXBL					F20	
		VCCE_GXBL					H19	

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					G23			
GXB_L1		REFCLK1Lp					H24			
GXB_L1		GXB_TX_L5n					F25			
GXB_L1		GXB_TX_L5p					G25			
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					E22			
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					F22			
GXB_L1		GXB_TX_L4n					J25			
GXB_L1		GXB_TX_L4p					K25			
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					H22			
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					J22			
GXB_L1		GXB_TX_L3n					M25			
GXB_L1		GXB_TX_L3p					N25			
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L22			
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					M22			
GXB_L0		GXB_TX_L2n					R25			
GXB_L0		GXB_TX_L2p					T25			
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					P22			
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R22			
GXB_L0		GXB_TX_L1n					V25			
GXB_L0		GXB_TX_L1p					W25			
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					U22			
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					V22			
GXB_L0		GXB_TX_L0n					AA25			
GXB_L0		GXB_TX_L0p					AB25			
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					Y22			
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA22			
GXB_L0		REFCLK0Lp					AC24			
GXB_L0		REFCLK0Ln					AC23			
3A		TDO		TDO			AD25			
3A		nCSO		DATA4			AD24			
3A		TMS		TMS			AE25			
3A		AS_DATA3		DATA3			AE24			
3A		TCK		TCK			AC22			
3A		AS_DATA2		DATA2			AB21			
3A		TDI		TDI			AD23			
3A		AS_DATA1		DATA1			AE21			
3A		DCLK		DCLK			AE22			
3A		AS_DATA0,ASDO		DATA0			AE23			
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AE18	DQ1B		
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AE20			
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AD19	DQ1B		
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD21	DQ1B		
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	AD18	DQSn1B		
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB20	DQ1B		
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AC17	DQS1B		
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AB19			
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AE17	DQ1B		
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AC19	DQ1B		
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AD16	DQ1B		
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AC18	DQ1B		
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AE16			
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AB17	DQ1B		
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	AE15			
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AA17	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AA16			
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AC16			
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AB15			
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	AD15			
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	AD14			
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AB14			
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AE13	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AA14	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AE12	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AE11	DQSn2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AD13	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AE10	DQS2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AC14			
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB12	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AD11	DQ2B		
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AA12	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AC12	DQ2B		
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	AD10			
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AB11	DQ2B		
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	AD9			
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AA11	DQ2B		
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB10			
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AE8	DQ3B		
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AA9	DQ3B		
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AD8	DQ3B		
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AC9	DQSn3B		
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AB9	DQ3B		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AC8	DQS3B		
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AA8			
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AC7	DQ3B		
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AE6	DQ3B		
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AC6	DQ3B		
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AD6	DQ3B		
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	AE5			
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AC4	DQ3B		
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	AD5			
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AB5	DQ3B		
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC3			
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AE3	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AB4	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AE2	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AD4	DQSn4B		
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA4	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	AD3	DQS4B		
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AA3			
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	W3	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AE1	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	V4	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AD1	DQ4B		
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	AC2			
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	Y3	DQ4B		
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	AC1			
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	W4	DQ4B		
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AB2			
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	AB1			
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AA2			
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	Y2			
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	Y1			
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	W1			
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U2	DQ1R		
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V2			
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U1	DQ1R		
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V1			
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T4	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	R2	DQ1R		
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R3	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	T2	DQ1R		
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	P3			
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	P1	DQS1R		
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	N2	DQ1R		
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R1	DQSn1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	N4	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	M1	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	N3			
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	N1	DQ1R		
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L2			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M2			
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	K2			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	M4			
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	K1			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	L3			
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	H1			
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	J4			
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	J1			
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	J3			
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	H2			
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	H4			
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	G1			
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	H3			
		GND					F3			
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	E1		GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	D1		GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	F2			
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E2			
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	F4		T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E3			
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D3			
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	C1			
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C7	DQ1T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	B1			
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C6	DQ1T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C3	DQ1T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D4	DQ1T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C2	DQ1T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	C4	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	B2	DQS1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	D8		T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	A2	DQSn1T	T_DQS#_1	T_DQS#_1

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C8	DQ1T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	A4	DQ1T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	B5	DQ1T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	A3	DQ1T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	B4		GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	B6			
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	E8	DQ2T	T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	A5			
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	D9	DQ2T	T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	B7	DQ2T	T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	E10	DQ2T	T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	A7	DQ2T	T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D10	DQ2T	T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	A9	DQS2T	T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	E11		T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	A8	DQSn2T	T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	D11	DQ2T	T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	B9	DQ2T	T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ2T	T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	A10	DQ2T	T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B10			
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	B12			
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	E13	DQ3T	T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	A12			
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	D14	DQ3T	T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	A14	DQ3T	T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	E15	DQ3T	T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	A13	DQ3T	T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	D15	DQ3T	T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	C13	DQS3T	T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	E17		T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	C12	DQSn3T	T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E16	DQ3T	T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	C14	DQ3T	T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C16	DQ3T	T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	B14	DQ3T	T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	B15		GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	B16			
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	E18	DQ4T	T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	A15			
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	D19	DQ4T	T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	B17	DQ4T	T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	C19	DQ4T	T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	A17	DQ4T	T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	C18	DQ4T	T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	A19	DQS4T	T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	C21		T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	A18	DQSn4T	T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	B20	DQ4T	T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	B19	DQ4T	T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	D21	DQ4T	T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	A20	DQ4T	T_A_15	
9A		MSEL0		MSEL0			A23			
9A		CONF_DONE		CONF_DONE			A22			
9A		MSEL1		MSEL1			A24			
9A		nSTATUS		nSTATUS			B22			
9A		nCE		nCE			A25			
9A		MSEL2		MSEL2			B25			
9A		MSEL3		MSEL3			B24			
9A		nCONFIG		nCONFIG			C23			
9A		MSEL4		MSEL4			C24			
		GND					C22			
		GND					A1			
		GND					A11			
		GND					AA1			
		GND					AA10			
		GND					AA15			
		GND					AA23			
		GND					AB13			
		GND					AB24			
		GND					AC10			
		GND					P25			
		GND					AC25			
		GND					AC5			
		GND					AD17			
		GND					AD22			
		GND					AE14			
		GND					AE19			
		GND					AE4			
		GND					B13			
		GND					B18			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					B23			
		GND					B8			
		GND					C25			
		GND					C5			
		GND					D12			
		GND					D17			
		GND					D2			
		GND					D22			
		GND					D7			
		GND					E14			
		GND					E23			
		GND					E25			
		GND					E4			
		GND					F24			
		GND					G3			
		GND					H25			
		GND					R23			
		GND					K4			
		GND					L1			
		GND					L12			
		GND					L14			
		GND					M11			
		GND					M13			
		GND					M15			
		GND					M23			
		GND					P11			
		GND					P13			
		GND					P15			
		GND					R12			
		GND					R14			
		GND					R24			
		GND					T22			
		GND					T24			
		GND					U23			
		GND					U25			
		GND					V23			
		GND					V24			
		GND					Y23			
		GND					Y25			
		GND					AB22			
		GND					F23			
		GND					AA24			
		GND					G22			
		GND					G24			
		GND					H23			
		GND					J23			
		GND					J24			
		GND					K22			
		GND					K24			
		GND					L23			
		GND					L25			
		GND					M24			
		GND					N22			
		GND					N24			
		GND					P23			
		GND					T1			
		GND					U3			
		GND					W22			
		GND					W24			
		GND					Y4			
		VCC					L11			
		VCC					L13			
		VCC					L15			
		VCC					M12			
		VCC					M14			
		VCC					N11			
		VCC					N12			
		VCC					N13			
		VCC					N14			
		VCC					N15			
		VCC					P12			
		VCC					P14			
		VCC					R11			
		VCC					R13			
		VCC					R15			
		DNU					D24			
		DNU					E24			
		DNU					G2			
		DNU					B11			
		VCCPGM					AC21			
		VCCPGM					T3			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCPGM					D20			
		VCCBAT					B21			
		VCCIO3A					AB18			
		VCCIO3A					AC20			
		VCCIO3B					AC15			
		VCCIO3B					AD12			
		VCCIO3B					AE9			
		VCCIO4A					AB3			
		VCCIO4A					AB8			
		VCCIO4A					AD2			
		VCCIO4A					AD7			
		VCCIO4A					W2			
		VCCIO5A					P2			
		VCCIO5A					R4			
		VCCIO5B					J2			
		VCCIO5B					M3			
		VCCIO7A					A6			
		VCCIO7A					B3			
		VCCIO7A					C10			
		VCCIO7A					E9			
		VCCIO7A					F1			
		VCCIO8A					A16			
		VCCIO8A					A21			
		VCCIO8A					C15			
		VCCIO8A					C20			
		VCCPD3A					AB16			
		VCCPD3B4A					AB7			
		VCCPD3B4A					AC13			
		VCCPD5A					P4			
		VCCPD5B					L4			
		VCCPD7A8A					D13			
		VCCPD7A8A					D16			
		VCCPD7A8A					D6			
3A	VREFB3AN0	VREFB3AN0					AD20			
3B	VREFB3BN0	VREFB3BN0					AC11			
4A	VREFB4AN0	VREFB4AN0					AE7			
5A	VREFB5AN0	VREFB5AN0					V3			
5B	VREFB5BN0	VREFB5BN0					K3			
7A	VREFB7AN0	VREFB7AN0					C9			
8A	VREFB8AN0	VREFB8AN0					C17			
		VCCH_GXBL					L24			
		VCCH_GXBL					U24			
		VCCL_GXBL					K23			
		VCCL_GXBL					T23			
		RREF_TL					D25			
		VCCA_FPLL					AB23			
		VCCA_FPLL					D23			
		VCCA_FPLL					U4			
		VCCA_FPLL					G4			
		VCC_AUX					AA13			
		VCC_AUX					AA18			
		VCC_AUX					AB6			
		VCC_AUX					D18			
		VCC_AUX					D5			
		VCC_AUX					E12			
		VCCE_GXBL					N23			
		VCCE_GXBL					P24			
		VCCE_GXBL					W23			
		VCCE_GXBL					Y24			

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					F5				
GXB_L1		REFCLK1Lp					G4				
GXB_L1		GXB_TX_L5n					D3				
GXB_L1		GXB_TX_L5p					D4				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1				
GXB_L1		GXB_TX_L4n					E1				
GXB_L1		GXB_TX_L4p					E2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
GXB_L1		GXB_TX_L3n					J1				
GXB_L1		GXB_TX_L3p					J2				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
GXB_L0		GXB_TX_L2n					N1				
GXB_L0		GXB_TX_L2p					N2				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				
GXB_L0		GXB_TX_L1n					U1				
GXB_L0		GXB_TX_L1p					U2				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1				
GXB_L0		GXB_TX_L0n					Y3				
GXB_L0		GXB_TX_L0p					Y4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1				
GXB_L0		REFCLK0Lp					V4				
GXB_L0		REFCLK0Ln					U4				
3A		TDO		TDO			M5				
3A		nCSO		DATA4			R4				
3A		TMS		TMS			P5				
3A		AS_DATA3		DATA3			T4				
3A		TCK		TCK			V5				
3A		AS_DATA2		DATA2			AA5				
3A		TDI		TDI			W5				
3A		AS_DATA1		DATA1			AB3				
3A		DCLK		DCLK			V3				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	R6	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AB6			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	V9	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AB5	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	V10	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	P8	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	N8	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AA8	DQ2B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	T9	DQ2B		B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AB8	DQ2B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	U10	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	M8				
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AA10	DQ2B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	M9				
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AA9	DQ2B		B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10			GND	GND

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	T10	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	Y9	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	R9	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	U11	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	R12	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	U12	DQS3B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	P12			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	R10	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	R11	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P9				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	Y11	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	N9				
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AA12	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB13				
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	V13	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AB12	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	U13	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	T12	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AA14	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	T13	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AA13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	Y14	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AA15	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	Y15	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V14				
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AB17	DQ4B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	V15				
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AB18	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AB20			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y16	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AB21	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	Y17	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	T14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA17	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	U15	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AA18			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA19	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	V20	DQ5B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AA20	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	W19	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	V16				
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AB22	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	W16				
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AA22	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	Y22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	Y20	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	W22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y19	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	P14	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	Y21	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	R14	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	W21			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	U22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	V19	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	V21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	V18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	U16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	U21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	U17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	U20	DQ6B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	T19	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	T18				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	T20	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	T17				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21				
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	P18				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P17	DQ1R			
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	N16				
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	N20	DQ2R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M16				
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	N21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	N19	DQ2R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	M22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	M18	DQ2R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	L22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	K17	DQS2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	M20				
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	L17	DQSn2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	M21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	L19	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	K21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	L18	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	K22				
7A		GND					F17				
7A	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	E21	DQ1T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	G21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	D21	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E19	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	C20	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	D19	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	B20	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	J21	DQS1T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B18			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	J22	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	B17	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	C21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	G22	DQ1T	DQ1T	T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	B21	DQ1T	DQ1T	T_DQ_32	T_DQ_32
7A	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	F22			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	E22	DQ2T	DQ1T	T_DM_3	T_DM_3
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	H20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	D22	DQ2T	DQ1T	T_DQ_31	T_DQ_31
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C19	DQ2T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	B22	DQ2T	DQ1T	T_DQ_30	T_DQ_30
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C18	DQ2T	DQ1T	T_DQ_28	T_DQ_28
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	A22	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	F19	DQS2T	DQ1T	T_DQS_3	T_DQS_3
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	E20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	F18	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	F20	DQ2T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	A18	DQ2T	DQ1T	T_DQ_25	T_DQ_25
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A20	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	A17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A19			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	K20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	B16	DQ3T	DQ2T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	K19			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C16	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D17	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	G17	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E16	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	G16	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G18	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J19			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	H18	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	J18	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E15	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A15	DQ3T	DQ2T	T_DQ_18	T_DQ_18

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	F15	DQ3T	DQ2T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A14			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	H16				
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	J17	DQ4T	DQ2T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	H15				
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	K16	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C15	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	G15	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	B15	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F14	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	H14	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B13			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J13	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A13	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E14	DQ4T	DQ2T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	J11	DQ4T	DQ2T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	F13	DQ4T	DQ2T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	H10			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H13				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	G11	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G13				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	F12	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ5T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	B12	DQ5T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ5T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	A12	DQ5T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H11	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	L8			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G12	DQSn5T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	K9	DQ5T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	D12	DQ5T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ5T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	E12	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B11				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	L7	DQ6T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	K7	DQ6T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	J7	DQ6T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	H8	DQ6T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	J8	DQ6T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	G8	DQ6T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	A10			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	H9	DQSn6T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	A9	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	B10	DQ6T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	A5	DQ6T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ6T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	B5			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	E10				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	B6	DQ7T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	F9				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	B7	DQ7T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	A8	DQ7T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	C6	DQ7T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	A7	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	D6	DQ7T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	E9	DQS7T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	D7			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	D9	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	C8	DQ7T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	G6	DQ7T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	F7	DQ7T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	H6	DQ7T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E7			GND	GND
9A		MSEL0		MSEL0			L6				
9A		CONF_DONE		CONF_DONE			K6				
9A		MSEL1		MSEL1			J6				
9A		nSTATUS		nSTATUS			H5				
9A		nCE		nCE			G5				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			F3				
9A		GND					C5				
		GND					AB19				
		GND					AB14				
		GND					AB9				
		GND					AB2				
		GND					AB1				
		GND					AA11				
		GND					AA6				
		GND					AA4				
		GND					AA3				
		GND					Y18				
		GND					Y5				
		GND					Y2				
		GND					Y1				
		GND					W4				
		GND					W3				
		GND					V22				
		GND					V17				
		GND					V12				
		GND					V7				
		GND					V2				
		GND					V1				
		GND					U9				
		GND					U5				
		GND					U3				
		GND					T21				
		GND					T16				
		GND					T2				
		GND					T1				
		GND					R13				
		GND					R3				
		GND					P10				
		GND					P4				
		GND					P2				
		GND					P1				
		GND					N22				
		GND					N17				
		GND					N15				
		GND					N13				
		GND					N11				
		GND					N7				
		GND					N5				
		GND					N3				
		GND					M14				
		GND					M12				
		GND					M10				
		GND					M4				
		GND					M2				
		GND					M1				
		GND					L21				
		GND					L15				
		GND					L13				
		GND					L11				
		GND					L5				
		GND					L3				
		GND					K14				
		GND					K12				
		GND					K10				
		GND					K8				
		GND					K4				
		GND					K2				
		GND					K1				
		GND					J20				
		GND					J15				
		GND					J5				
		GND					J3				
		GND					H22				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					H12				
		GND					H7				
		GND					H4				
		GND					H3				
		GND					H2				
		GND					H1				
		GND					G19				
		GND					G9				
		GND					G3				
		GND					F16				
		GND					F6				
		GND					F2				
		GND					F1				
		GND					E13				
		GND					E4				
		GND					E3				
		GND					D20				
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C17				
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B9				
		GND					B2				
		GND					B1				
		GND					A21				
		GND					A11				
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
		VCC					N10				
		VCC					M15				
		VCC					M13				
		VCC					M11				
		VCC					L16				
		VCC					L14				
		VCC					L12				
		VCC					L10				
		VCC					K15				
		VCC					K13				
		VCC					K11				
		VCC					J16				
		VCC					J14				
		VCC					J12				
		VCC					J10				
		DNU					B3				
		DNU					B4				
		DNU					E17				
		DNU					L9				
		VCCPGM					V8				
		VCCPGM					R19				
		VCCPGM					F8				
		VCCBAT					A3				
		VCCIO3A					T6				
		VCCIO3A					Y8				
		VCCIO3B					Y13				
		VCCIO3B					W10				
		VCCIO3B					T11				
		VCCIO3B					R8				
		VCCIO4A					U19				
		VCCIO4A					AA21				
		VCCIO4A					AA16				
		VCCIO4A					W20				
		VCCIO4A					W15				
		VCCIO4A					U14				
		VCCIO5A					R18				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCIO5A					P20				
		VCCIO5B					M19				
		VCCIO5B					K18				
		VCCIO7A					B19				
		VCCIO7A					H17				
		VCCIO7A					G14				
		VCCIO7A					F21				
		VCCIO7A					F11				
		VCCIO7A					E18				
		VCCIO7A					D15				
		VCCIO7A					C22				
		VCCIO7A					C12				
		VCCIO7A					A16				
		VCCIO8A					A6				
		VCCIO8A					G7				
		VCCIO8A					E8				
		VCCIO8A					C7				
		VCCPD3A					W6				
		VCCPD3B4A					W17				
		VCCPD3B4A					W14				
		VCCPD3B4A					W12				
		VCCPD3B4A					W11				
		VCCPD5A					P21				
		VCCPD5B					N18				
		VCCPD5B					M17				
		VCCPD7A8A					E11				
		VCCPD7A8A					D16				
		VCCPD7A8A					D14				
		VCCPD7A8A					D8				
		VCCPD7A8A					C10				
3A	VREFB3AN0	VREFB3AN0					Y7				
3B	VREFB3BN0	VREFB3BN0					Y12				
4A	VREFB4AN0	VREFB4AN0					AB16				
5A	VREFB5AN0	VREFB5AN0					R20				
5B	VREFB5BN0	VREFB5BN0					L20				
7A	VREFB7AN0	VREFB7AN0					C14				
8A	VREFB8AN0	VREFB8AN0					B8				
		NC					Y6				
		NC					V11				
		VCCH_GXBL					M3				
		VCCH_GXBL					T3				
		VCCL_GXBL					P3				
		VCCL_GXBL					K3				
		RREF_TL					A1				
		VCCA_FPLL					T5				
		VCCA_FPLL					F4				
		VCCA_FPLL					U18				
		VCCA_FPLL					H19				
		VCC_AUX					E6				
		VCC_AUX					D18				
		VCC_AUX					W18				
		VCC_AUX					W13				
		VCC_AUX					W7				
		VCC_AUX					D11				
		VCCE_GXBL					L4				
		VCCE_GXBL					N4				
		VCCE_GXBL					K5				
		VCCE_GXBL					J4				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					G4				
GXB_L1		REFCLK1Lp					F5				
GXB_L1		GXB_TX_L5n					D3				
GXB_L1		GXB_TX_L5p					D4				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1				
GXB_L1		GXB_TX_L4n					E1				
GXB_L1		GXB_TX_L4p					E2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
GXB_L1		GXB_TX_L3n					J1				
GXB_L1		GXB_TX_L3p					J2				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
GXB_L0		GXB_TX_L2n					N1				
GXB_L0		GXB_TX_L2p					N2				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				
GXB_L0		GXB_TX_L1n					U1				
GXB_L0		GXB_TX_L1p					U2				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1				
GXB_L0		GXB_TX_L0n					Y3				
GXB_L0		GXB_TX_L0p					Y4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1				
GXB_L0		REFCLK0Lp					V4				
GXB_L0		REFCLK0Ln					U4				
3A		TDO		TDO			V3				
3A		nCSO		DATA4			AB6				
3A		TMS		TMS			R4				
3A		AS_DATA3		DATA3			AA5				
3A		TCK		TCK			V5				
3A		AS_DATA2		DATA2			T5				
3A		TDI		TDI			P5				
3A		AS_DATA1		DATA1			W5				
3A		DCLK		DCLK			M5				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	L8	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	V8			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	N8	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	W8	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	M8	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	N9	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	N10	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	Y7	DQ2B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	U8	DQ2B		B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	W7	DQ2B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	V9	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	R9				
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AB8	DQ2B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	P9				
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AA8	DQ2B		B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10			GND	GND

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AA9	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AA10	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	Y9	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	L9	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	W11	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	M10	DQS3B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	Y11			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	U10	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	U11	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	T10				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	R11	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	R10				
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	P12	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AA13				
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	W12	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AB13	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y12	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	U12	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	R12	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	T12	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	T13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	W13	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AB16	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	V13	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	T14				
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AB18	DQ4B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U13				
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AA18	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AA19			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y14	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	Y19	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	W14	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	P14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA20	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	R14	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	Y20			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA15	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U15	DQ5B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	Y15	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	V15	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	R15				
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AB20	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	T15				
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AB21	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	Y16	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AA22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U16	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AA17	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	U17	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AB17			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	Y22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	V18	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	Y21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	W18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	W16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	W21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	W17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	W22	DQ6B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	T20	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	T18	DQ1R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	T22				
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	R20	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	R21				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R			
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT_R9p	M16				
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	E21	DQ2R			
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	M17				
5B	VREFB5BN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	D22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	L19	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	K21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	L20	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	J21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	L15	DQS2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	G22				
5B	VREFB5BN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	K15	DQSn2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	G21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	L18	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	G20	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	K19	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	H21				
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L17				
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	E20	DQ3R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	K17				
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	F20	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	H20	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	G18	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	H19	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	G17	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	K16	DQS3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	F19				
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	J16	DQSn3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	F18	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	J17	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	J19	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	J18	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	H18				
7A		GND					F17				
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C21	DQ1T	DQ1T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	G16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C20	DQ1T	DQ1T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D18	DQ1T	DQ1T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B20	DQ1T	DQ1T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E17	DQ1T	DQ1T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B21	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G15	DQS1T	DQS1T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B22			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	G14	DQSn1T	DQSn1T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	A22	DQ1T	DQ1T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E16	DQ1T	DQ1T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A20	DQ1T	DQ1T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D17	DQ1T	DQ1T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A19			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	G13				
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C19	DQ2T	DQ1T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	F14				
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C18	DQ2T	DQ1T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C16	DQ2T	DQ1T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	B16	DQ2T	DQ1T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C15	DQ2T	DQ1T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B15	DQ2T	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	G12	DQS2T	DQ1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	A18			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	H12	DQSn2T	DQ1T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A17	DQ2T	DQ1T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F15	DQ2T	DQ1T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	B18	DQ2T	DQ1T	T_DQ_10	T_DQ_10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E14	DQ2T	DQ1T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	B17			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H10				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	A15	DQ3T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A14	DQ3T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ3T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C14	DQ3T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ3T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D14	DQ3T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H9	DQS3T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	A13			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G8	DQSn3T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	B13	DQ3T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E12	DQ3T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	B12	DQ3T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	F12	DQ3T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	A12				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	C11	DQ4T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B11	DQ4T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D11	DQ4T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A8	DQ4T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	E11	DQ4T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	A7	DQ4T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS4T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	F8			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	J8	DQSn4T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E7	DQ4T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	C10	DQ4T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C6	DQ4T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ4T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	D7			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	K7				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	A10	DQ5T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	J7				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	A9	DQ5T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	D9	DQ5T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	B6	DQ5T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	D8	DQ5T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	B5	DQ5T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	H8	DQS5T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	C8			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	G7	DQSn5T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	B8	DQ5T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	H6	DQ5T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	E6	DQ5T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	G6	DQ5T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	F7			GND	GND
9A		MSEL0		MSEL0			L6				
9A		CONF_DONE		CONF_DONE			J6				
9A		MSEL1		MSEL1			K6				
9A		nSTATUS		nSTATUS			G5				
9A		nCE		nCE			H5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			C5				
9A		GND					F3				
		GND					F21				
		GND					AB19				
		GND					AB2				
		GND					AB1				
		GND					AA16				
		GND					AA11				
		GND					AA4				
		GND					AA3				
		GND					Y13				
		GND					Y8				
		GND					Y5				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					Y2				
		GND					Y1				
		GND					W20				
		GND					W4				
		GND					W3				
		GND					V22				
		GND					V17				
		GND					V2				
		GND					V1				
		GND					U19				
		GND					U14				
		GND					U9				
		GND					U5				
		GND					U3				
		GND					T11				
		GND					T2				
		GND					T1				
		GND					R13				
		GND					R3				
		GND					P10				
		GND					P4				
		GND					P2				
		GND					P1				
		GND					N22				
		GND					N15				
		GND					N13				
		GND					N11				
		GND					N7				
		GND					N5				
		GND					N3				
		GND					M19				
		GND					M14				
		GND					M12				
		GND					M9				
		GND					M4				
		GND					M2				
		GND					M1				
		GND					L16				
		GND					L13				
		GND					L11				
		GND					L5				
		GND					L3				
		GND					K14				
		GND					K12				
		GND					K10				
		GND					K8				
		GND					K4				
		GND					K2				
		GND					K1				
		GND					J20				
		GND					J15				
		GND					J13				
		GND					J11				
		GND					J5				
		GND					J3				
		GND					H14				
		GND					H4				
		GND					H3				
		GND					H2				
		GND					H1				
		GND					G9				
		GND					G3				
		GND					F16				
		GND					F11				
		GND					F6				
		GND					F2				
		GND					F1				
		GND					E13				
		GND					E4				
		GND					E3				
		GND					D20				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C22				
		GND					C17				
		GND					C7				
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B2				
		GND					B1				
		GND					A21				
		GND					A11				
		GND					A5				
		VCC					J14				
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
		VCC					M15				
		VCC					M13				
		VCC					M11				
		VCC					L14				
		VCC					L12				
		VCC					L10				
		VCC					K13				
		VCC					K11				
		VCC					K9				
		VCC					J12				
		VCC					J10				
		VCC					H15				
		VCC					H13				
		VCC					H11				
		DNU					B3				
		DNU					B4				
		DNU					D21				
		DNU					E10				
		VCCPGM					Y6				
		VCCPGM					U20				
		VCCPGM					B7				
		VCCBAT					A3				
		VCCIO3A					T6				
		VCCIO3A					AA6				
		VCCIO3B					V7				
		VCCIO3B					AB9				
		VCCIO3B					W10				
		VCCIO3B					R8				
		VCCIO4A					T16				
		VCCIO4A					AB14				
		VCCIO4A					AA21				
		VCCIO4A					Y18				
		VCCIO4A					W15				
		VCCIO4A					V12				
		VCCIO5A					T21				
		VCCIO5A					R18				
		VCCIO5B					H22				
		VCCIO5B					P20				
		VCCIO5B					N17				
		VCCIO5B					L21				
		VCCIO5B					K18				
		VCCIO5B					G19				
		VCCIO7A					B19				
		VCCIO7A					H17				
		VCCIO7A					E18				
		VCCIO7A					D15				
		VCCIO7A					C12				
		VCCIO7A					A16				
		VCCIO8A					E8				
		VCCIO8A					H7				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCIO8A					B9				
		VCCIO8A					A6				
		VCCPD3A					V6				
		VCCPD3B4A					V16				
		VCCPD3B4A					W9				
		VCCPD3B4A					V14				
		VCCPD3B4A					V10				
		VCCPD5A					P17				
		VCCPD5B					N19				
		VCCPD5B					M18				
		VCCPD7A8A					F13				
		VCCPD7A8A					F9				
		VCCPD7A8A					E15				
		VCCPD7A8A					E9				
3A	VREFB3AN0	VREFB3AN0					W6				
3B	VREFB3BN0	VREFB3BN0					AB12				
4A	VREFB4AN0	VREFB4AN0					AA14				
5A	VREFB5AN0	VREFB5AN0					V21				
5B	VREFB5BN0	VREFB5BN0					K20				
7A	VREFB7AN0	VREFB7AN0					D16				
8A	VREFB8AN0	VREFB8AN0					B10				
		NC					AB3				
		NC					V11				
		NC					P22				
		NC					P21				
		NC					P18				
		NC					P16				
		NC					N21				
		NC					N20				
		NC					N18				
		NC					N16				
		NC					M22				
		NC					M21				
		NC					M20				
		NC					L22				
		NC					K22				
		NC					J22				
		NC					F22				
		NC					E22				
		VCCH_GXBL					T3				
		VCCH_GXBL					M3				
		VCCL_GXBL					P3				
		VCCL_GXBL					K3				
		RREF_TL					A1				
		VCCA_FPLL					T4				
		VCCA_FPLL					F4				
		VCCA_FPLL					U18				
		VCCA_FPLL					E19				
		VCC_AUX					D6				
		VCC_AUX					D12				
		VCC_AUX					D19				
		VCC_AUX					W19				
		VCC_AUX					AA12				
		VCC_AUX					AB5				
		VCCE_GXBL					L4				
		VCCE_GXBL					N4				
		VCCE_GXBL					K5				
		VCCE_GXBL					J4				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					P6				
GXB_L1		REFCLK1Lp					N7				
GXB_L1		GXB_TX_L5n					K1				
GXB_L1		GXB_TX_L5p					K2				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					M2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					M1				
GXB_L1		GXB_TX_L4n					P1				
GXB_L1		GXB_TX_L4p					P2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					T2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					T1				
GXB_L1		GXB_TX_L3n					W3				
GXB_L1		GXB_TX_L3p					W4				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					V2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					V1				
GXB_L0		GXB_TX_L2n					AA3				
GXB_L0		GXB_TX_L2p					AA4				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y1				
GXB_L0		GXB_TX_L1n					AC3				
GXB_L0		GXB_TX_L1p					AC4				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB1				
GXB_L0		GXB_TX_L0n					AE3				
GXB_L0		GXB_TX_L0p					AE4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD1				
GXB_L0		REFCLK0Lp					V6				
GXB_L0		REFCLK0Ln					W6				
3A		TDO		TDO			V7				
3A		nCSO		DATA4			Y6				
3A		TMS		TMS			R6				
3A		AS_DATA3		DATA3			U6				
3A		TCK		TCK			Y5				
3A		AS_DATA2		DATA2			AB5				
3A		TDI		TDI			T6				
3A		AS_DATA1		DATA1			AD5				
3A		DCLK		DCLK			N8				
3A		AS_DATA0,ASDO		DATA0			AF5				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	T7	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	T8	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V8	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	W8	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB6	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	Y9	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA6				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	R9	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	R8				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AD6	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	P8				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD7	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	U9			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	Y11	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	T9	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	W11	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	T11	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AC10	DQ2B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	R11	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB10			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AC8	DQ2B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AB11	DQ2B		B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AC9	DQ2B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AB12	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	T12				
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	Y10	DQ2B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	T13				
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	W10	DQ2B		B_CAS#	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	V9			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AE8	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	V10	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AD8	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	P10	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AF9	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	N10	DQS3B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AE9			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AF8	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	U11	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AF7	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	U10	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P12				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AF6	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	P11				
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE6	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AE11				
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AA14	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AD11	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y14	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	W13	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AD12	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	V13	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AD13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AE10	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	Y13	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AD10	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	W12	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V12				
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AF12	DQ4B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U12				
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AF11	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC13			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AC15	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AC14	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AB15	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	V14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AF13	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	U14	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AE13			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AF14	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AB16	DQ5B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AE14	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AA16	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	Y16				
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AF18	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	Y15				
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AE18	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AD18			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AD16	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AC18	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AD17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	W15	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AF19	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	V15	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AE19			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AF22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AC17	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AF21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AB17	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	U17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AE21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	T17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AE20	DQ6B	DQ1B	B_DM_2	B_DM_2
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AD20			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AE15	DQ7B	DQ2B	B_DQ_24	B_DQ_24
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AC20	DQ7B	DQ2B	B_DQ_26	B_DQ_26
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AE16	DQ7B	DQ2B	B_DQ_25	B_DQ_25
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	W17	DQSn7B	DQ2B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AD21	DQ7B	DQ2B	B_DQ_27	B_DQ_27

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	W16	DQS7B	DQ2B	B_DQS_3	B_DQS_3
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AD22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AE23	DQ7B	DQ2B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AF16	DQ7B	DQ2B	B_DQ_28	B_DQ_28
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AD23	DQ7B	DQ2B	B_DQ_30	B_DQ_30
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AF17	DQ7B	DQ2B	B_DQ_29	B_DQ_29
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	U16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AF23	DQ7B	DQ2B	B_DQ_31	B_DQ_31
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	U15			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AE24	DQ7B	DQ2B	B_DM_3	B_DM_3
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AF24			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AA18	DQ8B	DQ2B	B_DQ_32	B_DQ_32
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AE25	DQ8B	DQ2B	B_DQ_34	B_DQ_34
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	Y18	DQ8B	DQ2B	B_DQ_33	B_DQ_33
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	V17	DQSn8B	DQSn2B	B_DQS#_4	B_DQS#_4
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AE26	DQ8B	DQ2B	B_DQ_35	B_DQ_35
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	V18	DQS8B	DQS2B	B_DQS_4	B_DQS_4
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AD26			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AC19	DQ8B	DQ2B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	Y19	DQ8B	DQ2B	B_DQ_36	B_DQ_36
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AB19	DQ8B	DQ2B	B_DQ_38	B_DQ_38
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	Y20	DQ8B	DQ2B	B_DQ_37	B_DQ_37
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	W18			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AA21	DQ8B	DQ2B	B_DQ_39	B_DQ_39
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	V19			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AB22	DQ8B	DQ2B	B_DM_4	B_DM_4
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AC22	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	U19				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AC23	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V20				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AA22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	W20	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AA23	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	W21	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24				
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	V22	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB24	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	U22	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	Y23	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	T19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	Y24				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	U20	DQ1R			
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT_R9p	T21				
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	V23	DQ2R			
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	T22				
5B	VREFB5BN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	V24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	T23	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	AA24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	T24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	AB25	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	R23	DQS2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	AD25				
5B	VREFB5BN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	P23	DQSn2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AC25	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	R24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	U24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	R25	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	V25				
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	R20				
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	AB26	DQ3R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	P20				
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	AA26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	T26	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	Y25	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	R26	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	Y26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	P21	DQS3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	W25				
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	P22	DQSn3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	W26	DQ3R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	N25	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	U25	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	P26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	U26				
6A	VREFB6AN0	IO	CLK5p		DIFFIO_RX_R25p	DIFFOUT_R25p	N20				
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	J25	DQ4R			
6A	VREFB6AN0	IO	CLK5n		DIFFIO_RX_R25n	DIFFOUT_R25n	M21				
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	J26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	N24	DQ4R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R28p	DIFFOUT_R28p	F26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	M24	DQ4R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R28n	DIFFOUT_R28n	G26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	N23	DQS4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	G25				
6A	VREFB6AN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	M22	DQSn4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	H25	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	M25	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	D26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	M26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	E26				
6A	VREFB6AN0	IO	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	K25				
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	E24	DQ5R			
6A	VREFB6AN0	IO	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	K26				
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	E25	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	K24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R36p	F24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	K23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R36n	G24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	L23	DQS5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	H23				
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	L24	DQSn5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	H24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	H22	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	F23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	J23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	G22				
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R41p	L22				
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	B25	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R41n	K21				
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	B26	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	H19	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R44p	DIFFOUT_R44p	D25	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	H20	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R44n	DIFFOUT_R44n	C25	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	J20	DQS6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	D22				
6A	VREFB6AN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	J21	DQSn6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	E23	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	G20	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	E21	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	F21	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	F22				
7A		GND					D23				
7A	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H15			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	C23	DQ1T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	J16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	C22	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	B24	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	A23	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	A24	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	A22	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	H18	DQS1T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B22			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	H17	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	A21	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	D21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	B21	DQ1T	DQ1T	T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	D20	DQ1T	DQ1T	T_DQ_32	T_DQ_32
7A	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	B20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G16			GND	GND

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	C20	DQ2T	DQ1T	T_DM_3	T_DM_3
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	G17			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	B19	DQ2T	DQ1T	T_DQ_31	T_DQ_31
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	E20	DQ2T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C19	DQ2T	DQ1T	T_DQ_30	T_DQ_30
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	E19	DQ2T	DQ1T	T_DQ_28	T_DQ_28
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C18	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	J12	DQS2T	DQ1T	T_DQS_3	T_DQS_3
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	A19			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	J11	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	A18	DQ2T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	D18	DQ2T	DQ1T	T_DQ_25	T_DQ_25
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A17	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	D17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H14			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C17	DQ3T	DQ2T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	H13			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	B17	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	E18	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	A14	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	F18	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B14	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	L12	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B15			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	K11	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	C15	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	C14	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A8	DQ3T	DQ2T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D15	DQ3T	DQ2T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A9			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	G15				
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C9	DQ4T	DQ2T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	G14				
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	B9	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	E16	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D10	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D16	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	C10	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	N12	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B10			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	M12	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A11	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F16	DQ4T	DQ2T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	E10	DQ4T	DQ2T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E15	DQ4T	DQ2T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	E11			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H12				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B12	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A13	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	G12	DQ5T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	A12	DQ5T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F12	DQ5T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	B11	DQ5T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	M11	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	C13			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	L11	DQSn5T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	C12	DQ5T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E13	DQ5T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	D11	DQ5T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	D13	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D12				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	N9				
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	A5	DQ6T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	M10				
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B6	DQ6T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	H8	DQ6T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A7	DQ6T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	H9	DQ6T		T_A_5	T_CA_5

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	B7	DQ6T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	M9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	D6			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	L9	DQSn6T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E6	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	H10	DQ6T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	D7	DQ6T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	G10	DQ6T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	C7			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	L8				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	F6	DQ7T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	K9				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	G6	DQ7T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	K8	DQ7T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	G7	DQ7T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	J8	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	F7	DQ7T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	K10	DQS7T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	H7			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	J10	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	J7	DQ7T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	L7	DQ7T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	D8	DQ7T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	K6	DQ7T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E9			GND	GND
9A		MSEL0		MSEL0			M7				
9A		CONF_DONE		CONF_DONE			A6				
9A		MSEL1		MSEL1			L6				
9A		nSTATUS		nSTATUS			B5				
9A		nCE		nCE			D5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			K5				
9A		nCONFIG		nCONFIG			F5				
9A		MSEL4		MSEL4			J5				
9A		GND					H5				
		GND					V26				
		GND					A25				
		GND					D24				
		GND					H26				
		GND					L25				
		GND					P24				
		GND					AA25				
		GND					AC26				
		GND					AF25				
		GND					G23				
		GND					K22				
		GND					U23				
		GND					Y22				
		GND					AD24				
		GND					C21				
		GND					F20				
		GND					L20				
		GND					K19				
		GND					N21				
		GND					M19				
		GND					T20				
		GND					P19				
		GND					W19				
		GND					AC21				
		GND					AF20				
		GND					B18				
		GND					E17				
		GND					L18				
		GND					K17				
		GND					J18				
		GND					N18				
		GND					M17				
		GND					R18				
		GND					P17				
		GND					AB18				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					AE17				
		GND					A15				
		GND					D14				
		GND					H16				
		GND					L16				
		GND					L14				
		GND					K15				
		GND					J14				
		GND					N16				
		GND					N14				
		GND					M15				
		GND					T15				
		GND					R16				
		GND					R14				
		GND					P15				
		GND					V16				
		GND					AA15				
		GND					AD14				
		GND					G13				
		GND					K13				
		GND					K12				
		GND					M13				
		GND					R12				
		GND					P13				
		GND					U13				
		GND					Y12				
		GND					C11				
		GND					F10				
		GND					L10				
		GND					J9				
		GND					N11				
		GND					T10				
		GND					P9				
		GND					W9				
		GND					AC11				
		GND					AF10				
		GND					B8				
		GND					E7				
		GND					H6				
		GND					N6				
		GND					M8				
		GND					R7				
		GND					P7				
		GND					AB8				
		GND					AE7				
		GND					C5				
		GND					B4				
		GND					F4				
		GND					E5				
		GND					D4				
		GND					H4				
		GND					G5				
		GND					L4				
		GND					J4				
		GND					N4				
		GND					M5				
		GND					T5				
		GND					R4				
		GND					P5				
		GND					V5				
		GND					V4				
		GND					U4				
		GND					AA5				
		GND					Y4				
		GND					W5				
		GND					AC5				
		GND					AB4				
		GND					AF4				
		GND					AE5				
		GND					AD4				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					C2				
		GND					C1				
		GND					B3				
		GND					B2				
		GND					F3				
		GND					E2				
		GND					E1				
		GND					D3				
		GND					H3				
		GND					G2				
		GND					G1				
		GND					L2				
		GND					L1				
		GND					K3				
		GND					J2				
		GND					J1				
		GND					N2				
		GND					N1				
		GND					M3				
		GND					T3				
		GND					R2				
		GND					R1				
		GND					P3				
		GND					V3				
		GND					U2				
		GND					U1				
		GND					AA2				
		GND					AA1				
		GND					Y3				
		GND					W2				
		GND					W1				
		GND					AC2				
		GND					AC1				
		GND					AB3				
		GND					AF3				
		GND					AF2				
		GND					AE2				
		GND					AE1				
		GND					AD3				
		VCC					K20				
		VCC					L19				
		VCC					J19				
		VCC					N19				
		VCC					M20				
		VCC					R19				
		VCC					L17				
		VCC					K18				
		VCC					J17				
		VCC					N17				
		VCC					M18				
		VCC					T18				
		VCC					R17				
		VCC					P18				
		VCC					L15				
		VCC					K16				
		VCC					K14				
		VCC					J15				
		VCC					N15				
		VCC					M16				
		VCC					M14				
		VCC					T16				
		VCC					T14				
		VCC					R15				
		VCC					P16				
		VCC					P14				
		VCC					L13				
		VCC					J13				
		VCC					N13				
		VCC					R13				
		DNU					A4				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		DNU					A3				
		DNU					C24				
		DNU					F14				
		VCCPGM					AA9				
		VCCPGM					W22				
		VCCPGM					F8				
		VCCBAT					E8				
		VCCIO3A					Y7				
		VCCIO3A					AC6				
		VCCIO3B					U8				
		VCCIO3B					V11				
		VCCIO3B					AA10				
		VCCIO3B					AD9				
		VCCIO4A					U18				
		VCCIO4A					AE22				
		VCCIO4A					AA20				
		VCCIO4A					AD19				
		VCCIO4A					Y17				
		VCCIO4A					W14				
		VCCIO4A					AC16				
		VCCIO4A					AF15				
		VCCIO4A					AB13				
		VCCIO4A					AE12				
		VCCIO5A					V21				
		VCCIO5A					AB23				
		VCCIO5B					N26				
		VCCIO5B					T25				
		VCCIO5B					W24				
		VCCIO5B					R22				
		VCCIO6A					C26				
		VCCIO6A					F25				
		VCCIO6A					J24				
		VCCIO6A					E22				
		VCCIO6A					M23				
		VCCIO6A					H21				
		VCCIO7A					A10				
		VCCIO7A					B23				
		VCCIO7A					A20				
		VCCIO7A					D19				
		VCCIO7A					G18				
		VCCIO7A					C16				
		VCCIO7A					F15				
		VCCIO7A					B13				
		VCCIO7A					E12				
		VCCIO7A					H11				
		VCCIO8A					C6				
		VCCIO8A					D9				
		VCCIO8A					G8				
		VCCIO8A					K7				
		VCCPD3A					AB9				
		VCCPD3B4A					AB21				
		VCCPD3B4A					AA19				
		VCCPD3B4A					AA17				
		VCCPD3B4A					AA13				
		VCCPD3B4A					AA11				
		VCCPD5A					U21				
		VCCPD5B					N22				
		VCCPD5B					R21				
		VCCPD6A					J22				
		VCCPD6A					L21				
		VCCPD7A8A					F19				
		VCCPD7A8A					F17				
		VCCPD7A8A					F13				
		VCCPD7A8A					F11				
		VCCPD7A8A					F9				
3A	VREFB3AN0	VREFB3AN0					AC7				
3B	VREFB3BN0	VREFB3BN0					AC12				
4A	VREFB4AN0	VREFB4AN0					AD15				
5A	VREFB5AN0	VREFB5AN0					W23				
5B	VREFB5BN0	VREFB5BN0					P25				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
6A	VREFB6AN0	VREFB6AN0					L26				
7A	VREFB7AN0	VREFB7AN0					B16				
8A	VREFB8AN0	VREFB8AN0					C8				
		NC					AA12				
		NC					M6				
		NC					AB7				
		NC					C4				
		NC					E4				
		NC					G4				
		NC					L5				
		NC					C3				
		NC					F2				
		NC					F1				
		NC					E3				
		NC					D2				
		NC					D1				
		NC					H2				
		NC					H1				
		NC					G3				
		VCCH_GXBL					R3				
		VCCH_GXBL					T4				
		VCCH_GXBL					L3				
		VCCL_GXBL					J3				
		VCCL_GXBL					N3				
		VCCL_GXBL					U3				
		RREF_TL					B1				
		VCCA_FPLL					W7				
		VCCA_FPLL					J6				
		VCCA_FPLL					Y21				
		VCCA_FPLL					G21				
		VCC_AUX					G9				
		VCC_AUX					E14				
		VCC_AUX					G19				
		VCC_AUX					AB20				
		VCC_AUX					AB14				
		VCC_AUX					AA8				
		VCCE_GXBL					K4				
		VCCE_GXBL					N5				
		VCCE_GXBL					M4				
		VCCE_GXBL					R5				
		VCCE_GXBL					P4				
		VCCE_GXBL					U5				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Version Number	Date	Changes Made
1.0	11/29/2012	Initial release.
1.1	4/26/2013	- Added M301 package. - Updated the column from "HMC Pin Assignment for DDR3" to "HMC Pin Assignment for DDR3/DDR2". - Added note to the "HMC Pin Assignment for DDR3/DDR2" column.
1.2	7/4/2013	Added M383 package.
1.3	8/16/2013	Added nPERSTL0 to pin16 in F484 and U484 packages.