Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
QL1		GXB_TX7p			F4							
QL1		GXB_TX7n			F3							
QL1		GXB_RX7p			G2							
QL1		GXB_RX7n			G1							
QL1		GXB_TX6p			H4							
QL1		GXB_TX6n			H3							
QL1		GXB_RX6p			J2							
QL1		GXB_RX6n			J1							
QL1		GXB_TX5p			K4							
QL1		GXB_TX5n			K3							
QL1		GXB_RX5p			L2							
QL1		GXB_RX5n			L1							
QL1		GXB_TX4p			M4							
QL1		GXB_TX4n			M3							
QL1		GXB_RX4p			N2							
QL1		GXB_RX4n			N1							
QL0		GXB_TX3p			P4	F2						
QL0		GXB_TX3n			P3	F1						
QL0		GXB_RX3p			R2	H2						
QL0		GXB_RX3n			R1	H1						
QL0		GXB_TX2p			T4	K2						
QL0		GXB_TX2n			T3	K1						
QL0		GXB_RX2p			U2	M2						
QL0		GXB_RX2n			U1	M1						
QL0		GXB_TX1p			V4	P2						
QL0		GXB_TX1n			V3	P1						
QL0		GXB_RX1p			W2	T2						
QL0		GXB_RX1n			W1	T1						
QL0		GXB_TX0p			Y4	V2						
QL0		GXB_TX0n			Y3	V1						
QL0		GXB_RX0p			AA2	Y2						
QL0		GXB_RX0n			AA1	Y1						
B3		MSEL3		MSEL3	W7	P4						
B3		MSEL2		MSEL2	Y6	R5						
B3		MSEL1		MSEL1	Y7	P5						
B3		MSEL0		MSEL0	AA6	T6						
B3		CONF_DONE		CONF_DONE	AB6	U5						
B3		nSTATUS		nSTATUS	AA5	R8						
B3B	VREFB3N2	REFCLK0p	DIFFCLK_0p,CLKIO20		T9	M7						
B3B	VREFB3N2	REFCLK0n	DIFFCLK_0n		U9	N7						
B3B	VREFB3N2	REFCLK1p	DIFFCLK_1p,CLKIO22		T10	M8						
B3B	VREFB3N2	REFCLK1n	DIFFCLK_1n		U10	N8						
B3	VREFB3N2	IO	PLL1_CLKOUTp		AB5	T7						
B3	VREFB3N2	IO	PLL1_CLKOUTn		AC5	T8						
B3	VREFB3N2	IO	PLL5_CLKOUTp		AC4	U6						
B3	VREFB3N2	IO	PLL5_CLKOUTn		AD4	V6						
B3	VREFB3N2	IO	PLL6_CLKOUTp		AD3	U7						
B3	VREFB3N2	IO	PLL6_CLKOUTn		AE3	V7						
B3	VREFB3N2	IO		INIT_DONE	AB7	W8						
B3	VREFB3N2	IO	DIFFIO_B1p	DATA5	AE1	W4						
B3	VREFB3N2	IO	DIFFIO_B1n	DATA6	AE2	Y4						
B3	VREFB3N2	IO	DIFFIO_B2p	DATA7	AF2	R9						
B3	VREFB3N2	IO	DIFFIO_B2n		AF3	T9						
B3	VREFB3N2	IO	DIFFIO_B3p	CRC_ERROR	AC6	AA4						
B3	VREFB3N2	IO	DIFFIO_B3n	NCEO	AC7	AB3						
B3	VREFB3N2	IO	DIFFIO_B4p		AD7	P10	DM3B/BWS#3B	DM3B/BWS#3B	DM5B/BWS#5B			
B3	VREFB3N2	IO	DIFFIO_B4n		AD8	R10	DQ3B	DQ3B	DQ5B			
B3	VREFB3N2	IO	DIFFIO_B5p		AD5	W5	DQ3B	DQ3B	DQ5B	DM3B/BWS#3B	DM3B/BWS#3B	DM5B/BWS#5B
B3	VREFB3N2	IO	DIFFIO_B5n		AD6	Y5	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	VREFB3N2		AB9	V9						
B3	VREFB3N2	IO	DIFFIO_B6p		AC9	R11	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0
B3	VREFB3N2	IO	DIFFIO_B6n		AD9	T11	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B7p		AE5	W6	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B7n		AE6	Y6	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B8p		AF4	W7	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B8n		AF5	Y7	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B9p		AB11	AB4	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B9n		AC11	AB5	DM5B/BWS#5B	DM3B/BWS#3B	DM5B/BWS#5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B10p		AE7	AA6				DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B10n		AF6	AB6				DM5B/BWS#5B	DM3B/BWS#3B	DM5B/BWS#5B
B3	VREFB3N1	IO	DIFFIO_B11p		AB12	AA7	DQ5B	DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B11n		AC12	AB7	DQ5B	DQ3B	DQ5B			
B3	VREFB3N1	IO	VREFB3N1		AD11	W10						
B3	VREFB3N1	IO	DIFFIO_B12p		AC10	W9	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B12n		AD10	Y8	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1
B3	VREFB3N1	IO	DIFFIO_B13p		AF7	Y9				DQ5B	DQ3B	DQ5B

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B3	VREFB3N1	IO	DIFFIO_B13n		AF8	AA9	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B14p		AD12	AB8	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B14n		AE11	AB9	DQ5B	DQ3B	DQ5B			
B3	VREFB3N0	IO	DIFFIO_B15p		AE9	W11				DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B15n		AF9	Y11				DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B16p		AC13	Y10	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2
B3	VREFB3N0	IO	DIFFIO_B16n		AD13	AA10	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	VREFB3N0		AE13	U12						
B3	VREFB3N0	IO	DIFFIO_B17p		AE10	W12	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B17n		AF10	Y12	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B18p		AF11	AB10	DM4B	DM5B/BWS#5B	DM5B/BWS#5B	DM4B	DM5B/BWS#5B	DM5B/BWS#5B
B3	VREFB3N0	IO	DIFFIO_B18n		AF12	AB11		DQ5B	DQ5B		DQ5B	DQ5B
B3A	VREFB3N0	CLKIO12	DIFFCLK_7p,REFCLK2p		T14	M11						
B3A	VREFB3N0	CLKIO13	DIFFCLK_7n,REFCLK2n		T15	N11						
B4	VREFB4N2	CLKIO14	DIFFCLK_6p		AF13	AA12						
B4	VREFB4N2	CLKIO15	DIFFCLK_6n		AF14	AB12						
B4	VREFB4N2	IO	DIFFIO_B19p		AC14	R13	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B19n		AD14	T13	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3
B4	VREFB4N2	IO	DIFFIO_B20p		AE14	W13	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B20n		AE15	Y13	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B21p		AF15	AA13	DQ4B	DQ5B	DQ5B			
B4	VREFB4N2	IO	DIFFIO_B21n		AF16	AB13	DQ4B	DQ5B	DQ5B			
B4	VREFB4N2	IO	VREFB4N2		AB14	V13						
B4	VREFB4N2	IO	DIFFIO_B22p		AC16	AB14	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B22n		AD16	AB15	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B23p		AC17	W14	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B23n		AD17	Y14	DM2B	DM5B/BWS#5B	DM5B/BWS#5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B24p		AE17	R14						
B4	VREFB4N2	IO	DIFFIO_B24n		AF17	T14	DQ2B	DQ5B	DQ5B			
B4	VREFB4N1	IO	DIFFIO_B25p		AE18	W15				DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B25n		AF18	Y15				DM2B	DM5B/BWS#5B	DM5B/BWS#5B
B4	VREFB4N1	IO	DIFFIO_B26p		AC18	U14	DQ2B	DQ5B	DQ5B			
B4	VREFB4N1	IO	DIFFIO_B26n		AD18	U15	DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	VREFB4N1		AB18	W16						
B4	VREFB4N1	IO	DIFFIO_B27p		AC19	AA15	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4
B4	VREFB4N1	IO	DIFFIO_B27n		AD19	AB16						
B4	VREFB4N1	IO	DIFFIO_B28p		AE19	Y16				DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B28n		AF19	AA16	DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B29p		AF20	AB17	DQ2B	DQ5B	DQ5B			
B4	VREFB4N1	IO	DIFFIO_B29n		AF21	AB18	DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B30p		AD20	W17	DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B30n		AE21	Y17						
B4	VREFB4N1	IO	DIFFIO_B31p		AE22	Y18				DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B31n		AF22	AA18				DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B32p		AE23	R15						
B4	VREFB4N0	IO	DIFFIO_B32n		AF23	T15						
B4	VREFB4N0	IO	DIFFIO_B33p		AF24	AA19						
B4	VREFB4N0	IO	DIFFIO_B33n		AF25	AB19						
B4	VREFB4N0	IO	VREFB4N0		AC20	T16						
B4	VREFB4N0	IO	DIFFIO_B34p		AC22	AA20						
B4	VREFB4N0	IO	DIFFIO_B34n		AD22	AB20	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5
B4	VREFB4N0	IO	DIFFIO_B35p		AC21	AA21		DQ5B	DQ5B			
B4	VREFB4N0	IO	DIFFIO_B35n		AD21	AB21	DQ2B	DQ5B	DQ5B		DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B36p		AD23	W18						
B4	VREFB4N0	IO	DIFFIO_B36n		AD24	Y19				DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	PLL3_CLKOUTp		AA21	AA22						
B4	VREFB4N0	IO	PLL3_CLKOUTn		AB21	AB22						
B4	VREFB4N0	IO	RUP2		Y21	W19						
B4	VREFB4N0	IO	RDN2		AA22	Y20						
B5	VREFB5N2	IO	RUP3		Y22	T17						
B5	VREFB5N2	IO	RDN3		Y23	T18						
B5	VREFB5N2	IO	DIFFIO_R49n		AA24	R17	DM3R/BWS#3R	DM3R/BWS#3R	DM1R/BWS#1R	DM3R/BWS#3R	DM3R/BWS#3R	DM1R/BWS#1R
B5	VREFB5N2	IO	DIFFIO_R49p		AA23	R16	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6
B5	VREFB5N2	IO	DIFFIO_R48n		AB24							
B5	VREFB5N2	IO	DIFFIO_R48p		AB23							
B5	VREFB5N2	IO	VREFB5N2		W23	U18						
B5	VREFB5N2	IO	DIFFIO_R47n		AC24	W22	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R47p		AC23	Y22	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R46n		AE26	N15						
B5	VREFB5N2	IO	DIFFIO_R46p		AE25	P15						
B5	VREFB5N2	IO	DIFFIO_R45n		AD26	W21	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R45p		AD25	W20	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R44n	DEV_OE	W22	P14						
B5	VREFB5N2	IO	DIFFIO_R44p	DEV_CLRn	V21	P13						
B5	VREFB5N2	IO	DIFFIO_R43n		U23	V21	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R43p		V22	V20	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B5	VREFB5N1	IO	DIFFIO_R42n		V24	U20	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R42p		V23	T19						
B5	VREFB5N1	IO	DIFFIO_R41n		AC26	T20	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R41p		AC25	R19	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R40n		AB26	U22						
B5	VREFB5N1	IO	DIFFIO_R40p		AA25	V22	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7
B5	VREFB5N1	IO	DIFFIO_R39n		U22	R21						
B5	VREFB5N1	IO	DIFFIO_R39p		T21	R20	DM1R/BWS#1R	DM3R/BWS#3R	DM1R/BWS#1R	DM1R/BWS#1R	DM3R/BWS#3R	DM1R/BWS#1R
B5	VREFB5N1	IO	DIFFIO_R38n		Y25	T22						
B5	VREFB5N1	IO	DIFFIO_R38p		Y24	T21	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R37n		Y26							
B5	VREFB5N1	IO	DIFFIO_R37p		AA26							
B5	VREFB5N1	IO	VREFB5N1		U24	P20						
B5	VREFB5N1	IO	DIFFIO_R36n		T19	M15						
B5	VREFB5N1	IO	DIFFIO_R36p		U19	N14						
B5	VREFB5N1	IO	DIFFIO_R35n		W25	M14						
B5	VREFB5N1	IO	DIFFIO_R35p		W24	N13						
B5	VREFB5N1	IO	DIFFIO_R34n		V26	L15	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R34p		W26	L14						
B5	VREFB5N0	IO	DIFFIO_R33n		T23	P22	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R33p		T22	R22						
B5	VREFB5N0	IO	DIFFIO_R32n		U26	M17						
B5	VREFB5N0	IO	DIFFIO_R32p		U25	N17	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R31n		T25	L13						
B5	VREFB5N0	IO	DIFFIO_R31p		T24	M13	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R30n		R20	N20						
B5	VREFB5N0	IO	DIFFIO_R30p		R19	N19	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8
B5	VREFB5N0	IO	DIFFIO_R29n		T26	N22	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R29p		R25	N21	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R28n		R23							
B5	VREFB5N0	IO	DIFFIO_R28p		R22							
B5	VREFB5N0	IO	VREFB5N0		R24	M20						
B5	VREFB5N0	IO	DIFFIO_R27n		P20	L16						
B5	VREFB5N0	IO	DIFFIO_R27p		P19	M16						
B5	VREFB5N0	IO	DIFFIO_R26n		P24	M19	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R26p		P23	M18	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	CLKIO4	DIFFCLK_2n		P26	M22						
B5	VREFB5N0	CLKIO5	DIFFCLK_2p		R26	M21						
B6	VREFB6N2	CLKIO6	DIFFCLK_3n		N26	L22						
B6	VREFB6N2	CLKIO7	DIFFCLK_3p		N25	L21						
B6	VREFB6N2	IO	DIFFIO_R25n		N20	L20	DM0R	DM1R/BWS#1R	DM1R/BWS#1R	DM0R	DM1R/BWS#1R	DM1R/BWS#1R
B6	VREFB6N2	IO	DIFFIO_R25p		N19	L19	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R24n		N23							
B6	VREFB6N2	IO	DIFFIO_R24p		N22							
B6	VREFB6N2	IO	VREFB6N2		M23	J15						
B6	VREFB6N2	IO	DIFFIO_R23n		M24	J20	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R23p		N24	J19	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R22n		L19	H22	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9
B6	VREFB6N2	IO	DIFFIO_R22p		M19	J21						
B6	VREFB6N2	IO	DIFFIO_R21n		M26	J22						
B6	VREFB6N2	IO	DIFFIO_R21p		M25	K22	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R20n		L22	K20						
B6	VREFB6N2	IO	DIFFIO_R20p		M22	K19	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R19n		L26	H21						
B6	VREFB6N2	IO	DIFFIO_R19p		L25	H20	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R18n		L24	G21						
B6	VREFB6N2	IO	DIFFIO_R18p		L23	G20	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R17n		K26	E20						
B6	VREFB6N1	IO	DIFFIO_R17p		J26	F20						
B6	VREFB6N1	IO	DIFFIO_R16n		L21	F22	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R16p		K20	G22						
B6	VREFB6N1	IO	DIFFIO_R15n		J25	E22						
B6	VREFB6N1	IO	DIFFIO_R15p		K24	E21		DQ1R	DQ1R		DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R14n		H26	D22						
B6	VREFB6N1	IO	DIFFIO_R14p		H25	D21	DM2R	DM1R/BWS#1R	DM1R/BWS#1R	DM2R	DM1R/BWS#1R	DM1R/BWS#1R
B6	VREFB6N1	IO	DIFFIO_R13n		K22			DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R13p		K21		DQ2R	DQ1R	DQ1R			
B6	VREFB6N1	IO	VREFB6N1		J24	H17						
B6	VREFB6N1	IO	DIFFIO_R12n		F26	B22						
B6	VREFB6N1	IO	DIFFIO_R12p		G26	C22	DQ2R	DQ1R	DQ1R		DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R11n		J23	A22	DQ2R	DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R11p		K23	A21	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R10n		E26	D20	DQ2R	DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R10p		E25	D19	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R9n		D26	B21	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10
B6	VREFB6N1	IO	DIFFIO_R9p		D25	B20				DQ2R	DQ1R	DQ1R

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B6	VREFB6N1	IO	DIFFIO_R8n		G25	C20						
B6	VREFB6N1	IO	DIFFIO_R8p		H24	C19				DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R7n		H23	A20						
B6	VREFB6N1	IO	DIFFIO_R7p		H22	B19				DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R6n		G24	K17						
B6	VREFB6N0	IO	DIFFIO_R6p		F23	J16						
B6	VREFB6N0	IO	DIFFIO_R5n		E24							
B6	VREFB6N0	IO	DIFFIO_R5p		F24							
B6	VREFB6N0	IO	VREFB6N0		G23	G18						
B6	VREFB6N0	IO	DIFFIO_R4n		C26	K14						
B6	VREFB6N0	IO	DIFFIO_R4p		C25	K13						
B6	VREFB6N0	IO	DIFFIO_R3n		B26	H16	DQ2R	DQ1R	DQ1R			
B6	VREFB6N0	IO	DIFFIO_R3p		B25	H15	DQ2R	DQ1R	DQ1R			
B6	VREFB6N0	IO	DIFFIO_R2n		C24	G17				DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R2p		D24	G16	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11
B6	VREFB6N0	IO	DIFFIO_R1n		G22	G19				DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R1p		F21	F18				DQ2R	DQ1R	DQ1R
B7	VREFB7N0	IO	RUP4		E23	F16						
B7	VREFB7N0	IO	RDN4		D23	F17						
B7	VREFB7N0	IO	PLL4_CLKOUTn		E21	C17						
B7	VREFB7N0	IO	PLL4_CLKOUTp		E22	C18						
B7	VREFB7N0	IO			C23	B18						
B7	VREFB7N0	IO	DIFFIO_T37n		C22	A18	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T37p		D22	A19	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T36n		A23	D17						
B7	VREFB7N0	IO	DIFFIO_T36p		B23	E17						
B7	VREFB7N0	IO	VREFB7N0		E20	D16						
B7	VREFB7N0	IO	DIFFIO_T35n		A24	B16	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12
B7	VREFB7N0	IO	DIFFIO_T35p		A25	C16	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T34n		D20	A16				DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T34p		D21	A17						
B7	VREFB7N0	IO	DIFFIO_T33n		B22	C15	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T33p		C21	D15						
B7	VREFB7N1	IO	DIFFIO_T32n		C20	A15	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T32p		D19	B15				DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T31n		A22	C14	DQ2T	DQ5T	DQ5T			
B7	VREFB7N1	IO	DIFFIO_T31p		B21	D14	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T30n		A20	A13						
B7	VREFB7N1	IO	DIFFIO_T30p		A21	A14	DQ2T	DQ5T	DQ5T		DQ5T	DQ5T
B7	VREFB7N1	IO	VREFB7N1		E17	D13						
B7	VREFB7N1	IO	DIFFIO_T29n		B19	C12				DM2T	DM5T/BWS#5T	DM5T/BWS#5T
B7	VREFB7N1	IO	DIFFIO_T29p		C19	C13		DQ5T	DQ5T			
B7	VREFB7N1	IO	DIFFIO_T28n		C18	B12	DM2T	DM5T/BWS#5T	DM5T/BWS#5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T28p		D18	B13				DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T27n		A18	G14						
B7	VREFB7N1	IO	DIFFIO_T27p		A19	G15	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13
B7	VREFB7N1	IO	DIFFIO_T26n		D17	H14	DQ4T	DQ5T	DQ5T			
B7	VREFB7N1	IO	DIFFIO_T26p		E16	J14	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T25n		B18	J12						
B7	VREFB7N2	IO	DIFFIO_T25p		C17	K12	DQ4T	DQ5T	DQ5T			
B7	VREFB7N2	IO	DIFFIO_T24n		A16	C10	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T24p		A17	C11						
B7	VREFB7N2	IO	VREFB7N2		D16	F12						
B7	VREFB7N2	IO	DIFFIO_T23n		B17	H13	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T23p		C16	J13	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T22n		A15	A11	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T22p		B15	A12						
B7	VREFB7N2	IO	DIFFIO_T21n		D15	A10	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T21p		E15	B10	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14
B7	VREFB7N2	IO	DIFFIO_T20n		C14	G12		DQ5T	DQ5T		DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T20p		C15	H12	DM4T	DM5T/BWS#5T	DM5T/BWS#5T	DM4T	DM5T/BWS#5T	DM5T/BWS#5T
B7	VREFB7N2	CLKIO8	DIFFCLK_5n		A14	A9						
B7	VREFB7N2	CLKIO9	DIFFCLK_5p		B14	B9						
B8A	VREFB8N0	CLKIO10	DIFFCLK_4n,REFCLK3n		L14	J10						
B8A	VREFB8N0	CLKIO11	DIFFCLK_4p,REFCLK3p		L15	K10						
B8	VREFB8N0	IO	DIFFIO_T19n		A12	A8	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15
B8	VREFB8N0	IO	DIFFIO_T19p		A13	B7	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T18n		B13	A6						
B8	VREFB8N0	IO	DIFFIO_T18p		C13	A7				DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T17n		A11	A4	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T17p		B11	A5	DQ5T	DQ3T	DQ5T			
B8	VREFB8N0	IO	VREFB8N0		D14	D12						
B8	VREFB8N0	IO	DIFFIO_T16n		A10	A2	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T16p		B10	A3	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T15n		A8	B3	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T15p		A9	B4						

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B8	VREFB8N0	IO	DIFFIO_T14n		A6	B6	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T14p		A7	C6	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T13n		C11	A1						
B8	VREFB8N1	IO	DIFFIO_T13p		C12	B1	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T12n		A5	C8						
B8	VREFB8N1	IO	DIFFIO_T12p		B5	D8						
B8	VREFB8N1	IO	VREFB8N1		D11	D11						
B8	VREFB8N1	IO	DIFFIO_T11n		B6	C1	DM5T/BWS#5T	DM3T/BWS#3T	DM5T/BWS#5T	DM5T/BWS#5T	DM3T/BWS#3T	DM5T/BWS#5T
B8	VREFB8N1	IO	DIFFIO_T11p		B7	C2						
B8	VREFB8N1	IO	DIFFIO_T10n		A4	C7	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16
B8	VREFB8N1	IO	DIFFIO_T10p		B4	D7	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T9n		B9	C3						
B8	VREFB8N1	IO	DIFFIO_T9p		C10	C4	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T8n		A2	E8	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T8p		A3	F8						
B8	VREFB8N2	IO	DIFFIO_T7n		C4	C5	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T7p		C5	D4						
B8	VREFB8N2	IO	DIFFIO_T6n		D9	D5	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T6p		D10	E5	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17
B8	VREFB8N2	IO	VREFB8N2		E9	D10						
B8	VREFB8N2	IO	DIFFIO_T5n		B1	C9				DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T5p		B2	D9				DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T4n		C3	D6	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T4p		D3	E6	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T3n		C2	G7	DQ3T	DQ3T	DQ5T			
B8	VREFB8N2	IO	DIFFIO_T3p		D2	H7	DQ3T	DQ3T	DQ5T			
B8	VREFB8N2	IO	DIFFIO_T2n	DATA4	C6	F6	DM3T/BWS#3T	DM3T/BWS#3T	DM5T/BWS#5T	DM3T/BWS#3T	DM3T/BWS#3T	DM5T/BWS#5T
B8	VREFB8N2	IO	DIFFIO_T2p	DATA3	C7	G6						
B8	VREFB8N2	IO	DIFFIO_T1n	DATA2	C8	G8						
B8	VREFB8N2	IO	DIFFIO_T1p		C9	H8						
B8	VREFB8N2	IO	PLL2_CLKOUTn		D7	G10						
B8	VREFB8N2	IO	PLL2_CLKOUTp		E7	H9						
B8	VREFB8N2	IO	PLL7_CLKOUTn		C1							
B8	VREFB8N2	IO	PLL7_CLKOUTp		D1							
B8	VREFB8N2	IO	PLL8_CLKOUTn		E1							
B8	VREFB8N2	IO	PLL8_CLKOUTp		E2							
B8	VREFB8N2	IO		CLKUSR	D4	G11						
B8B	VREFB8N2	REFCLK4n	DIFFCLK_8n		K10							
B8B	VREFB8N2	REFCLK4p	DIFFCLK_8p,CLKIO17		L10							
B8B	VREFB8N2	REFCLK5n	DIFFCLK_9n		K9							
B8B	VREFB8N2	REFCLK5p	DIFFCLK_9p,CLKIO19		L9							
B9	VREFB8N2	IO		DATA0	D6	K4						
B9	VREFB8N2	IO		DATA1,ASDO	E6	D1						
B9	VREFB8N2	IO		NCSO	D5	J4						
B9		DCLK		DCLK	F6	D3						
B9		nCONFIG		nCONFIG	E5	H4						
B9		nCE		nCE	H7	D2						
B9		TDI		TDI	G6	F5						
B9		TCK		TCK	G8	E4						
B9		TMS		TMS	F5	G5						
B9		TDO		TDO	H8	E3						
		GND			J7	F3						
		GND			K6	M3						
		GND			N6	T4						
		GND			P6	U3						
		GND			U6	V19						
		GND			V7	E19						
		GND			W20	H5						
		GND			G20	AA11						
		GND			AB10	AA14						
		GND			AB13	AA17						
		GND			AB16	AA5						
		GND			AB19	AA8						
		GND			AB22	B11						
		GND			AB25	B14						
		GND			AE12	B17						
		GND			AE16	B2						
		GND			AE20	B5						
		GND			AE24	B8						
		GND			AE4	C21						
		GND			AE8	D18						
		GND			B12	E7						
		GND			B16	F11						
		GND			B20	F13						
		GND			B24	F15						
		GND			B3	F21						

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		GND			B8	F9						
		GND			F10	H11						
		GND			F12	H18						
		GND			F17	J6						
		GND			F19	J8						
		GND			F22	K11						
		GND			F25	K15						
		GND			F7	K21						
		GND			G13	K5						
		GND			H19	K7						
		GND			J22	K9						
		GND			J8	L10						
		GND			K11	L12						
		GND			K15	L18						
		GND			K17	L6						
		GND			K25	L8						
		GND			L12	M5						
		GND			L16	M9						
		GND			L18	N10						
		GND			L8	N4						
		GND			M11	N6						
		GND			M13	P11						
		GND			M15	P16						
		GND			M17	P18						
		GND			M21	P21						
		GND			M9	P9						
		GND			N10	R12						
		GND			N12	R6						
		GND			N14	U10						
		GND			N16	U17						
		GND			N18	U21						
		GND			N8	V11						
		GND			P11	V14						
		GND			P13	V5						
		GND			P15	V8						
		GND			P17	Y21						
		GND			P22	AA1						
		GND			P25	AA2						
		GND			P9	AB2						
		GND			R10	E1						
		GND			R12	E2						
		GND			R14	G1						
		GND			R16	G2						
		GND			R18	J1						
		GND			T11	J2						
		GND			T13	L1						
		GND			T17	L2						
		GND			T7	N1						
		GND			U21	N2						
		GND			U8	R1						
		GND			V25	R2						
		GND			Y16	U1						
		GND			Y18	U2						
		GND			Y8	W1						
		GND			W14	W2						
		GND			Y13							
		GND			V13							
		GND			W12							
		GND			U12							
		GND			Y11							
		GND			Y9							
		GND			W10							
		GND			V11							
		GND			AC8							
		GND			AA15							
		GND			V15							
		GND			W16							
		GND			U16							
		GND			V17							
		GND			W18							
		GND			Y17							
		GND			AA17							
		GND			U18							
		GND			AA20							
		GND			V19							
		GND			J20							

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		GND			K19							
		GND			G14							
		GND			H15							
		GND			E18							
		GND			J16							
		GND			H17							
		GND			J18							
		GND			J14							
		GND			K13							
		GND			E13							
		GND			E14							
		GND			H13							
		GND			J12							
		GND			H11							
		GND			H10							
		GND			H9							
		GND			D8							
		GND			E8							
		GND			AB1							
		GND			AB2							
		GND			AC2							
		GND			AD1							
		GND			E3							
		GND			E4							
		GND			F1							
		GND			F2							
		GND			G3							
		GND			G4							
		GND			H1							
		GND			H2							
		GND			J3							
		GND			J4							
		GND			K1							
		GND			K2							
		GND			L3							
		GND			L4							
		GND			M1							
		GND			M2							
		GND			N3							
		GND			N4							
		GND			P1							
		GND			P2							
		GND			R3							
		GND			R4							
		GND			T1							
		GND			T2							
		GND			U3							
		GND			U4							
		GND			V1							
		GND			V2							
		GND			W3							
		GND			W4							
		GND			Y1							
		GND			Y2							
		GND			M7							
		GND			R8							
		VCC_CLKIN3A			U14	N12						
		VCC_CLKIN3B			V9	P7						
		VCC_CLKIN8A			K14	H10						
		VCC_CLKIN8B			J9							
		VCCD_PLL			J6	G3						
		VCCD_PLL			L6	M4						
		VCCD_PLL			M6	R4						
		VCCD_PLL			R6	U4						
		VCCD_PLL			T6	V18						
		VCCD_PLL			V6	E18						
		VCCD_PLL			Y20							
		VCCD_PLL			G21							
		VCCINT			J10	J5						
		VCCINT			K16	F7						
		VCCINT			K18	G13						
		VCCINT			K8	G9						
		VCCINT			L11	H6						
		VCCINT			L13	J11						
		VCCINT			L17	J17						
		VCCINT			M10	J7						

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		VCCINT			M12	J9						
		VCCINT			M14	K16						
		VCCINT			M16	K6						
		VCCINT			M18	K8						
		VCCINT			M8	L11						
		VCCINT			N11	L17						
		VCCINT			N13	L5						
		VCCINT			N15	L7						
		VCCINT			N17	L9						
		VCCINT			N9	M10						
		VCCINT			P10	M12						
		VCCINT			P12	M6						
		VCCINT			P14	N16						
		VCCINT			P16	N5						
		VCCINT			P18	N9						
		VCCINT			P8	P12						
		VCCINT			R11	P17						
		VCCINT			R13	P6						
		VCCINT			R15	P8						
		VCCINT			R17	R7						
		VCCINT			R7	T10						
		VCCINT			R9	T12						
		VCCINT			T12	U16						
		VCCINT			T16							
		VCCINT			T18							
		VCCINT			U11							
		VCCINT			U13							
		VCCINT			U15							
		VCCINT			U17							
		VCCINT			V10							
		VCCINT			V8							
		VCCINT			W13							
		VCCINT			V14							
		VCCINT			Y12							
		VCCINT			V12							
		VCCINT			W11							
		VCCINT			Y10							
		VCCINT			W9							
		VCCINT			Y14							
		VCCINT			W15							
		VCCINT			V16							
		VCCINT			W17							
		VCCINT			V18							
		VCCINT			W19							
		VCCINT			H14							
		VCCINT			J15							
		VCCINT			G15							
		VCCINT			H16							
		VCCINT			G17							
		VCCINT			J19							
		VCCINT			J17							
		VCCINT			H18							
		VCCINT			J13							
		VCCINT			H12							
		VCCINT			J11							
		VCCINT			K12							
		VCCINT			G11							
		VCCINT			G10							
		VCCINT			G9							
		VCCINT			F8							
		VCCINT			L7							
		VCCINT			T8							
		VCCIO3			AA10	U11						
		VCCIO3			AA11	U8						
		VCCIO3			AA12	U9						
		VCCIO3			AA13	V10						
		VCCIO3			AA14	V12						
		VCCIO3			W8							
		VCCIO4			AA16	U13						
		VCCIO4			AA18	V15						
		VCCIO4			AA19	V16						
		VCCIO4			AB17	V17						
		VCCIO4			Y15							
		VCCIO4			Y19							
		VCCIO5			P21	N18						
		VCCIO5			R21	P19						

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F672	F484	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		VCCIO5			T20	R18						
		VCCIO5			U20							
		VCCIO5			V20							
		VCCIO6			H21	H19						
		VCCIO6			J21	J18						
		VCCIO6			L20	K18						
		VCCIO6			M20							
		VCCIO6			N21							
		VCCIO7			F16	E13						
		VCCIO7			F18	E14						
		VCCIO7			F20	E15						
		VCCIO7			G16	E16						
		VCCIO7			G18	F14						
		VCCIO7			G19							
		VCCIO8			E10	E10						
		VCCIO8			F11	E11						
		VCCIO8			F13	E12						
		VCCIO8			F14	E9						
		VCCIO8			F9	F10						
		VCCIO8			G12							
		VCCIO9			G7	G4						
		VCCA			H6	F4						
		VCCA			K7	L4						
		VCCA			N7	T5						
		VCCA			P7	V4						
		VCCA			U7	U19						
		VCCA			W6	F19						
		VCCA			W21							
		VCCA			H20							
		NC			AB3	Y3						
		NC			AB4	AA3						
		NC			AA9							
		NC			AA7							
		NC			AB15							
		NC			AB20							
		NC			AC15							
		NC			AD15							
		NC			F15							
		NC			E19							
		NC			D13							
		NC			E12							
		NC			D12							
		NC			E11							
		NC			AB8							
		NC			AA8							
		VCCL_GXB			AD2	V3						
		VCCL_GXB			G5	K3						
		VCCL_GXB			H5	L3						
		VCCL_GXB			L5	N3						
		VCCL_GXB			P5	T3						
		VCCL_GXB			AA3							
		VCCL_GXB			AA4							
		VCCL_GXB			U5							
		VCCL_GXB			Y5							
		VCCH_GXB			J5	H3						
		VCCH_GXB			M5	P3						
		VCCH_GXB			R5							
		VCCH_GXB			V5							
		RREF0			AC1	AB1						
		VCCA_GXB			AC3	W3						
		VCCA_GXB			K5	J3						
		VCCA_GXB			N5	R3						
		VCCA_GXB			T5							
		VCCA_GXB			W5							

Notes:
(1) For DQS pins that do not have the associated DQ pins, the particular DQS is not supported.
(2) For implementation of transceiver applications that run at ≥2.97Gbps data rate, you must refer to the Cyclone IV Device Family Pin Connection Guidelines.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
CLK[5, 7, 9, 11, 12,14], DIFFCLK_[2..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLK[4, 6, 8, 10, 13, 15], DIFFCLK_[2..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
DIFFCLK_[0, 1, 8, 9]p, CLKIO[17, 19, 20, 22]	Clock, Input	Optional positive terminal inputs for differential global clock input or single-ended clock input.
DIFFCLK_[0, 1, 8, 9]n	Clock, Input	Optional negative terminal inputs for differential global clock input.
PLL[1..8]_CLKOUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
PLL[1..8]_CLKOUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
	Configuration/JTAG Pins	
MSEL[0..3]	Input	Configuration input pins that set the Cyclone IV GX device configuration scheme. The smaller devices like EP4CGX15, EP4CGX22, and EP4CGX30 do not have the MSEL3 pin.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
NCEO	I/O, Output	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as an user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
NCSO	I/O, Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO, DATA1	Input (PS, FPP) Output (AS)	This pin functions as DATA1 in PS and FPP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide configuration data is presented to the target device on DATA[0..7]. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual- Purpose Pin settings. ASDO: Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.

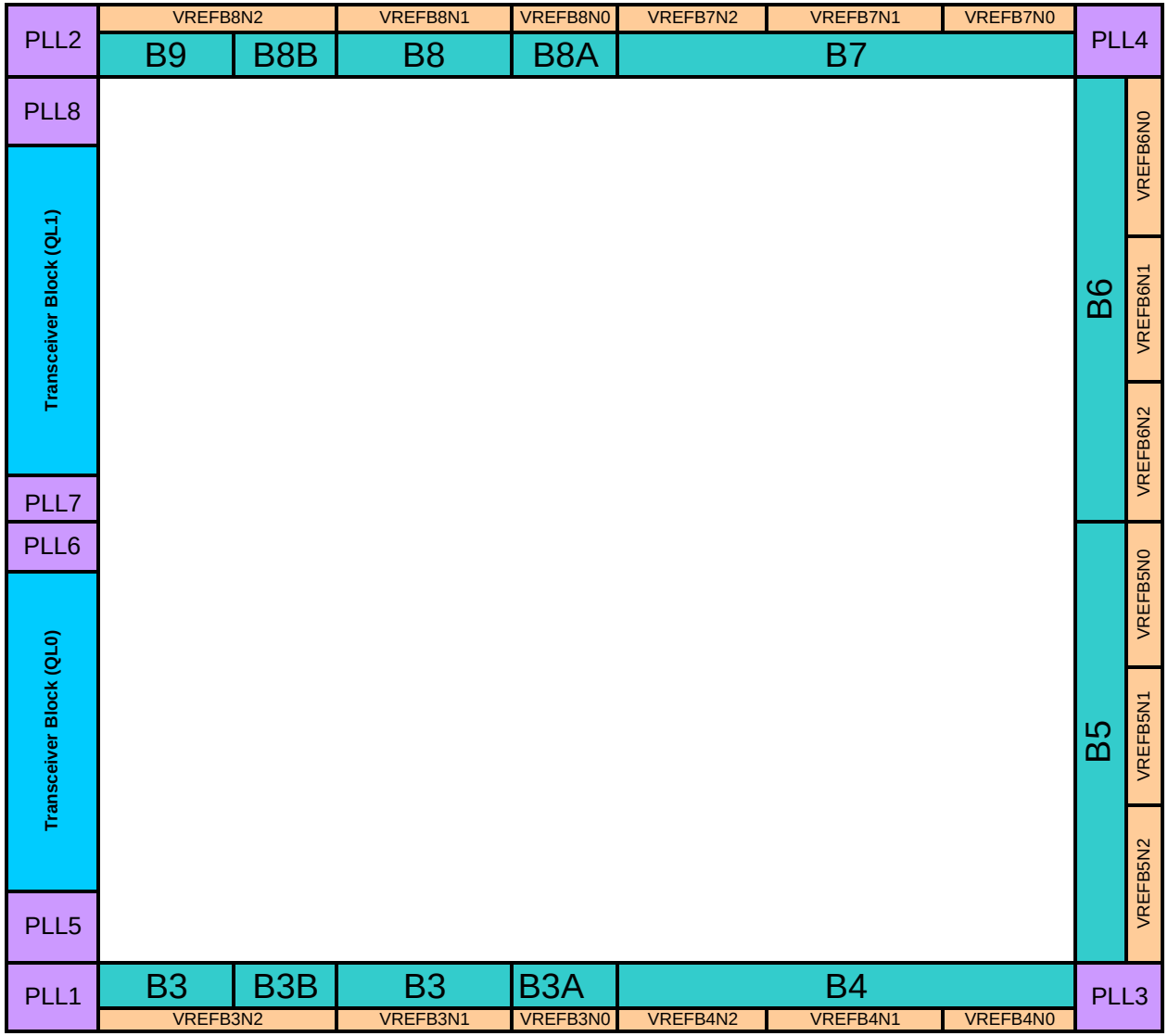
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DATA[2..7]	Input (FPP)	Data inputs. Byte-wide configuration data is presented to the target device on DATA [0..7]. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [2..7] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
Differential I/O Pins		
DIFFIO_[R,T,B]0..72][n,p]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[0..5][R,T,B]/CQ[0,1,3,5][R,T,B][#],DPCLK[0..17]	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ[0..5][R,T,B]	I/O, DQ	Optional data signal for use in external memory interface.
DM[0..5][R,B,T]/BWS#[0..5][R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDR II SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.
Reference Pins		
RUP[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. If the RUP pin is not used, this pin can function as a regular I/O pin.
RDN[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If the RDN pin is not used, this pin can function as a regular I/O pin.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCCINT	Power	These are internal logic array voltage supply pins.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
VCCD_PLL	Power	Digital power for PLLs. The designer must power up these pins, even if the PLL is not used.
VCCA	Power	Analog power for PLLs. All VCCA pins must be powered and all VCCA pins must be powered up and powered down at the same time even if not all the PLLs are used. Designer is advised to keep VCCA isolated from other VCC for better jitter performance.
VCCIO[3..9]	Power	These are I/O supply voltage pins for banks 3 through 9. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards.
VCC_CLKIN[3,8]A	Power	CLLKIN power in bank 3A and bank 8A.
VREFB[3..8]N[0..2]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
GND	Ground	Device ground pins. All GND pins should be connected to GND plane on the board.
Transceiver Pins		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX, and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA_GXB	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0..7]p	Input	High speed positive differential receiver channels.
GXB_RX[0..7]n	Input	High speed negative differential receiver channels.
GXB_TX[0..7]p	Output	High speed positive differential transmitter channels.
GXB_TX[0..7]n	Output	High speed negative differential transmitter channels.
REFCLK[0..5]p *(2)*	Input	High speed differential reference clock positive.
REFCLK[0..5]n *(2)*	Input	High speed differential reference clock complement.
RREF0	Input	Reference resistor for transceiver.

Notes:

(1) The pin definitions are prepared based on the device with the largest density, EP4CGX150. For the availability of pins in each density, refer to the pin list.

(2) For implementation of transceiver applications that run at ≥2.97Gbps data rate, you must refer to the Cyclone IV Device Family Pin Connection Guidelines.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to provide an idea of placement on the device. For exact locations, refer to the pin list and the Quartus® II software.

Version Number	Date	Changes Made
1.0	6/23/2010	Initial release.
1.1	11/8/2010	Added new note in Pin List and Pin Definitions.