Pin Information for the Cyclone® IV GX EP4CGX15 Device
Version 1.2
Note (1)

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F169	DQS for X8 in F169
QL0		GXB_TX1p			C2	
QL0		GXB_TX1n			C1	
QL0		GXB_RX1p			E2	
QL0		GXB_RX1n			E1	
QL0		GXB_TX0p			G2	
QL0		GXB_TX0n			G1	
QL0		GXB_RX0p			J2	
QL0		GXB_RX0n			J1	
B3		MSEL2		MSEL2	L3	
B3		MSEL1		MSEL1	N3	
B3		MSEL0		MSEL0	K5	
B3		CONF_DONE		CONF_DONE	J5	
B3		nSTATUS		nSTATUS	K6	
B3	VREFB3N0	IO	PLL1_CLKOUTp		L4	
B3	VREFB3N0	IO	PLL1_CLKOUTn		M4	
B3	VREFB3N0	IO	DIFFIO_B1p	CRC_ERROR	N4	
B3	VREFB3N0	IO	DIFFIO_B1n	NCEO	N5	
B3	VREFB3N0	IO	DIFFIO_B2p	INIT_DONE	M6	
B3	VREFB3N0	IO	DIFFIO_B2n		N6	DQ0B
B3	VREFB3N0	IO			L5	DQS1B/CQ0B#, DPCLK2
B3	VREFB3N0	IO	VREFB3N0		L7	
B3A	VREFB3N0	CLK12	DIFFCLK_7p,REFCLK0p		J6	
B3A	VREFB3N0	CLK13	DIFFCLK_7n,REFCLK0n		J7	
B4	VREFB4N0	CLK14	DIFFCLK_6p		M7	
B4	VREFB4N0	CLK15	DIFFCLK_6n		N7	
B4	VREFB4N0	IO	DIFFIO_B3p		N8	DQ0B
B4	VREFB4N0	IO	DIFFIO_B3n		N9	DQ0B
B4	VREFB4N0	IO	VREFB4N0		K8	
B4	VREFB4N0	IO			K9	DQ0B
B4	VREFB4N0	IO	DIFFIO_B4p		L9	DQ0B
B4	VREFB4N0	IO	DIFFIO_B4n		M9	DQS0B/CQ0B, DPCLK5
B4	VREFB4N0	IO	DIFFIO_B5p		N10	DQ0B
B4	VREFB4N0	IO	DIFFIO_B5n		N11	DQ0B

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F169	DQS for X8 in F169
B4	VREFB4N0	IO	RUP2		M11	DQ0B
B4	VREFB4N0	IO	RDN2		N12	DM0B
B4	VREFB4N0	IO	PLL3_CLKOUTp		K10	
B4	VREFB4N0	IO	PLL3_CLKOUTn		L11	
B5	VREFB5N0	IO	RUP3		N13	
B5	VREFB5N0	IO	RDN3		M13	
B5	VREFB5N0	IO	DIFFIO_R7n		K12	DQ0R
B5	VREFB5N0	IO	DIFFIO_R7p		K11	DQ0R
B5	VREFB5N0	IO	DIFFIO_R6n		L13	DQ0R
B5	VREFB5N0	IO	DIFFIO_R6p		L12	DQ0R
B5	VREFB5N0	IO	VREFB5N0		H12	
B5	VREFB5N0	IO			H10	DQS1R/CQ0R#, DPCLK7
B5	VREFB5N0	IO	DIFFIO_R5n		J13	DQ0R
B5	VREFB5N0	IO	DIFFIO_R5p		K13	DQ0R
B5	VREFB5N0	CLK4	DIFFCLK_2n		G13	
B5	VREFB5N0	CLK5	DIFFCLK_2p		H13	
B6	VREFB6N0	CLK6	DIFFCLK_3n		F13	
B6	VREFB6N0	CLK7	DIFFCLK_3p		F12	
B6	VREFB6N0	IO	DIFFIO_R4n	DEV_OE	G10	
B6	VREFB6N0	IO	DIFFIO_R4p		G9	DQS0R/CQ0R, DPCLK8
B6	VREFB6N0	IO	DIFFIO_R3n		F11	DQ0R
B6	VREFB6N0	IO	DIFFIO_R3p		F10	DQ0R
B6	VREFB6N0	IO	VREFB6N0		E13	
B6	VREFB6N0	IO			F9	
B6	VREFB6N0	IO	DIFFIO_R2n	DEV_CLRn	D10	
B6	VREFB6N0	IO	DIFFIO_R2p		E10	DM0R
B6	VREFB6N0	IO	DIFFIO_R1n		D12	
B6	VREFB6N0	IO	DIFFIO_R1p		D11	
B7	VREFB7N0	IO	RUP4		C11	DQ0T
B7	VREFB7N0	IO	RDN4		C12	DQ0T
B7	VREFB7N0	IO	DIFFIO_T4n		C13	DQ0T
B7	VREFB7N0	IO	DIFFIO_T4p		D13	DQ0T
B7	VREFB7N0	IO	DIFFIO_T3n		A13	DQS0T/CQ0T, DPCLK10

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F169	DQS for X8 in F169
B7	VREFB7N0	IO	DIFFIO_T3p		B13	DQ0T
B7	VREFB7N0	IO			B11	
B7	VREFB7N0	IO	VREFB7N0		B10	
B7	VREFB7N0	IO	DIFFIO_T2n		B8	DQ0T
B7	VREFB7N0	IO	DIFFIO_T2p		C8	DQ0T
B7	VREFB7N0	IO	DIFFIO_T1n		A11	DQ0T
B7	VREFB7N0	IO	DIFFIO_T1p		A12	DM0T
B7	VREFB7N0	CLK8	DIFFCLK_5n		A9	
B7	VREFB7N0	CLK9	DIFFCLK_5p		A10	
B8A	VREFB8N0	CLK10	DIFFCLK_4n,REFCLK1n		E6	
B8A	VREFB8N0	CLK11	DIFFCLK_4p,REFCLK1p		E7	
B8	VREFB8N0	IO	VREFB8N0		C6	
B8	VREFB8N0	IO			B6	DQS1T/CQ0T#, DPCLK13
B8	VREFB8N0	IO	PLL2_CLKOUTn		A7	
B8	VREFB8N0	IO	PLL2_CLKOUTp		A8	
B8	VREFB8N0	IO		CLKUSR	A6	
B9	VREFB8N0	IO		DATA0	A5	
B9	VREFB8N0	IO		ASDO	B5	
B9	VREFB8N0	IO		NCSO	C5	
B9		DCLK		DCLK	A4	
B9		nCONFIG		nCONFIG	D5	
B9		nCE		nCE	C4	
B9		TDI		TDI	A3	
B9		TCK		TCK	B3	
B9		TMS		TMS	A2	
B9		TDO		TDO	A1	
		GND			E3	
		GND			K3	
		GND			J9	
		GND			D6	
		GND			M12	
		GND			M10	
		GND			M8	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F169	DQS for X8 in F169
		GND			M5	
		GND			J12	
		GND			H8	
		GND			H6	
		GND			H4	
		GND			G12	
		GND			G7	
		GND			G5	
		GND			F8	
		GND			F6	
		GND			F4	
		GND			E12	
		GND			E9	
		GND			E5	
		GND			D8	
		GND			B12	
		GND			B9	
		GND			B7	
		GND			B4	
		GND			M1	
		GND			L2	
		GND			K2	
		GND			K1	
		GND			H2	
		GND			H1	
		GND			F2	
		GND			F1	
		GND			D2	
		GND			D1	
		GND			B2	
		GND			B1	
		VCCINT			E8	
		VCCINT			J8	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F169	DQS for X8 in F169
		VCCINT			H7	
		VCCINT			H5	
		VCCINT			G8	
		VCCINT			G6	
		VCCINT			G4	
		VCCINT			F7	
		VCCINT			F5	
		VCCINT			E4	
		VCCIO3			L6	
		VCCIO4			L8	
		VCCIO4			L10	
		VCCIO5			H11	
		VCCIO5			J11	
		VCCIO6			E11	
		VCCIO6			G11	
		VCCIO7			C10	
		VCCIO7			C9	
		VCCIO8			C7	
		VCCIO9			C3	
		NC			N2	
		NC			M3	
		VCCA			D4	
		VCCA			K4	
		VCCA			H9	
		VCCA			D9	
		VCCL_GXB			N1	
		VCCL_GXB			F3	
		VCCL_GXB			H3	
		VCCL_GXB				
		VCCL_GXB				
		VCCH_GXB			G3	
		VCCH_GXB				
		RREF0			L1	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F169	DQS for X8 in F169
		VCC_CLKIN3A			K7	
		VCCD_PLL			D3	
		VCCD_PLL			J4	
		VCCD_PLL			J10	
		VCC_CLKIN8A			D7	
		VCCA_GXB			M2	
		VCCA_GXB			J3	
		VCCA_GXB				

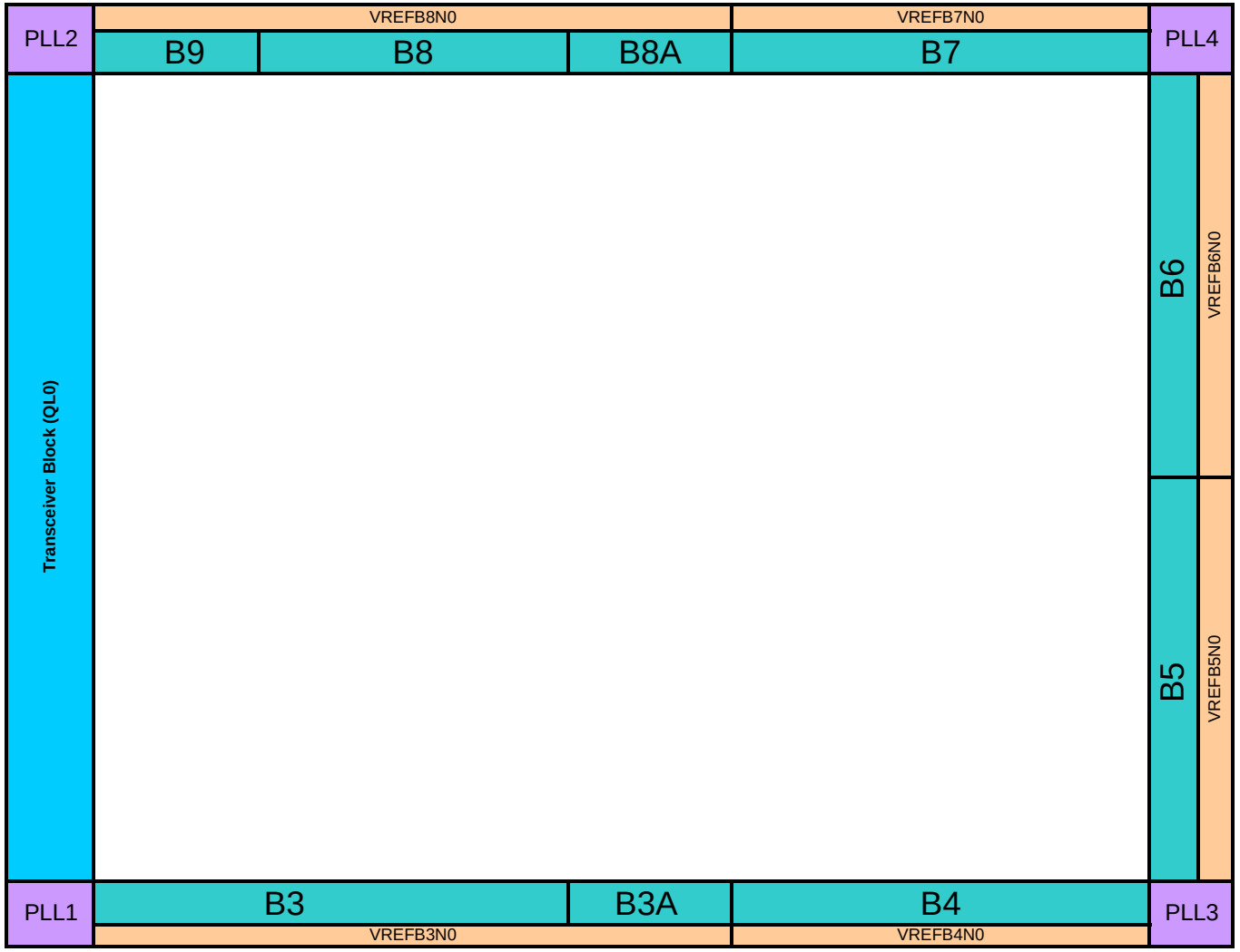
Note:
(1) For DQS pins that do not have the associated DQ pins, the particular DQS is not supported.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Clock and PLL Pins		
CLK[5, 7, 9, 11, 12,14], DIFFCLK_[2..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLK[4, 6, 8, 10, 13, 15], DIFFCLK_[2..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
PLL[1..8]_CLKOUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
PLL[1..8]_CLKOUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
Configuration/JTAG Pins		
MSEL[0..3]	Input	Configuration input pins that set the Cyclone IV GX device configuration scheme. The smaller devices like EP4CGX15, EP4CGX22, and EP4CGX30 do not have the MSEL3 pin.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
NCEO	I/O, Output	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as an user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
NCSO	I/O, Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO, DATA1	Input (PS, FPP) Output (AS)	This pin functions as DATA1 in PS and FPP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide configuration data is presented to the target device on DATA[0..7]. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. ASDO: Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DATA[2..7]	Input (FPP)	Data inputs. Byte-wide configuration data is presented to the target device on DATA [0..7]. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [2..7] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
Differential I/O Pins		
DIFFIO_[R,T,B]0..72][n,p]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[0..5][R,T,B]/CQ[0,1,3,5][R,T,B][#],DPCLK[0..17]	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ[0..5][R,T,B]	I/O, DQ	Optional data signal for use in external memory interface.
DM[0..5][R,B,T]/BWS#[0..5][R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDR II SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.
Reference Pins		
RUP[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5 and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. If the RUP pin is not used, this pin can function as a regular I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
RDN[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5 and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If the RDN pin is not used, this pin can function as a regular I/O pin.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCCINT	Power	These are internal logic array voltage supply pins.
VCCD_PLL	Power	Digital power for PLLs. The designer must power up these pins, even if the PLL is not used.
VCCA	Power	Analog power for PLLs. All VCCA pins must be powered and all VCCA pins must be powered up and powered down at the same time even if not all the PLLs are used. Designer is advised to keep VCCA isolated from other VCC for better jitter performance.
VCCIO[3..9]	Power	These are I/O supply voltage pins for banks 3 through 9. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards.
VCC_CLKIN[3,8]A	Power	CLLKIN power in bank 3A and bank 8A.
VREFB[3..8]N0	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
GND	Ground	Device ground pins. All GND pins should be connected to GND plane on the board.
Transceiver Pins		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX, and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA_GXB	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0..7]p	Input	High speed positive differential receiver channels.
GXB_RX[0..7]n	Input	High speed negative differential receiver channels.
GXB_TX[0..7]p	Output	High speed positive differential transmitter channels.
GXB_TX[0..7]n	Output	High speed negative differential transmitter channels.
REFCLK[0..5]p	Input	High speed differential reference clock positive.
REFCLK[0..5]n	Input	High speed differential reference clock complement.
RREF0	Input	Reference resistor for transceiver.

Note:
(1) The pin definitions are prepared based on the device with the largest density, EP4CGX150. Refer to the pin list for the availability of pins in each density.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	12/18/2009	Initial release.
1.1	4/7/2015	Added Note *(2)* to Pin List N148.
1.2	3/21/2016	Removed Pin List N148.