Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
QL1		GXB_TX7p			H4	F4										
QL1		GXB_TX7n			H3	F3										
QL1		GXB_RX7p			J2	G2										
QL1		GXB_RX7n			J1	G1										
QL1		GXB_TX6p			K4	H4										
QL1		GXB_TX6n			K3	H3										
QL1		GXB_RX6p			L2	J2										
QL1		GXB_RX6n			L1	J1										
QL1		GXB_TX5p			M4	K4										
QL1		GXB_TX5n			M3	K3										
QL1		GXB_RX5p			N2	L2										
QL1		GXB_RX5n			N1	L1										
QL1		GXB_TX4p			P4	M4										
QL1		GXB_TX4n			P3	M3										
QL1		GXB_RX4p			R2	N2										
QL1		GXB_RX4n			R1	N1										
QL0		GXB_TX3p			T4	P4	F2									
QL0		GXB_TX3n			T3	P3	F1									
QL0		GXB_RX3p			U2	R2	H2									
QL0		GXB_RX3n			U1	R1	H1									
QL0		GXB_TX2p			V4	T4	K2									
QL0		GXB_TX2n			V3	T3	K1									
QL0		GXB_RX2p			W2	U2	M2									
QL0		GXB_RX2n			W1	U1	M1									
QL0		GXB_TX1p			Y4	V4	P2									
QL0		GXB_TX1n			Y3	V3	P1									
QL0		GXB_RX1p			AA2	W2	T2									
QL0		GXB_RX1n			AA1	W1	T1									
QL0		GXB_TX0p			AB4	Y4	V2									
QL0		GXB_TX0n			AB3	Y3	V1									
QL0		GXB_RX0p			AC2	AA2	Y2									
QL0		GXB_RX0n			AC1	AA1	Y1									
B3		MSEL3		MSEL3	AC8	W7	P4									
B3		MSEL2		MSEL2	AC7	Y6	R5									
B3		MSEL1		MSEL1	AD8	Y7	P5									
B3		MSEL0		MSEL0	AD7	AA6	T6									
B3		CONF_DONE		CONF_DONE	AB9	AB6	U5									
B3		nSTATUS		nSTATUS	AJ1	AA5	R8									
B3	VREFB3N2	IO		INIT_DONE	AE8	AB7	W8									
B3	VREFB3N2	IO	DIFFIO_B1p	CRC_ERROR	AD6	AC6	AA4									
B3	VREFB3N2	IO	DIFFIO_B1n	NCEO	AE7	AC7	AB3									
B3B	VREFB3N2	REFCLK0p	DIFFCLK_0p,CLKIO20		V11	T9	M7									
B3B	VREFB3N2	REFCLK0n	DIFFCLK_0n		W11	U9	N7									
B3B	VREFB3N2	REFCLK1p	DIFFCLK_1p,CLKIO22		V12	T10	M8									
B3B	VREFB3N2	REFCLK1n	DIFFCLK_1n		W12	U10	N8									
B3	VREFB3N2	IO	PLL1_CLKOUTp		AE6	AB5	T7									
B3	VREFB3N2	IO	PLL1_CLKOUTn		AF6	AC5	T8									
B3	VREFB3N2	IO	PLL5_CLKOUTp		AF7	AC4	U6									
B3	VREFB3N2	IO	PLL5_CLKOUTn		AG6	AD4	V6									
B3	VREFB3N2	IO	PLL6_CLKOUTp		AE9	AD3	U7									
B3	VREFB3N2	IO	PLL6_CLKOUTn		AF9	AE3	V7									
B3	VREFB3N2	IO	DIFFIO_B2p	DATA5	AE4	AE1	W4									
B3	VREFB3N2	IO	DIFFIO_B2n	DATA6	AE5	AE2	Y4									
B3	VREFB3N2	IO	DIFFIO_B3p	DATA7	AE10	AF2	R9									
B3	VREFB3N2	IO	DIFFIO_B3n		AF10	AF3	T9									
B3	VREFB3N2	IO	DIFFIO_B4p		AF4	AA7										
B3	VREFB3N2	IO	DIFFIO_B4n		AG4	AA8										
B3	VREFB3N2	IO	DIFFIO_B5p		AE3	AB8	W5	DM1B	DM1B/BWS#1B					DM3B/BWS#3B	DM3B/BWS#3B	DM5B/BWS#5B
B3	VREFB3N2	IO	DIFFIO_B5n		AF3	AC8	Y5	DQ1B	DQ1B					DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B6p		AG3				DQ1B							
B3	VREFB3N2	IO	DIFFIO_B6n		AH3											
B3	VREFB3N2	IO	VREFB3N2		AE11	AB9	V9									
B3	VREFB3N2	IO	DIFFIO_B7p		AD9	AC9	R11	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0	DQS1B/CQ1B#,DPCLK0
B3	VREFB3N2	IO	DIFFIO_B7n		AD10	AD9	T11		DQ1B		DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B8p		AH2	W9	W6	DQ1B	DQ1B					DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B8n		AJ3	Y9	Y6	DQ1B	DQ1B					DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B9p		AH4	AD7	W7				DM3B/BWS#3B	DM3B/BWS#3B	DM5B/BWS#5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B9n		AJ4	AD8	Y7	DQ1B	DQ1B		DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B10p		AG5	AD5		DQ1B	DQ1B		DQ3B	DQ3B	DQ5B			
B3	VREFB3N2	IO	DIFFIO_B10n		AH5	AD6					DQ3B	DQ3B	DQ5B			
B3	VREFB3N2	IO	DIFFIO_B11p		AK3	AE5					DQ3B	DQ3B	DQ5B			
B3	VREFB3N2	IO	DIFFIO_B11n		AK4	AE6		DQ1B	DQ1B		DQ3B	DQ3B	DQ5B			
B3	VREFB3N2	IO	DIFFIO_B12p		AH6	AF4		DQ1B	DQ1B		DQ3B	DQ3B	DQ5B			
B3	VREFB3N2	IO	DIFFIO_B12n		AJ6	AF5		DM3B/BWS#3B	DM1B/BWS#1B	DM2B/BWS#2B	DQ3B	DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B13p		AK5		AB4	DQ1B	DQ1B					DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B13n		AK6		AB5							DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B14p		AE12	V11		DQ3B	DQ1B							
B3	VREFB3N1	IO	DIFFIO_B14n		AF12	W10										
B3	VREFB3N1	IO	DIFFIO_B15p		AG9	Y10		DQ3B	DQ1B							
B3	VREFB3N1	IO	DIFFIO_B15n		AH9	AA9										
B3	VREFB3N1	IO	DIFFIO_B16p		AE13	W11		DQ3B	DQ1B	DQ2B						
B3	VREFB3N1	IO	DIFFIO_B16n		AF13	Y11										
B3	VREFB3N1	IO	DIFFIO_B17p		AG10	U12	AA6	DQ3B	DQ1B	DQ2B				DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B17n		AH10	V12	AB6							DM5B/BWS#5B	DM3B/BWS#3B	DM5B/BWS#5B
B3	VREFB3N1	IO	DIFFIO_B18p		AH11			DQ3B	DQ1B	DQ2B						
B3	VREFB3N1	IO	DIFFIO_B18n		AJ10			DQ3B	DQ1B	DQ2B						
B3	VREFB3N1	IO	VREFB3N1		AG11	AD11	W10									
B3	VREFB3N1	IO	DIFFIO_B19p		AG12	AB11	AA7				DQ3B	DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B19n		AH12	AC11	AB7	DQ3B	DQ1B		DM5B/BWS#5B	DM3B/BWS#3B	DM5B/BWS#5B			
B3	VREFB3N1	IO	DIFFIO_B20p		AA12	W12										
B3	VREFB3N1	IO	DIFFIO_B20n		AB11	Y12										
B3	VREFB3N1	IO	DIFFIO_B21p		AG13	AC10	W9	DQ3B	DQ1B		DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B21n		AH13	AD10	Y8	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1	DQS3B/CQ3B#,DPCLK1
B3	VREFB3N1	IO	DIFFIO_B22p		AG8		Y9							DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B22n		AH8		AA9	DQ3B	DQ4B					DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B23p		AA13	AB12	AB8				DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B23n		AB13	AC12	AB9	DM5B/BWS#5B	DM4B/BWS#4B	DM2B/BWS#2B	DQ5B	DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B24p		AG7				DQ4B							
B3	VREFB3N1	IO	DIFFIO_B24n		AH7											
B3	VREFB3N1	IO	DIFFIO_B25p		AA16	AE7			DQ4B							
B3	VREFB3N1	IO	DIFFIO_B25n		AB16	AF6		DQ5B	DQ4B							

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B3	VREFB3N1	IO	DIFFIO_B26p		AG14	V13										
B3	VREFB3N1	IO	DIFFIO_B26n		AH14	V14										
B3	VREFB3N1	IO	DIFFIO_B27p		AJ7	AF7		DQ5B	DQ4B	DQ2B						
B3	VREFB3N1	IO	DIFFIO_B27n		AK7	AF8					DQ5B	DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B28p		AJ9	AD12					DQ5B	DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B28n		AK8	AE11		DQ5B	DQ4B	DQ2B	DQ5B	DQ3B	DQ5B			
B3	VREFB3N0	IO	DIFFIO_B29p		AK9											
B3	VREFB3N0	IO	DIFFIO_B29n		AK10											
B3	VREFB3N0	IO	DIFFIO_B30p		AA15	W13	W11	DQ5B	DQ4B	DQ2B				DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B30n		AB14	Y13	Y11							DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B31p		AE14			DQ5B	DQ4B	DQ2B						
B3	VREFB3N0	IO	DIFFIO_B31n		AE15											
B3	VREFB3N0	IO	DIFFIO_B32p		AF15	AC13	Y10	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2	DQS5B/CQ5B#,DPCLK2
B3	VREFB3N0	IO	DIFFIO_B32n		AG15	AD13	AA10				DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	VREFB3N0		AC16	AE13	U12									
B3	VREFB3N0	IO	DIFFIO_B33p		AK11	W14		DQ5B	DQ4B	DQ2B						
B3	VREFB3N0	IO	DIFFIO_B33n		AK12	Y14										
B3	VREFB3N0	IO	DIFFIO_B34p		AJ12	AE9										
B3	VREFB3N0	IO	DIFFIO_B34n		AK13	AF9										
B3	VREFB3N0	IO	DIFFIO_B35p		AH15	AE10	W12	DQ5B	DQ4B	DQ2B	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B35n		AH16	AF10	Y12	DQ5B	DQ4B	DQ2B	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B36p		AJ13	AF11	AB10				DM4B	DM5B/BWS#5B	DM5B/BWS#5B	DM4B	DM5B/BWS#5B	DM5B/BWS#5B
B3	VREFB3N0	IO	DIFFIO_B36n		AK14	AF12	AB11	DQ5B	DQ4B	DQ2B		DQ5B	DQ5B		DQ5B	DQ5B
B3A	VREFB3N0	CLKIO12	DIFFCLK_7p,REFCLK2p		V15	T14	M11									
B3A	VREFB3N0	CLKIO13	DIFFCLK_7n,REFCLK2n		W15	T15	N11									
B4	VREFB4N2	CLKIO14	DIFFCLK_6p		AJ16	AF13	AA12									
B4	VREFB4N2	CLKIO15	DIFFCLK_6n		AK16	AF14	AB12									
B4	VREFB4N2	IO	DIFFIO_B37p		Y17	AC14	R13	DM4B	DM4B/BWS#4B		DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B37n		AA17	AD14	T13	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3	DQS4B/CQ5B,DPCLK3
B4	VREFB4N2	IO	DIFFIO_B38p		AF16											
B4	VREFB4N2	IO	DIFFIO_B38n		AG16											
B4	VREFB4N2	IO	DIFFIO_B39p		AJ15	AE14	W13	DQ4B	DQ4B	DQ2B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B39n		AK15	AE15	Y13	DQ4B	DQ4B	DQ2B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B40p		AD16											
B4	VREFB4N2	IO	DIFFIO_B40n		AE16											
B4	VREFB4N2	IO	VREFB4N2		AB17	AB14	V13									
B4	VREFB4N2	IO	DIFFIO_B41p		AE17	AC15	AA13									
B4	VREFB4N2	IO	DIFFIO_B41n		AF18	AD15	AB13									
B4	VREFB4N2	IO	DIFFIO_B42p		AK17	AF15		DQ4B	DQ4B	DQ2B	DQ4B	DQ5B	DQ5B			
B4	VREFB4N2	IO	DIFFIO_B42n		AK18	AF16		DQ4B	DQ4B	DQ2B	DQ4B	DQ5B	DQ5B			
B4	VREFB4N2	IO	DIFFIO_B43p		AH18	AC16		DQ4B	DQ4B	DQ2B	DQ4B	DQ5B	DQ5B			
B4	VREFB4N2	IO	DIFFIO_B43n		AJ18	AD16		DQ4B	DQ4B	DQ2B	DQ4B	DQ5B	DQ5B			
B4	VREFB4N2	IO	DIFFIO_B44p		AG17		AB14							DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B44n		AH17		AB15							DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B45p		AJ19	AA15	W14							DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B45n		AK19	AB15	Y14							DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B46p		AE18		R14	DQ4B	DQ2B	DQ2B						
B4	VREFB4N2	IO	DIFFIO_B46n		AE19		T14	DM2B	DM2B/BWS#2B	DM2B/BWS#2B						
B4	VREFB4N2	IO	DIFFIO_B47p		AG18	AC17					DQ4B	DQ5B	DQ5B			
B4	VREFB4N2	IO	DIFFIO_B47n		AH19	AD17		DQ4B	DQ2B	DQ2B	DM2B	DM5B/BWS#5B	DM5B/BWS#5B			
B4	VREFB4N2	IO	DIFFIO_B48p		AF19	AE17										
B4	VREFB4N2	IO	DIFFIO_B48n		AG19	AF17					DQ2B	DQ5B	DQ5B			
B4	VREFB4N1	IO	DIFFIO_B49p		Y18	V15										
B4	VREFB4N1	IO	DIFFIO_B49n		AA18	W15										
B4	VREFB4N1	IO	DIFFIO_B50p		AK20	V16										
B4	VREFB4N1	IO	DIFFIO_B50n		AK21	W16										
B4	VREFB4N1	IO	DIFFIO_B51p		AJ22	U16										
B4	VREFB4N1	IO	DIFFIO_B51n		AK22	V17										
B4	VREFB4N1	IO	DIFFIO_B52p		AG20	AE18	W15							DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B52n		AH20	AF18	Y15							DM2B	DM5B/BWS#5B	DM5B/BWS#5B
B4	VREFB4N1	IO	DIFFIO_B53p		AH21	Y17										
B4	VREFB4N1	IO	DIFFIO_B53n		AJ21	AA17										
B4	VREFB4N1	IO	VREFB4N1		AG21	AB18	W16									
B4	VREFB4N1	IO	DIFFIO_B54p		Y19	AC18	U14	DQ2B	DQ2B	DQ2B	DQ2B	DQ5B	DQ5B			
B4	VREFB4N1	IO	DIFFIO_B54n		AA20	AD18	U15	DQ2B	DQ2B	DQ2B	DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B55p		AE20	AE19	Y16							DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B55n		AE21	AF19	AA16	DQ2B	DQ2B	DQ2B	DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B56p		AG22											
B4	VREFB4N1	IO	DIFFIO_B56n		AH22											
B4	VREFB4N1	IO	DIFFIO_B57p		AF21	W17	AB17									
B4	VREFB4N1	IO	DIFFIO_B57n		AF22	W18	AB18							DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B58p		AD22	AC19	AA15	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4	DQS2B/CQ3B,DPCLK4
B4	VREFB4N1	IO	DIFFIO_B58n		AE22	AD19	AB16									
B4	VREFB4N1	IO	DIFFIO_B59p		AK23	AF20	W17	DQ2B	DQ2B	DQ2B	DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B59n		AK24	AF21	Y17				DQ2B	DQ5B	DQ5B			
B4	VREFB4N1	IO	DIFFIO_B60p		AJ24		Y18	DQ2B	DQ2B	DQ2B				DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B60n		AK25		AA18							DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B61p		AG23	AD20		DQ2B	DQ2B	DQ2B	DQ2B	DQ5B	DQ5B			
B4	VREFB4N1	IO	DIFFIO_B61n		AH23	AE21										
B4	VREFB4N1	IO	DIFFIO_B62p		AK26	AE22		DQ2B	DQ2B	DQ2B						
B4	VREFB4N1	IO	DIFFIO_B62n		AK27	AF22										
B4	VREFB4N0	IO	DIFFIO_B63p		AH25	U18		DQ2B	DQ2B	DQ2B						
B4	VREFB4N0	IO	DIFFIO_B63n		AJ25	V18										
B4	VREFB4N0	IO	DIFFIO_B64p		AJ27	AA20		DM0B	DM2B/BWS#2B	DM2B/BWS#2B						
B4	VREFB4N0	IO	DIFFIO_B64n		AK28	AB20										
B4	VREFB4N0	IO	DIFFIO_B65p		AG24	AE23										
B4	VREFB4N0	IO	DIFFIO_B65n		AH24	AF23										
B4	VREFB4N0	IO	VREFB4N0		AB21	AC20	T16									
B4	VREFB4N0	IO	DIFFIO_B66p		AJ28											
B4	VREFB4N0	IO	DIFFIO_B66n		AK29											
B4	VREFB4N0	IO	DIFFIO_B67p		Y20	AC21	AA19	DQ0B	DQ2B	DQ2B		DQ5B	DQ5B			
B4	VREFB4N0	IO	DIFFIO_B67n		Y21	AD21	AB19	DQ0B	DQ2B	DQ2B	DQ2B	DQ5B	DQ5B			
B4	VREFB4N0	IO	DIFFIO_B68p		AG26	AF24										
B4	VREFB4N0	IO	DIFFIO_B68n		AH26	AF25										
B4	VREFB4N0	IO	DIFFIO_B69p		AA21	AC22	AA20	DQ0B	DQ2B	DQ2B						
B4	VREFB4N0	IO	DIFFIO_B69n		AB22	AD22	AB20	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5	DQS0B/CQ1B,DPCLK5
B4	VREFB4N0	IO	DIFFIO_B70p		AG27	AD23	AA21									
B4	VREFB4N0	IO	DIFFIO_B70n		AH27	AD24	AB21	DQ0B	DQ2B	DQ2B					DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B71p		AD23											
B4	VREFB4N0	IO	DIFFIO_B71n		AE23											
B4	VREFB4N0	IO			AG25			DQ0B	DQ2B	DQ2B						

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B4	VREFB4N0	IO	DIFFIO_B72p		AG28	V19	W18	DQ0B	DQ2B	DQ2B						
B4	VREFB4N0	IO	DIFFIO_B72n		AH28	W19	Y19							DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	PLL3_CLKOUTp		AF24	AA21	AA22									
B4	VREFB4N0	IO	PLL3_CLKOUTn		AF25	AB21	AB22									
B4	VREFB4N0	IO	RUP2		AD24	Y21	W19	DQ0B	DQ2B	DQ2B						
B4	VREFB4N0	IO	RDN2		AE24	AA22	Y20	DQ0B	DQ2B	DQ2B						
B5	VREFB5N2	IO	RUP3		AD25	Y22	T17									
B5	VREFB5N2	IO	RDN3		AD26	Y23	T18									
B5	VREFB5N2	IO	DIFFIO_R61n		AB26	AA24	R17	DM5R/BWS#5R	DM3R/BWS#3R	DM0R/BWS#0R	DM3R/BWS#3R	DM3R/BWS#3R	DM1R/BWS#1R	DM3R/BWS#3R	DM3R/BWS#3R	DM1R/BWS#1R
B5	VREFB5N2	IO	DIFFIO_R61p		AC25	AA23	R16	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6	DQS5R/CQ5R#,DPCLK6
B5	VREFB5N2	IO	DIFFIO_R60n		AA25	AB24	W22	DQ5R	DQ3R	DQ0R				DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R60p		AB25	AB23	Y22	DQ5R	DQ3R	DQ0R				DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO			Y25			DQ5R	DQ3R	DQ0R						
B5	VREFB5N2	IO	DIFFIO_R59n		AE26	AC24		DQ5R	DQ3R	DQ0R	DQ3R	DQ3R	DQ1R			
B5	VREFB5N2	IO	DIFFIO_R59p		AE25	AC23					DQ3R	DQ3R	DQ1R			
B5	VREFB5N2	IO	DIFFIO_R58n		AH30											
B5	VREFB5N2	IO	DIFFIO_R58p		AJ30											
B5	VREFB5N2	IO	DIFFIO_R57n		AG29	AE26	W21	DQ5R	DQ3R	DQ0R				DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R57p		AH29	AE25	W20	DQ5R	DQ3R	DQ0R				DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R56n		Y27			DQ5R	DQ3R	DQ0R						
B5	VREFB5N2	IO	DIFFIO_R56p		AA27			DQ5R	DQ3R	DQ0R						
B5	VREFB5N2	IO	VREFB5N2		AA26	W23	U18									
B5	VREFB5N2	IO	DIFFIO_R55n	DEV_OE	AF28	W22	P14									
B5	VREFB5N2	IO	DIFFIO_R55p	DEV_CLRn	AF27	V21	P13									
B5	VREFB5N2	IO	DIFFIO_R54n		AF30	AD26	V21	DQ5R	DQ3R	DQ0R	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R54p		AG30	AD25	V20	DM3R/BWS#3R	DM3R/BWS#3R	DM0R/BWS#0R	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R53n		AE28	U23		DQ3R	DQ3R	DQ0R	DQ3R	DQ3R	DQ1R			
B5	VREFB5N2	IO	DIFFIO_R53p		AE27	V22		DQ3R	DQ3R	DQ0R	DQ3R	DQ3R	DQ1R			
B5	VREFB5N1	IO	DIFFIO_R52n		AE30	V24	U20				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R52p		AE29	V23	T19	DQ3R	DQ3R	DQ0R						
B5	VREFB5N1	IO	DIFFIO_R51n		AD28	AC26	T20				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R51p		AD27	AC25	R19	DQ3R	DQ3R	DQ0R	DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R50n		Y22	AB26	U22	DQ3R	DQ3R	DQ0R						
B5	VREFB5N1	IO	DIFFIO_R50p		AA22	AA25	V22	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7	DQS3R/CQ3R#,DPCLK7
B5	VREFB5N1	IO	DIFFIO_R49n		AC28	U22		DQ3R	DQ3R	DQ0R						
B5	VREFB5N1	IO	DIFFIO_R49p		AC27	T21					DM1R/BWS#1R	DM3R/BWS#3R	DM1R/BWS#1R			
B5	VREFB5N1	IO	DIFFIO_R48n		AB28	Y25	R21	DQ3R	DQ3R	DQ0R						
B5	VREFB5N1	IO	DIFFIO_R48p		AB27	Y24	R20				DQ1R	DQ3R	DQ1R	DM1R/BWS#1R	DM3R/BWS#3R	DM1R/BWS#1R
B5	VREFB5N1	IO	DIFFIO_R47n		AD30	Y26		DQ3R	DQ3R	DQ0R						
B5	VREFB5N1	IO	DIFFIO_R47p		AD29	AA26										
B5	VREFB5N1	IO	DIFFIO_R46n		AB30	T19	T22	DQ3R	DQ3R	DQ0R						
B5	VREFB5N1	IO	DIFFIO_R46p		AC30	U19	T21							DQ1R	DQ3R	DQ1R
B5	VREFB5N1	IO	VREFB5N1		V21	U24	P20									
B5	VREFB5N1	IO	DIFFIO_R45n		Y28											
B5	VREFB5N1	IO	DIFFIO_R45p		AA28											
B5	VREFB5N1	IO	DIFFIO_R44n		AA29	W25		DM1R								
B5	VREFB5N1	IO	DIFFIO_R44p		AB29	W24										
B5	VREFB5N1	IO	DIFFIO_R43n		Y30	V26	L15	DQ1R			DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R43p		AA30	W26	L14									
B5	VREFB5N1	IO	DIFFIO_R42n		T21			DQ1R								
B5	VREFB5N1	IO	DIFFIO_R42p		U21											
B5	VREFB5N0	IO	DIFFIO_R41n		V26	T23	P22				DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R41p		V25	T22	R22									
B5	VREFB5N0	IO	DIFFIO_R40n		T25	U26	M17									
B5	VREFB5N0	IO	DIFFIO_R40p		U25	U25	N17	DQ1R			DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R39n		W26	T25	L13									
B5	VREFB5N0	IO	DIFFIO_R39p		W25	T24	M13	DQ1R			DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R38n		W28	R20	N20									
B5	VREFB5N0	IO	DIFFIO_R38p		W27	R19	N19	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8	DQS1R/CQ1R#,DPCLK8
B5	VREFB5N0	IO	DIFFIO_R37n		W30											
B5	VREFB5N0	IO	DIFFIO_R37p		W29											
B5	VREFB5N0	IO	DIFFIO_R36n		V28	T26	N22	DQ1R			DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R36p		V27	R25	N21	DQ1R			DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R35n		U28	R23										
B5	VREFB5N0	IO	DIFFIO_R35p		U27	R22										
B5	VREFB5N0	IO	VREFB5N0		U30	R24	M20									
B5	VREFB5N0	IO	DIFFIO_R34n		T24	P20	M19	DQ1R						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R34p		T23	P19	M18	DQ1R						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R33n		T27	P24					DQ1R	DQ3R	DQ1R			
B5	VREFB5N0	IO	DIFFIO_R33p		T26	P23					DQ1R	DQ3R	DQ1R			
B5	VREFB5N0	CLKIO4	DIFFCLK_2n		V30	P26	M22									
B5	VREFB5N0	CLKIO5	DIFFCLK_2p		V29	R26	M21									
B6	VREFB6N2	CLKIO6	DIFFCLK_3n		T30	N26	L22									
B6	VREFB6N2	CLKIO7	DIFFCLK_3p		T29	N25	L21									
B6	VREFB6N2	IO	DIFFIO_R32n		R29	N20	L20	DM0R	DM0R/BWS#0R	DM0R/BWS#0R	DM0R	DM1R/BWS#1R	DM1R/BWS#1R	DM0R	DM1R/BWS#1R	DM1R/BWS#1R
B6	VREFB6N2	IO	DIFFIO_R32p		T28	N19	L19	DQ0R	DQ0R	DQ0R	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R31n		R26	N23	J20							DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R31p		R25	N22	J19							DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R30n		R28	M24		DQ0R	DQ0R	DQ0R	DQ0R	DQ1R	DQ1R			
B6	VREFB6N2	IO	DIFFIO_R30p		R27	N24		DQ0R	DQ0R	DQ0R	DQ0R	DQ1R	DQ1R			
B6	VREFB6N2	IO	DIFFIO_R29n		P30	L19	H22	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9	DQS0R/CQ1R,DPCLK9
B6	VREFB6N2	IO	DIFFIO_R29p		R30	M19	J21									
B6	VREFB6N2	IO	DIFFIO_R28n		P28											
B6	VREFB6N2	IO	DIFFIO_R28p		P27											
B6	VREFB6N2	IO	VREFB6N2		N26	M23	J15									
B6	VREFB6N2	IO	DIFFIO_R27n		N30											
B6	VREFB6N2	IO	DIFFIO_R27p		N29											
B6	VREFB6N2	IO	DIFFIO_R26n		P25	M26	J22									
B6	VREFB6N2	IO	DIFFIO_R26p		R24	M25	K22	DQ0R	DQ0R	DQ0R	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R25n		N28	L22	K20									
B6	VREFB6N2	IO	DIFFIO_R25p		N27	M22	K19	DQ0R	DQ0R	DQ0R	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R24n		M26	L26										
B6	VREFB6N2	IO	DIFFIO_R24p		N25	L25		DQ0R	DQ0R	DQ0R	DQ0R	DQ1R	DQ1R			
B6	VREFB6N2	IO	DIFFIO_R23n		M30	L24	H21									
B6	VREFB6N2	IO	DIFFIO_R23p		M29	L23	H20	DQ0R	DQ0R	DQ0R	DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R22n		M25		G21									
B6	VREFB6N2	IO	DIFFIO_R22p		N24		G20							DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R21n		M28	K26		DQ0R	DQ0R	DQ0R						
B6	VREFB6N1	IO	DIFFIO_R21p		M27	J26										
B6	VREFB6N1	IO	DIFFIO_R20n		K30	L21	E20				DQ0R	DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R20p		L30	K20	F20									

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B6	VREFB6N1	IO	DIFFIO_R19n		G30	J25	F22							DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R19p		H30	K24	G22	DQ2R	DQ0R	DQ0R		DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R18n		J30	K22						DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R18p		J29	K21					DQ2R	DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R17n		K29	J20	E22									
B6	VREFB6N1	IO	DIFFIO_R17p		K28	K19	E21								DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R16n		N21	H26	D22									
B6	VREFB6N1	IO	DIFFIO_R16p		P21	H25	D21	DM2R			DM2R	DM1R/BWS#1R	DM1R/BWS#1R	DM2R	DM1R/BWS#1R	DM1R/BWS#1R
B6	VREFB6N1	IO	DIFFIO_R15n		L28	F26	B22									
B6	VREFB6N1	IO	DIFFIO_R15p		L27	G26	C22	DQ2R	DQ0R	DQ0R	DQ2R	DQ1R	DQ1R		DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R14n		M22		A22									
B6	VREFB6N1	IO	DIFFIO_R14p		M21		A21							DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	VREFB6N1		L25	J24	H17									
B6	VREFB6N1	IO	DIFFIO_R13n		E30	J23	D20	DQ2R			DQ2R	DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R13p		F30	K23	D19	DQ2R	DQ0R	DQ0R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R12n		G29	G25	A20									
B6	VREFB6N1	IO	DIFFIO_R12p		G28	H24	B19							DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R11n		K27	E26	C20	DQ2R			DQ2R	DQ1R	DQ1R			
B6	VREFB6N1	IO	DIFFIO_R11p		K26	E25	C19	DQ2R			DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R10n		J26	D26	B21	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10	DQS2R/CQ3R,DPCLK10
B6	VREFB6N1	IO	DIFFIO_R10p		K25	D25	B20	DQ2R						DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R9n		D30	H23										
B6	VREFB6N1	IO	DIFFIO_R9p		D29	H22		DQ2R	DQ0R	DQ0R						
B6	VREFB6N0	IO	DIFFIO_R8n		H28											
B6	VREFB6N0	IO	DIFFIO_R8p		J28											
B6	VREFB6N0	IO	DIFFIO_R7n		C30	G24		DM4R	DM0R/BWS#0R	DM0R/BWS#0R						
B6	VREFB6N0	IO	DIFFIO_R7p		C29	F23		DQ4R	DQ0R	DQ0R						
B6	VREFB6N0	IO	VREFB6N0		K24	G23	G18									
B6	VREFB6N0	IO	DIFFIO_R6n		H25			DQ4R								
B6	VREFB6N0	IO	DIFFIO_R6p		J25											
B6	VREFB6N0	IO	DIFFIO_R5n		H27	E24		DQ4R	DQ0R	DQ0R						
B6	VREFB6N0	IO	DIFFIO_R5p		J27	F24		DQ4R	DQ0R	DQ0R						
B6	VREFB6N0	IO	DIFFIO_R4n		F29	C26										
B6	VREFB6N0	IO	DIFFIO_R4p		F28	C25										
B6	VREFB6N0	IO	DIFFIO_R3n		E28	B26		DQ4R	DQ0R	DQ0R	DQ2R	DQ1R	DQ1R			
B6	VREFB6N0	IO	DIFFIO_R3p		E27	B25		DQ4R			DQ2R	DQ1R	DQ1R			
B6	VREFB6N0	IO	DIFFIO_R2n		G27	C24	G17							DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R2p		G26	D24	G16	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11	DQS4R/CQ5R,DPCLK11
B6	VREFB6N0	IO	DIFFIO_R1n		F27	G22	G19	DQ4R	DQ0R	DQ0R				DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R1p		F26	F21	F18	DQ4R	DQ0R	DQ0R				DQ2R	DQ1R	DQ1R
B7	VREFB7N0	IO	RUP4		G25	E23	F16									
B7	VREFB7N0	IO	RDN4		F25	D23	F17									
B7	VREFB7N0	IO	PLL4_CLKOUTn		C27	E21	C17									
B7	VREFB7N0	IO	PLL4_CLKOUTp		D27	E22	C18									
B7	VREFB7N0	IO			F24	C23	B18									
B7	VREFB7N0	IO			E25											
B7	VREFB7N0	IO	DIFFIO_T69n		C28	H18	A18	DQ0T	DQ5T					DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T69p		D28	J17	A19	DQ0T	DQ5T					DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T68n		G24			DQ0T	DQ5T							
B7	VREFB7N0	IO	DIFFIO_T68p		H24			DQ0T	DQ5T							
B7	VREFB7N0	IO	DIFFIO_T67n		K22	J18	D17									
B7	VREFB7N0	IO	DIFFIO_T67p		K21	J19	E17									
B7	VREFB7N0	IO	DIFFIO_T66n		F23	C22		DQ0T	DQ5T		DQ2T	DQ5T	DQ5T			
B7	VREFB7N0	IO	DIFFIO_T66p		G23	D22		DQ0T	DQ5T		DQ2T	DQ5T	DQ5T			
B7	VREFB7N0	IO	DIFFIO_T65n		A29	A24	B16	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12	DQS0T/CQ1T,DPCLK12
B7	VREFB7N0	IO	DIFFIO_T65p		B30	A25	C16	DQ0T	DQ5T		DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	VREFB7N0		G21	E20	D16									
B7	VREFB7N0	IO	DIFFIO_T64n		F22	G17		DQ0T	DQ5T							
B7	VREFB7N0	IO	DIFFIO_T64p		G22	H17		DM0T	DM5T/BWS#5T							
B7	VREFB7N0	IO	DIFFIO_T63n		A28	A23	A16							DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T63p		B28	B23	A17	DQ2T	DQ5T	DQ5T						
B7	VREFB7N0	IO	DIFFIO_T62n		A27	D20										
B7	VREFB7N0	IO	DIFFIO_T62p		B27	D21		DQ2T	DQ5T	DQ5T						
B7	VREFB7N0	IO	DIFFIO_T61n		D24	H16	C15							DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T61p		E24	J16	D15	DQ2T	DQ5T	DQ5T						
B7	VREFB7N0	IO	DIFFIO_T60n		C26	E18										
B7	VREFB7N0	IO	DIFFIO_T60p		D26	E19		DQ2T	DQ5T	DQ5T						
B7	VREFB7N0	IO	DIFFIO_T59n		A25	H15										
B7	VREFB7N0	IO	DIFFIO_T59p		A26	J15		DQ2T	DQ5T	DQ5T						
B7	VREFB7N0	IO	DIFFIO_T58n		C25	B22					DQ2T	DQ5T	DQ5T			
B7	VREFB7N0	IO	DIFFIO_T58p		D25	C21										
B7	VREFB7N1	IO	DIFFIO_T57n		D22	C20		DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T			
B7	VREFB7N1	IO	DIFFIO_T57p		E22	D19										
B7	VREFB7N1	IO	DIFFIO_T56n		D21	F15	A15	DQ2T	DQ5T	DQ5T				DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T56p		E21	G15	B15							DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T55n		F19		C14	DQ2T	DQ5T	DQ5T						
B7	VREFB7N1	IO	DIFFIO_T55p		G20		D14							DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T54n		A24			DM2T	DM5T/BWS#5T	DM5T/BWS#5T						
B7	VREFB7N1	IO	DIFFIO_T54p		B25											
B7	VREFB7N1	IO	DIFFIO_T53n		B24											
B7	VREFB7N1	IO	DIFFIO_T53p		C24											
B7	VREFB7N1	IO	DIFFIO_T52n		C23	A22	A13				DQ2T	DQ5T	DQ5T			
B7	VREFB7N1	IO	DIFFIO_T52p		D23	B21	A14				DQ2T	DQ5T	DQ5T		DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T51n		A22	A20	C12							DM2T	DM5T/BWS#5T	DM5T/BWS#5T
B7	VREFB7N1	IO	DIFFIO_T51p		A23	A21	C13	DQ4T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T			
B7	VREFB7N1	IO	VREFB7N1		C21	E17	D13									
B7	VREFB7N1	IO	DIFFIO_T50n		F20											
B7	VREFB7N1	IO	DIFFIO_T50p		F21											
B7	VREFB7N1	IO	DIFFIO_T49n		B22	B19	B12							DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T49p		C22	C19	B13	DQ4T	DQ5T	DQ5T		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T48n		A21	C18					DM2T	DM5T/BWS#5T	DM5T/BWS#5T			
B7	VREFB7N1	IO	DIFFIO_T48p		B21	D18										
B7	VREFB7N1	IO	DIFFIO_T47n		F17	A18	G14									
B7	VREFB7N1	IO	DIFFIO_T47p		G17	A19	G15	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13	DQS2T/CQ3T,DPCLK13
B7	VREFB7N1	IO	DIFFIO_T46n		C20	D17					DQ4T	DQ5T	DQ5T			
B7	VREFB7N1	IO	DIFFIO_T46p		D20	E16					DQ4T	DQ5T	DQ5T			
B7	VREFB7N1	IO	DIFFIO_T45n		E18		H14	DQ4T	DQ3T	DQ5T						
B7	VREFB7N1	IO	DIFFIO_T45p		E19		J14	DQ4T	DQ3T	DQ5T				DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T44n		A20	B18										
B7	VREFB7N2	IO	DIFFIO_T44p		B19	C17					DQ4T	DQ5T	DQ5T			
B7	VREFB7N2	IO	DIFFIO_T43n		C19											

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B7	VREFB7N2	IO	DIFFIO_T43p		D19			DQ4T	DQ3T	DQ5T						
B7	VREFB7N2	IO	DIFFIO_T42n		A19	G14	C10							DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T42p		B18	H14	C11									
B7	VREFB7N2	IO	DIFFIO_T41n		C18	A16	H13	DQ4T	DQ3T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T41p		D18	A17	J13							DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	VREFB7N2		G16	D16	F12									
B7	VREFB7N2	IO	DIFFIO_T40n		F18	B17	A11				DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T40p		G18	C16	A12				DQ4T	DQ5T	DQ5T			
B7	VREFB7N2	IO	DIFFIO_T39n		A17	A15		DQ4T	DQ3T	DQ5T	DQ4T	DQ5T	DQ5T			
B7	VREFB7N2	IO	DIFFIO_T39p		A18	B15										
B7	VREFB7N2	IO	DIFFIO_T38n		C17											
B7	VREFB7N2	IO	DIFFIO_T38p		D17											
B7	VREFB7N2	IO	DIFFIO_T37n		K18	D15	A10	DQ4T	DQ3T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T37p		K19	E15	B10	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14	DQS4T/CQ5T,DPCLK14
B7	VREFB7N2	IO	DIFFIO_T36n		A16	C14	G12			DQ5T		DQ5T	DQ5T		DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T36p		B16	C15	H12	DM4T	DM3T/BWS#3T	DM5T/BWS#5T	DM4T	DM5T/BWS#5T	DM5T/BWS#5T	DM4T	DM5T/BWS#5T	DM5T/BWS#5T
B7	VREFB7N2	IO			K17											
B7	VREFB7N2	CLKIO8	DIFFCLK_5n		A15	A14	A9									
B7	VREFB7N2	CLKIO9	DIFFCLK_5p		B15	B14	B9									
B8A	VREFB8N0	CLKIO10	DIFFCLK_4n,REFCLK3n		K15	L14	J10									
B8A	VREFB8N0	CLKIO11	DIFFCLK_4p,REFCLK3p		L15	L15	K10									
B8	VREFB8N0	IO	DIFFIO_T35n		F16	B13										
B8	VREFB8N0	IO	DIFFIO_T35p		G15	C13										
B8	VREFB8N0	IO	DIFFIO_T34n		C16	A12	A8	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15	DQS5T/CQ5T#,DPCLK15
B8	VREFB8N0	IO	DIFFIO_T34p		D16	A13	B7	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T33n		G13											
B8	VREFB8N0	IO	DIFFIO_T33p		G14											
B8	VREFB8N0	IO	DIFFIO_T32n		A13	A11		DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T			
B8	VREFB8N0	IO	DIFFIO_T32p		A14	B11		DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T			
B8	VREFB8N0	IO	DIFFIO_T31n		E16	A10	A6				DQ5T	DQ3T	DQ5T			
B8	VREFB8N0	IO	DIFFIO_T31p		F15	B10	A7				DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	VREFB8N0		B13	D14	D12									
B8	VREFB8N0	IO	DIFFIO_T30n		E15	A8					DQ5T	DQ3T	DQ5T			
B8	VREFB8N0	IO	DIFFIO_T30p		F14	A9										
B8	VREFB8N0	IO	DIFFIO_T29n		A12	A6		DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T			
B8	VREFB8N0	IO	DIFFIO_T29p		B12	A7					DQ5T	DQ3T	DQ5T			
B8	VREFB8N0	IO	DIFFIO_T28n		C15	J14	A4							DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T28p		D15	K13	A5	DQ5T	DQ3T	DQ5T						
B8	VREFB8N0	IO	DIFFIO_T27n		A10											
B8	VREFB8N0	IO	DIFFIO_T27p		A11											
B8	VREFB8N0	IO	DIFFIO_T26n		C14	E13	A2	DQ5T	DQ3T	DQ5T				DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T26p		D14	E14	A3							DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T25n		C13											
B8	VREFB8N0	IO	DIFFIO_T25p		D13											
B8	VREFB8N0	IO	DIFFIO_T24n		E13	H13	B3							DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T24p		F13	J13	B4	DQ5T	DQ3T	DQ5T						
B8	VREFB8N0	IO	DIFFIO_T23n		B10	D13	B6							DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T23p		C10	E12	C6							DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T22n		F12	C11		DQ5T	DQ3T	DQ5T						
B8	VREFB8N1	IO	DIFFIO_T22p		G12	C12					DQ5T	DQ3T	DQ5T			
B8	VREFB8N1	IO	DIFFIO_T21n		C12	A5				DQ5T						
B8	VREFB8N1	IO	DIFFIO_T21p		D12	B5										
B8	VREFB8N1	IO	DIFFIO_T20n		A8	H12	A1	DM5T	DM3T/BWS#3T	DQ5T						
B8	VREFB8N1	IO	DIFFIO_T20p		B7	J12	B1							DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T19n		A9	J11	C8									
B8	VREFB8N1	IO	DIFFIO_T19p		B9	K12	D8	DQ3T	DQ3T	DQ5T						
B8	VREFB8N1	IO	DIFFIO_T18n		A7	D12										
B8	VREFB8N1	IO	DIFFIO_T18p		B6	E11		DQ3T	DQ3T	DQ5T						
B8	VREFB8N1	IO	DIFFIO_T17n		C11	G11	C1							DM5T/BWS#5T	DM3T/BWS#3T	DM5T/BWS#5T
B8	VREFB8N1	IO	DIFFIO_T17p		D11	H11	C2	DQ3T	DQ3T	DQ5T						
B8	VREFB8N1	IO	VREFB8N1		G11	D11	D11									
B8	VREFB8N1	IO	DIFFIO_T16n		A5	B6		DM3T/BWS#3T	DM1T/BWS#1T	DM5T/BWS#5T	DM5T/BWS#5T	DM3T/BWS#3T	DM5T/BWS#5T			
B8	VREFB8N1	IO	DIFFIO_T16p		A6	B7										
B8	VREFB8N1	IO	DIFFIO_T15n		D7	A4	C7	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16	DQS3T/CQ3T#,DPCLK16
B8	VREFB8N1	IO	DIFFIO_T15p		E7	B4	D7				DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T14n		E12	B9	C3									
B8	VREFB8N1	IO	DIFFIO_T14p		F11	C10	C4	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T13n		C4	A2	E8				DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T13p		D4	A3	F8	DQ3T	DQ1T							
B8	VREFB8N1	IO	DIFFIO_T12n		C5			DQ3T	DQ1T	DQ5T						
B8	VREFB8N1	IO	DIFFIO_T12p		C6											
B8	VREFB8N2	IO	DIFFIO_T11n		C7	C4		DQ3T	DQ1T	DQ5T	DQ3T	DQ3T	DQ5T			
B8	VREFB8N2	IO	DIFFIO_T11p		D6	C5		DQ3T	DQ1T							
B8	VREFB8N2	IO	DIFFIO_T10n		D5	B1	C5	DQ3T	DQ1T					DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T10p		E6	B2	D4	DQ1T	DQ1T							
B8	VREFB8N2	IO	DIFFIO_T9n		F10	D9	D5	DQ1T	DQ1T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T9p		G10	D10	E5	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17	DQS1T/CQ1T#,DPCLK17
B8	VREFB8N2	IO	DIFFIO_T8n		C3	G10	C9	DQ1T	DQ1T	DQ5T				DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T8p		D3	H10	D9	DQ1T	DQ1T	DQ5T				DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T7n		D10	G9	D6	DQ1T	DQ1T					DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T7p		E10	H9	E6	DQ1T	DQ1T					DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T6n		C9	D8	G7	DQ1T	DQ1T							
B8	VREFB8N2	IO	DIFFIO_T6p		D9	E8	H7	DQ1T	DQ1T							
B8	VREFB8N2	IO	VREFB8N2		C8	E9	D10									
B8	VREFB8N2	IO	DIFFIO_T5n		E9											
B8	VREFB8N2	IO	DIFFIO_T5p		F9			DQ1T	DQ1T							
B8	VREFB8N2	IO	DIFFIO_T4n	DATA4	C2	C6	F6	DM1T/BWS#1T	DM1T/BWS#1T	DM5T/BWS#5T	DM3T/BWS#3T	DM3T/BWS#3T	DM5T/BWS#5T	DM3T/BWS#3T	DM3T/BWS#3T	DM5T/BWS#5T
B8	VREFB8N2	IO	DIFFIO_T4p	DATA3	D1	C7	G6									
B8	VREFB8N2	IO	DIFFIO_T3n		E3	C3			DQ1T		DQ3T	DQ3T	DQ5T			
B8	VREFB8N2	IO	DIFFIO_T3p		E4	D3			DQ1T		DQ3T	DQ3T	DQ5T			
B8	VREFB8N2	IO	DIFFIO_T2n		F4	C2			DQ1T		DQ3T	DQ3T	DQ5T			
B8	VREFB8N2	IO	DIFFIO_T2p		F5	D2			DQ1T		DQ3T	DQ3T	DQ5T			
B8	VREFB8N2	IO	DIFFIO_T1n	DATA2	H9	C8	G8									
B8	VREFB8N2	IO	DIFFIO_T1p		J9	C9	H8									
B8	VREFB8N2	IO			D8	F8										
B8	VREFB8N2	IO	PLL2_CLKOUTn		F6	D7	G10									
B8	VREFB8N2	IO	PLL2_CLKOUTp		G6	E7	H9									
B8	VREFB8N2	IO	PLL7_CLKOUTn		F7	C1										
B8	VREFB8N2	IO	PLL7_CLKOUTp		G7	D1										
B8	VREFB8N2	IO	PLL8_CLKOUTn		F8	E1										
B8	VREFB8N2	IO	PLL8_CLKOUTp		G8	E2										

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B8	VREFB8N2	IO		CLKUSR	A4	D4	G11									
B8B	VREFB8N2	REFCLK4n	DIFFCLK_8n		K11	K10										
B8B	VREFB8N2	REFCLK4p	DIFFCLK_8p,CLKIO17		L11	L10										
B8B	VREFB8N2	REFCLK5n	DIFFCLK_9n		L10	K9										
B8B	VREFB8N2	REFCLK5p	DIFFCLK_9p,CLKIO19		M10	L9										
B9	VREFB8N2	IO		DATA0	A3	D6	K4									
B9	VREFB8N2	IO		DATA1,ASDO	G9	E6	D1									
B9	VREFB8N2	IO		NCSO	B4	D5	J4									
B9		DCLK		DCLK	B3	F6	D3									
B9		nCONFIG		nCONFIG	B1	E5	H4									
B9		nCE		nCE	C1	H7	D2									
B9		TDI		TDI	E2	G6	F5									
B9		TCK		TCK	F2	G8	E4									
B9		TMS		TMS	E1	F5	G5									
B9		TDO		TDO	F1	H8	E3									
		GND			J7	J7	F3									
		GND			L7	K6	M3									
		GND			R7	N6	T4									
		GND			T7	P6	U3									
		GND			AA8	U6	V19									
		GND			Y9	V7	E19									
		GND			AC24	W20	H5									
		GND			J24	G20	AA11									
		GND			AA11	M7	AA14									
		GND			AA19	AB10	AA17									
		GND			AB10	AB13	AA5									
		GND			AC11	AB16	AA8									
		GND			AC14	AB19	B11									
		GND			AC17	AB22	B14									
		GND			AC20	AB25	B17									
		GND			AC23	AE12	B2									
		GND			AC26	AE16	B5									
		GND			AC29	AE20	B8									
		GND			AC6	AE24	C21									
		GND			AF11	AE4	D18									
		GND			AF14	AE8	E7									
		GND			AF17	B12	F11									
		GND			AF20	B16	F13									
		GND			AF23	B20	F15									
		GND			AF26	B24	F21									
		GND			AF29	B3	F9									
		GND			AF5	B8	H11									
		GND			AF8	F10	H18									
		GND			AG2	F12	J6									
		GND			AJ11	F17	J8									
		GND			AJ14	F19	K11									
		GND			AJ17	F22	K15									
		GND			AJ2	F25	K21									
		GND			AJ20	F7	K5									
		GND			AJ23	G13	K7									
		GND			AJ26	H19	K9									
		GND			AJ29	J22	L10									
		GND			AJ5	J8	L12									
		GND			AJ8	K11	L18									
		GND			B11	K15	L6									
		GND			B14	K17	L8									
		GND			B17	K25	M5									
		GND			B2	L12	M9									
		GND			B20	L16	N10									
		GND			B23	L18	N4									
		GND			B26	L8	N6									
		GND			B29	M11	P11									
		GND			B5	M13	P16									
		GND			B8	M15	P18									
		GND			D2	M17	P21									
		GND			E11	M21	P9									
		GND			E14	M9	R12									
		GND			E17	N10	R6									
		GND			E20	N12	U10									
		GND			E23	N14	U17									
		GND			E26	N16	U21									
		GND			E29	N18	V11									
		GND			E5	N8	V14									
		GND			E8	P11	V5									
		GND			F3	P13	V8									
		GND			H11	P15	Y21									
		GND			H14	P17	R10									
		GND			H17	P22	R15									
		GND			H20	P25	N13									
		GND			H23	P9	M14									
		GND			H26	R10	N15									
		GND			H29	R12	M16									
		GND			H8	R14	L16									
		GND			J8	R16	K17									
		GND			K12	R18	J16									
		GND			K14	T11	K13									
		GND			K20	T13	H15									
		GND			K7	T17	J12									
		GND			L13	T7	AA1									
		GND			L17	U21	AA2									
		GND			L19	U8	AB2									
		GND			L21	V25	E1									
		GND			L23	Y16	E2									
		GND			L26	Y18	G1									
		GND			L29	Y8	G2									
		GND			L9	R8	J1									
		GND			M12	AB1	J2									
		GND			M14	AB2	L1									
		GND			M16	AC2	L2									
		GND			M18	AD1	N1									
		GND			M20	E3	N2									

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		GND			N11	E4	R1									
		GND			N13	F1	R2									
		GND			N15	F2	U1									
		GND			N17	G3	U2									
		GND			N19	G4	W1									
		GND			N9	H1	W2									
		GND			P10	H2										
		GND			P12	J3										
		GND			P14	J4										
		GND			P16	K1										
		GND			P18	K2										
		GND			P20	L3										
		GND			P23	L4										
		GND			P26	M1										
		GND			P29	M2										
		GND			P8	N3										
		GND			R11	N4										
		GND			R13	P1										
		GND			R15	P2										
		GND			R17	R3										
		GND			R19	R4										
		GND			R21	T1										
		GND			R9	T2										
		GND			T10	U3										
		GND			T12	U4										
		GND			T14	V1										
		GND			T16	V2										
		GND			T18	W3										
		GND			T20	W4										
		GND			T22	Y1										
		GND			U11	Y2										
		GND			U13											
		GND			U15											
		GND			U17											
		GND			U19											
		GND			U23											
		GND			U26											
		GND			U29											
		GND			U9											
		GND			V10											
		GND			V14											
		GND			V16											
		GND			V18											
		GND			V20											
		GND			V24											
		GND			V8											
		GND			W13											
		GND			W17											
		GND			W19											
		GND			W21											
		GND			W9											
		GND			Y10											
		GND			Y14											
		GND			Y16											
		GND			Y23											
		GND			Y26											
		GND			Y29											
		GND			AA3											
		GND			AA4											
		GND			AA5											
		GND			AB1											
		GND			AB2											
		GND			AB5											
		GND			AB6											
		GND			AC3											
		GND			AC4											
		GND			AC5											
		GND			AD1											
		GND			AD2											
		GND			AD5											
		GND			AE2											
		GND			AF1											
		GND			AF2											
		GND			G1											
		GND			G2											
		GND			G3											
		GND			G4											
		GND			G5											
		GND			H1											
		GND			H2											
		GND			H5											
		GND			H6											
		GND			J3											
		GND			J4											
		GND			J5											
		GND			K1											
		GND			K2											
		GND			L3											
		GND			L4											
		GND			L5											
		GND			M1											
		GND			M2											
		GND			M6											
		GND			N3											
		GND			N4											
		GND			N6											
		GND			P1											
		GND			P2											
		GND			P5											
		GND			R3											
		GND			R4											

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		GND			R5											
		GND			T1											
		GND			T2											
		GND			T5											
		GND			U3											
		GND			U4											
		GND			U5											
		GND			V1											
		GND			V2											
		GND			V6											
		GND			W3											
		GND			W4											
		GND			W5											
		GND			W6											
		GND			Y1											
		GND			Y2											
		GND			K8											
		GND			AB7											
		VCC_CLKIN3A			W16	U14	N12									
		VCC_CLKIN3B			Y12	V9	P7									
		VCC_CLKIN8A			K16	K14	H10									
		VCC_CLKIN8B			K10	J9										
		VCCD_PLL			K6	J6	G3									
		VCCD_PLL			M8	L6	M4									
		VCCD_PLL			P7	M6	R4									
		VCCD_PLL			U7	R6	U4									
		VCCD_PLL			Y7	T6	V18									
		VCCD_PLL			Y8	V6	E18									
		VCCD_PLL			AB23	Y20										
		VCCD_PLL			J23	G21										
		VCCINT			AA10	L7	J5									
		VCCINT			AA14	J10	F7									
		VCCINT			K13	K16	G13									
		VCCINT			L12	K18	G9									
		VCCINT			L14	K8	H6									
		VCCINT			L16	L11	J11									
		VCCINT			L18	L13	J17									
		VCCINT			L20	L17	J7									
		VCCINT			M11	M10	J9									
		VCCINT			M13	M12	K16									
		VCCINT			M15	M14	K6									
		VCCINT			M17	M16	K8									
		VCCINT			M19	M18	L11									
		VCCINT			M9	M8	L17									
		VCCINT			N10	N11	L5									
		VCCINT			N12	N13	L7									
		VCCINT			N14	N15	L9									
		VCCINT			N16	N17	M10									
		VCCINT			N18	N9	M12									
		VCCINT			N20	P10	M6									
		VCCINT			N8	P12	N16									
		VCCINT			P11	P14	N5									
		VCCINT			P13	P16	N9									
		VCCINT			P15	P18	P12									
		VCCINT			P17	P8	P17									
		VCCINT			P19	R11	P6									
		VCCINT			P9	R13	P8									
		VCCINT			R10	R15	R7									
		VCCINT			R12	R17	T10									
		VCCINT			R14	R7	T12									
		VCCINT			R16	R9	U16									
		VCCINT			R18	T12	P10									
		VCCINT			R20	T16	T15									
		VCCINT			T11	T18	N14									
		VCCINT			T13	U11	M15									
		VCCINT			T15	U13	P15									
		VCCINT			T17	U15	K14									
		VCCINT			T19	U17	H16									
		VCCINT			T9	V10	K12									
		VCCINT			U10	V8										
		VCCINT			U12	T8										
		VCCINT			U14											
		VCCINT			U16											
		VCCINT			U18											
		VCCINT			U20											
		VCCINT			U8											
		VCCINT			V13											
		VCCINT			V17											
		VCCINT			V19											
		VCCINT			V9											
		VCCINT			W10											
		VCCINT			W14											
		VCCINT			W18											
		VCCINT			W20											
		VCCINT			W8											
		VCCINT			Y11											
		VCCINT			Y13											
		VCCINT			Y15											
		VCCINT			K9											
		VCCINT			AB8											
		VCCIO3			AB12	AA10	U11									
		VCCIO3			AB15	AA11	U8									
		VCCIO3			AC10	AA12	U9									
		VCCIO3			AC12	AA13	V10									
		VCCIO3			AC13	AA14	V12									
		VCCIO3			AC15	W8										
		VCCIO3			AC9											
		VCCIO3			AD11											
		VCCIO3			AD12											
		VCCIO3			AD13											
		VCCIO3			AD14											

Bank Number	VREFB Group	Pin Name / Function (2)	Optional Function(s) (2)	Configuration Function	F896	F672	F484	DQS for X8/X9 in F896	DQS for X16/X18 in F896	DQS for X32/X36 in F896	DQS for X8/X9 in F672	DQS for X16/X18 in F672	DQS for X32/X36 in F672	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		VCCIO3			AD15											
		VCCIO4			AB18	AA16	U13									
		VCCIO4			AB19	AA18	V15									
		VCCIO4			AB20	AA19	V16									
		VCCIO4			AC18	AB17	V17									
		VCCIO4			AC19	Y15										
		VCCIO4			AC21	Y19										
		VCCIO4			AC22											
		VCCIO4			AD17											
		VCCIO4			AD18											
		VCCIO4			AD19											
		VCCIO4			AD20											
		VCCIO4			AD21											
		VCCIO5			AA23	P21	N18									
		VCCIO5			AA24	R21	P19									
		VCCIO5			U22	T20	R18									
		VCCIO5			U24	U20										
		VCCIO5			V22	V20										
		VCCIO5			V23											
		VCCIO5			W22											
		VCCIO5			W23											
		VCCIO5			W24											
		VCCIO5			Y24											
		VCCIO6			L22	H21	H19									
		VCCIO6			L24	J21	J18									
		VCCIO6			M23	L20	K18									
		VCCIO6			M24	M20										
		VCCIO6			N22	N21										
		VCCIO6			N23											
		VCCIO6			P22											
		VCCIO6			P24											
		VCCIO6			R22											
		VCCIO6			R23											
		VCCIO7			G19	F16	E13									
		VCCIO7			H18	F18	E14									
		VCCIO7			H19	F20	E15									
		VCCIO7			H21	G16	E16									
		VCCIO7			H22	G18	F14									
		VCCIO7			J17	G19										
		VCCIO7			J18											
		VCCIO7			J19											
		VCCIO7			J20											
		VCCIO7			J21											
		VCCIO7			J22											
		VCCIO8			H10	E10	E10									
		VCCIO8			H12	F11	E11									
		VCCIO8			H13	F13	E12									
		VCCIO8			H15	F14	E9									
		VCCIO8			H16	F9	F10									
		VCCIO8			J10	G12										
		VCCIO8			J11											
		VCCIO8			J12											
		VCCIO8			J13											
		VCCIO8			J14											
		VCCIO8			J15											
		VCCIO8			J16											
		VCCIO9			H7	G7	G4									
		VCCA			J6	H6	F4									
		VCCA			L8	K7	L4									
		VCCA			R8	N7	T5									
		VCCA			T8	P7	V4									
		VCCA			AA7	U7	U19									
		VCCA			AA9	W6	F19									
		VCCA			AB24	W21										
		VCCA			K23	H20										
		NC			AG1	AB3	Y3									
		NC			AH1	AB4	AA3									
		NC			A2											
		NC			AK2											
		VCCL_GXB			AD4	AD2	V3									
		VCCL_GXB			K5	G5	K3									
		VCCL_GXB			M5	H5	L3									
		VCCL_GXB			N7	L5	N3									
		VCCL_GXB			P6	P5	T3									
		VCCL_GXB			AA6	AA3										
		VCCL_GXB			T6	AA4										
		VCCL_GXB			V5	U5										
		VCCL_GXB			Y5	Y5										
		VCCH_GXB			L6	J5	H3									
		VCCH_GXB			N5	M5	P3									
		VCCH_GXB			U6	R5										
		VCCH_GXB			W7	V5										
		RREF0			AE1	AC1	AB1									
		VCCA_GXB			AD3	AC3	W3									
		VCCA_GXB			M7	K5	J3									
		VCCA_GXB			R6	N5	R3									
		VCCA_GXB			V7	T5										
		VCCA_GXB			Y6	W5										

Notes:
(1) For DQS pins that do not have the associated DQ pins, the particular DQS is not supported.
(2) For implementation of transceiver applications that run at ≥2.97Gbps data rate, you must refer to the Cyclone IV Device Family Pin Connection Guidelines.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
CLKIO[5, 7, 9, 11, 12,14], DIFFCLK_[2..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLKIO[4, 6, 8, 10, 13, 15], DIFFCLK_[2..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
DIFFCLK_[0, 1, 8, 9]p, CLKIO[17, 19, 20, 22]	Clock, Input	Optional positive terminal inputs for differential global clock input or single-ended clock input.
DIFFCLK_[0, 1, 8, 9]n	Clock, Input	Optional negative terminal inputs for differential global clock input.
PLL[1..8]_CLKOUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
PLL[1..8]_CLKOUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
	Configuration/JTAG Pins	
MSEL[0..3]	Input	Configuration input pins that set the Cyclone IV GX device configuration scheme. The smaller devices like EP4CGX15, EP4CGX22, and EP4CGX30 do not have the MSEL3 pin.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
NCEO	I/O, Output	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as an user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
NCSO	I/O, Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO, DATA1	Input (PS, FPP) Output (AS)	This pin functions as DATA1 in PS and FPP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide configuration data is presented to the target device on DATA[0..7]. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual- Purpose Pin settings. ASDO: Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[2..7]	Input (FPP)	Data inputs. Byte-wide configuration data is presented to the target device on DATA [0..7]. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [2..7] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.

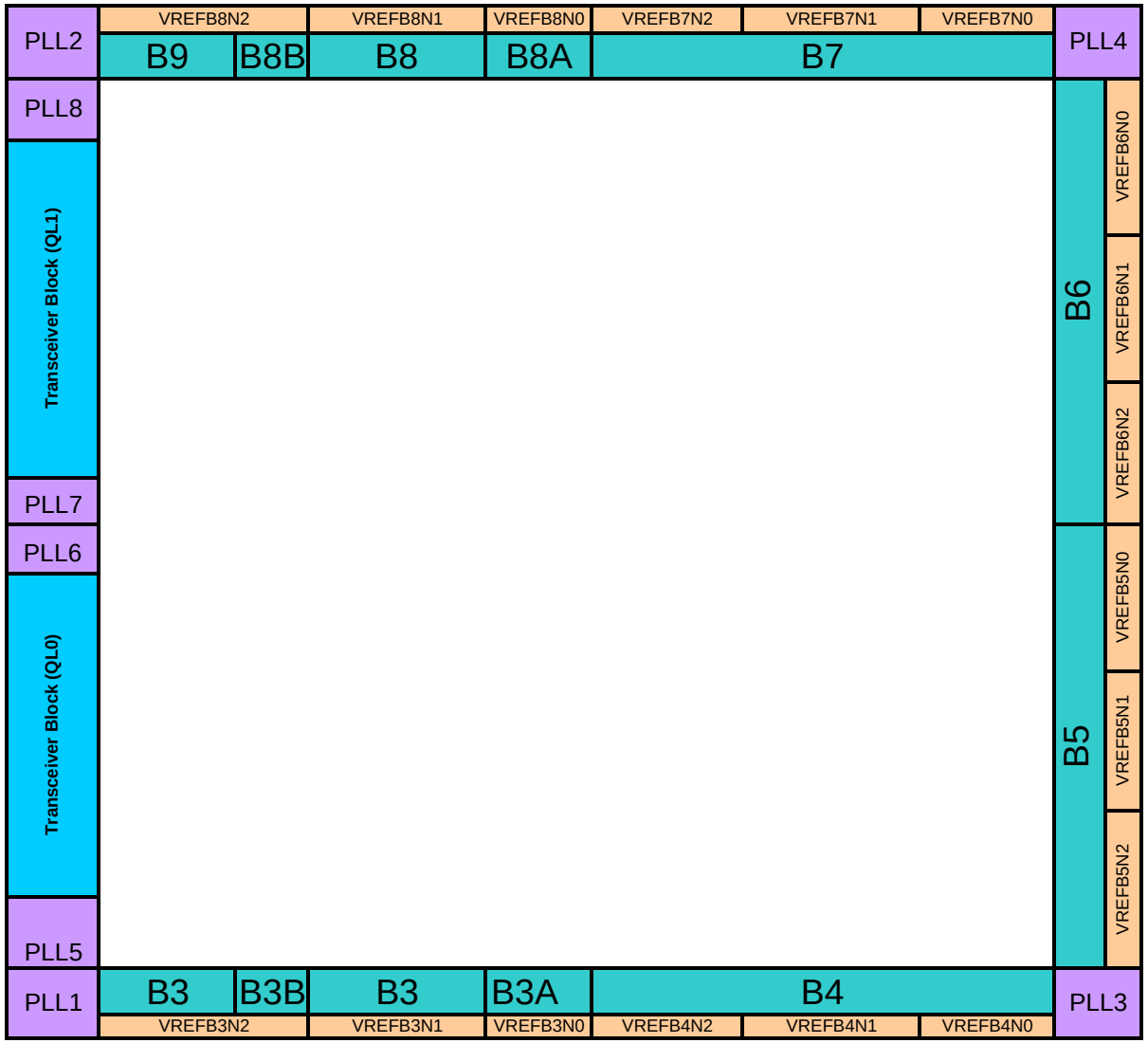
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
Differential I/O Pins		
DIFFIO_[R,T,B]0..72][n,p]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[0..5][R,T,B]/CQ[0,1,3,5][R,T,B][#],DPCLK[0..17]	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ[0..5][R,T,B]	I/O, DQ	Optional data signal for use in external memory interface.
DM[0..5][R,B,T]/BWS#[0..5][R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDR II SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.
Reference Pins		
RUP[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. If the RUP pin is not used, this pin can function as a regular I/O pin.
RDN[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If the RDN pin is not used, this pin can function as a regular I/O pin.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCCINT	Power	These are internal logic array voltage supply pins.
VCCD_PLL	Power	Digital power for PLLs. The designer must power up these pins, even if the PLL is not used.
VCCA	Power	Analog power for PLLs. All VCCA pins must be powered and all VCCA pins must be powered up and powered down at the same time even if not all the PLLs are used. Designer is advised to keep VCCA isolated from other VCC for better jitter performance.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
VCCIO[3..9]	Power	These are I/O supply voltage pins for banks 3 through 9. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards.
VCC_CLKIN[3,8]A	Power	CLLKIN power in bank 3A and bank 8A.
VREFB[3..8]N[0..2]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
GND	Ground	Device ground pins. All GND pins should be connected to GND plane on the board.
Transceiver Pins		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX, and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA_GXB	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0..7]p	Input	High speed positive differential receiver channels.
GXB_RX[0..7]n	Input	High speed negative differential receiver channels.
GXB_TX[0..7]p	Output	High speed positive differential transmitter channels.
GXB_TX[0..7]n	Output	High speed negative differential transmitter channels.
REFCLK[0..5]p *(2)*	Input	High speed differential reference clock positive.
REFCLK[0..5]n *(2)*	Input	High speed differential reference clock complement.
RREF0	Input	Reference resistor for transceiver.

Notes:

(1) The pin definitions are prepared based on the device with the largest density, EP4CGX150. For the availability of pins in each density, refer to the pin list.

(2) For implementation of transceiver applications that run at ≥2.97Gbps data rate, you must refer to the Cyclone IV Device Family Pin Connection Guidelines.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to provide an idea of placement on the device. For exact locations, refer to the pin list and the Quartus® II software.

Version Number	Date	Changes Made
1.0	6/23/2010	Initial release.
1.1	11/8/2010	Added new note in Pin List and Pin Definitions.