Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F256/ U256	E144 (4)	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in E144
B1	VREFB1N0	IO			D4	1			
B1	VREFB1N0	IO			E5	2			
B1	VREFB1N0	IO			F5	3			
B1	VREFB1N0	IO			B1		DQS2L/CQ3L	DQS2L/CQ3L	DQS2L/CQ3L
B1	VREFB1N0	IO	DIFFIO_L1p		C2				
B1	VREFB1N0	IO	DIFFIO_L1n	DATA1,ASDO	C1	6			
B1	VREFB1N0	IO	VREFB1N0		F3	7			
B1	VREFB1N0	IO	DIFFIO_L2p	FLASH_nCE,nCSO	D2	8			
B1	VREFB1N0	IO	DIFFIO_L2n		D1				
B1	VREFB1N0	nSTATUS		nSTATUS	F4	9			
B1	VREFB1N0	IO			G5				
B1	VREFB1N0	IO	DIFFIO_L3p		F2				
B1	VREFB1N0	IO	DIFFIO_L3n		F1				
B1	VREFB1N0	IO	DIFFIO_L4p		G2	10	DQS0L/CQ1L,DPCLK0	DQS0L/CQ1L,DPCLK0	DQS0L/CQ1L,DPCLK0
B1	VREFB1N0	IO	DIFFIO_L4n		G1	11			
B1	VREFB1N0	DCLK		DCLK	H1	12			
B1	VREFB1N0	IO		DATA0	H2	13			
B1	VREFB1N0	nCONFIG		nCONFIG	H5	14			
B1	VREFB1N0	TDI		TDI	H4	15			
B1	VREFB1N0	TCK		TCK	H3	16			
B1	VREFB1N0	TMS		TMS	J5	18			
B1	VREFB1N0	TDO		TDO	J4	20			
B1	VREFB1N0	nCE		nCE	J3	21			
B1	VREFB1N0	CLK1	DIFFCLK_0n		E1	23			
B2	VREFB2N0	CLK2	DIFFCLK_1p		M2	24			
B2	VREFB2N0	CLK3	DIFFCLK_1n		M1	25			
B2	VREFB2N0	IO	DIFFIO_L5p		J2		DQ1L		
B2	VREFB2N0	IO	DIFFIO_L5n		J1		DQ1L		
B2	VREFB2N0	IO			J6				
B2	VREFB2N0	IO	DIFFIO_L6p		K6				
B2	VREFB2N0	IO	DIFFIO_L6n		L6	28			
B2	VREFB2N0	IO	DIFFIO_L7p		K2				
B2	VREFB2N0	IO	DIFFIO_L7n		K1		DQ1L		
B2	VREFB2N0	IO	DIFFIO_L8p		L2	30	DQS1L/CQ1L#,DPCLK1	DQS1L/CQ1L#,DPCLK1	DQS1L/CQ1L#,DPCLK1
B2	VREFB2N0	IO	DIFFIO_L8n		L1		DQ1L		
B2	VREFB2N0	IO	VREFB2N0		L3	31			
B2	VREFB2N0	IO	DIFFIO_L9p		N2		DQ1L		
B2	VREFB2N0	IO	DIFFIO_L9n		N1		DQ1L		
B2	VREFB2N0	IO	RUP1		K5	32	DQ1L		
B2	VREFB2N0	IO	RDN1		L4	33	DQ1L		
B2	VREFB2N0	IO				34			
B2	VREFB2N0	IO			R1		DQS3L/CQ3L#	DQS3L/CQ3L#	DQS3L/CQ3L#
B2	VREFB2N0	IO	DIFFIO_L10p		P2		DQ1L		
B2	VREFB2N0	IO	DIFFIO_L10n		P1		DM1L/BWS#1L		
B3	VREFB3N0	IO	DIFFIO_B1p		N3	38			
B3	VREFB3N0	IO	DIFFIO_B1n		P3	39	DM3B/BWS#3B	DM5B/BWS#5B	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F256/U256	E144 (4)	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in E144
B3	VREFB3N0	IO	DIFFIO_B2p		R3		DQ3B	DQ5B	
B3	VREFB3N0	IO	DIFFIO_B2n		T3				
B3	VREFB3N0	IO			T2	42	DQS1B/CQ1B#,DPCLK2	DQS1B/CQ1B#,DPCLK2	DQS1B/CQ1B#,DPCLK2
B3	VREFB3N0	IO	PLL1_CLKOUTp		R4	43			
B3	VREFB3N0	IO	PLL1_CLKOUTn		T4	44			
B3	VREFB3N0	IO	DIFFIO_B4p		N5		DQ3B	DQ5B	
B3	VREFB3N0	IO	DIFFIO_B4n		N6		DQ3B	DQ5B	
B3	VREFB3N0	IO			M6		DQ3B	DQ5B	
B3	VREFB3N0	IO	VREFB3N0		P6	46			
B3	VREFB3N0	IO	DIFFIO_B5p		M7		DQS3B/CQ3B#	DQS3B/CQ3B#	DQS3B/CQ3B#
B3	VREFB3N0	IO	DIFFIO_B5n		K8				
B3	VREFB3N0	IO	DIFFIO_B6p		R5		DQ3B	DQ5B	
B3	VREFB3N0	IO	DIFFIO_B6n		T5				
B3	VREFB3N0	IO	DIFFIO_B7p		R6		DQ3B	DQ5B	
B3	VREFB3N0	IO	DIFFIO_B7n		T6				
B3	VREFB3N0	IO			L7		DQ3B	DQ5B	
B3	VREFB3N0	IO	DIFFIO_B8p		R7		DQ3B	DQ5B	
B3	VREFB3N0	IO	DIFFIO_B8n		T7		DQS5B/CQ5B#	DQS5B/CQ5B#	DQS5B/CQ5B#
B3	VREFB3N0	IO	DIFFIO_B9p		L8	49	DQ3B	DQ5B	DQ1B
B3	VREFB3N0	IO	DIFFIO_B9n		M8	50	DM5B/BWS#5B	DM5B/BWS#5B	DQ1B
B3	VREFB3N0	IO	DIFFIO_B10p		N8	51	DQ5B	DQ5B	DQ1B
B3	VREFB3N0	IO	DIFFIO_B10n		P8		DQ5B	DQ5B	
B3	VREFB3N0	IO	DIFFIO_B11p		R8	52			
B3	VREFB3N0	IO	DIFFIO_B11n		T8	53			
B4	VREFB4N0	IO	DIFFIO_B12p		R9	54			
B4	VREFB4N0	IO	DIFFIO_B12n		T9	55			
B4	VREFB4N0	IO	DIFFIO_B13p		K9				
B4	VREFB4N0	IO	DIFFIO_B13n		L9				
B4	VREFB4N0	IO	DIFFIO_B14p		M9				
B4	VREFB4N0	IO	DIFFIO_B14n		N9		DQ5B	DQ5B	
B4	VREFB4N0	IO	DIFFIO_B15p		R10	58	DQ5B	DQ5B	DQ1B
B4	VREFB4N0	IO	DIFFIO_B15n		T10		DQS4B/CQ5B	DQS4B/CQ5B	DQS4B/CQ5B
B4	VREFB4N0	IO	DIFFIO_B16p		R11	59	DQ5B	DQ5B	DQ1B
B4	VREFB4N0	IO	DIFFIO_B16n		T11	60			DQ1B
B4	VREFB4N0	IO	DIFFIO_B17p		R12		DQ5B	DQ5B	
B4	VREFB4N0	IO	DIFFIO_B17n		T12		DQ5B	DQ5B	
B4	VREFB4N0	IO	DIFFIO_B18p		K10				
B4	VREFB4N0	IO	DIFFIO_B18n		L10				
B4	VREFB4N0	IO			P9	64	DQS2B/CQ3B	DQS2B/CQ3B	
B4	VREFB4N0	IO	VREFB4N0		P11	65			
B4	VREFB4N0	IO	DIFFIO_B19p		R13				
B4	VREFB4N0	IO	DIFFIO_B19n		T13		DQ5B	DQ5B	
B4	VREFB4N0	IO	RUP2		M10	66			DQ1B
B4	VREFB4N0	IO	RDN2		N11	67			DQ1B
B4	VREFB4N0	IO	DIFFIO_B20p		T14		DQ5B	DQ5B	
B4	VREFB4N0	IO	DIFFIO_B20n		T15	68	DQS0B/CQ1B,DPCLK3	DQS0B/CQ1B,DPCLK3	DQS0B/CQ1B,DPCLK3

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F256/ U256	E144 (4)	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in E144
B4	VREFB4N0	IO			R14	69			
B4	VREFB4N0	IO	DIFFIO_B21p		P14	70			
B4	VREFB4N0	IO	DIFFIO_B21n		L11	71			
B4	VREFB4N0	IO	DIFFIO_B22p		M11	72			
B4	VREFB4N0	IO	DIFFIO_B22n		N12				
B5	VREFB5N0	IO			N13	73			
B5	VREFB5N0	IO			M12	74			
B5	VREFB5N0	IO			L12	75			
B5	VREFB5N0	IO			K12				
B5	VREFB5N0	IO	RUP3		N14	76	DM1R/BWS#1R		
B5	VREFB5N0	IO	RDN3		P15	77	DQ1R		
B5	VREFB5N0	IO	DIFFIO_R11n		P16		DQS3R/CQ3R#	DQS3R/CQ3R#	DQS3R/CQ3R#
B5	VREFB5N0	IO	DIFFIO_R11p		R16		DQ1R		
B5	VREFB5N0	IO			K11				
B5	VREFB5N0	IO	DIFFIO_R10n		N16		DQ1R		
B5	VREFB5N0	IO	DIFFIO_R10p		N15		DQ1R		
B5	VREFB5N0	IO	VREFB5N0		L14	80			
B5	VREFB5N0	IO			L13		DQ1R		
B5	VREFB5N0	IO	DIFFIO_R9n		L16		DQ1R		
B5	VREFB5N0	IO	DIFFIO_R9p		L15				
B5	VREFB5N0	IO			J11	83			
B5	VREFB5N0	IO	DIFFIO_R8n		K16	84	DQ1R		
B5	VREFB5N0	IO	DIFFIO_R8p		K15	85	DQS1R/CQ1R#,DPCLK4	DQS1R/CQ1R#,DPCLK4	DQS1R/CQ1R#,DPCLK4
B5	VREFB5N0	IO	DIFFIO_R7n	DEV_OE	J16	86			
B5	VREFB5N0	IO	DIFFIO_R7p	DEV_CLRn	J15	87			
B5	VREFB5N0	IO	DIFFIO_R6n		J14		DQ1R		
B5	VREFB5N0	IO	DIFFIO_R6p		J12				
B5	VREFB5N0	IO			J13		DQ1R		
B5	VREFB5N0	CLK7	DIFFCLK_3n		M16	88			
B5	VREFB5N0	CLK6	DIFFCLK_3p		M15	89			
B6	VREFB6N0	CLK5	DIFFCLK_2n		E16	90			
B6	VREFB6N0	CLK4	DIFFCLK_2p		E15	91			
B6	VREFB6N0	CONF_DONE		CONF_DONE	H14	92			
B6	VREFB6N0	MSEL0		MSEL0	H13	94			
B6	VREFB6N0	MSEL1		MSEL1	H12	96			
B6	VREFB6N0	MSEL2		MSEL2	G12	97			
B6	VREFB6N0	IO	DIFFIO_R4n	INIT_DONE	G16	98			
B6	VREFB6N0	IO	DIFFIO_R4p	CRC_ERROR	G15	99			
B6	VREFB6N0	IO			F13	100			
B6	VREFB6N0	IO	DIFFIO_R3n	nCEO	F16	101			
B6	VREFB6N0	IO	DIFFIO_R3p	CLKUSR	F15	103			
B6	VREFB6N0	IO			B16	104	DQS0R/CQ1R,DPCLK5	DQS0R/CQ1R,DPCLK5	DQS0R/CQ1R,DPCLK5
B6	VREFB6N0	IO	VREFB6N0		F14	105			
B6	VREFB6N0	IO	DIFFIO_R2n		D16				
B6	VREFB6N0	IO	DIFFIO_R2p		D15				
B6	VREFB6N0	IO			G11				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F256/U256	E144 (4)	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in E144
B6	VREFB6N0	IO	DIFFIO_R1n		C16	106	DQS2R/CQ3R	DQS2R/CQ3R	
B6	VREFB6N0	IO	DIFFIO_R1p		C15				
B7	VREFB7N0	IO	DIFFIO_T21n		C14				
B7	VREFB7N0	IO	DIFFIO_T21p		D14		DQ5T	DQ5T	
B7	VREFB7N0	IO	DIFFIO_T20n		D11				
B7	VREFB7N0	IO	DIFFIO_T20p		D12	110	DQS0T/CQ1T,DPCLK6	DQS0T/CQ1T,DPCLK6	DQS0T/CQ1T,DPCLK6
B7	VREFB7N0	IO	DIFFIO_T19n		A13				
B7	VREFB7N0	IO	DIFFIO_T19p		B13	111	DQ5T	DQ5T	
B7	VREFB7N0	IO	PLL2_CLKOUTn		A14	112			
B7	VREFB7N0	IO	PLL2_CLKOUTp		B14	113			
B7	VREFB7N0	IO	RUP4		E11	114			DQ1T
B7	VREFB7N0	IO	RDN4		E10	115			DQ1T
B7	VREFB7N0	IO	DIFFIO_T18n		A12		DQ5T	DQ5T	
B7	VREFB7N0	IO	DIFFIO_T18p		B12		DQ5T	DQ5T	
B7	VREFB7N0	IO	DIFFIO_T17n		A11		DQ5T	DQ5T	
B7	VREFB7N0	IO	DIFFIO_T17p		B11		DQ5T	DQ5T	
B7	VREFB7N0	IO	VREFB7N0		C11	119			
B7	VREFB7N0	IO	DIFFIO_T16n		F10	120			DQ1T
B7	VREFB7N0	IO	DIFFIO_T16p		F9	121	DQS2T/CQ3T	DQS2T/CQ3T	
B7	VREFB7N0	IO	DIFFIO_T15n		F11				
B7	VREFB7N0	IO	DIFFIO_T15p		A15				
B7	VREFB7N0	IO	DIFFIO_T14n		A10		DQ5T	DQ5T	
B7	VREFB7N0	IO	DIFFIO_T14p		B10		DQ5T	DQ5T	
B7	VREFB7N0	IO	DIFFIO_T13n		C9		DQ5T	DQ5T	
B7	VREFB7N0	IO	DIFFIO_T13p		D9	124	DM5T/BWS#5T	DM5T/BWS#5T	
B7	VREFB7N0	IO			E9	125	DQS4T/CQ5T	DQS4T/CQ5T	
B7	VREFB7N0	IO	DIFFIO_T12n		A9	126			
B7	VREFB7N0	IO	DIFFIO_T12p		B9	127			
B8	VREFB8N0	IO	DIFFIO_T11n		A8	128			
B8	VREFB8N0	IO	DIFFIO_T11p		B8	129			
B8	VREFB8N0	IO			C8		DQS5T/CQ5T#	DQS5T/CQ5T#	DQS5T/CQ5T#
B8	VREFB8N0	IO			D8		DQ3T	DQ5T	
B8	VREFB8N0	IO	DIFFIO_T10n	DATA2	E8	132	DQ3T	DQ5T	DQ1T
B8	VREFB8N0	IO	DIFFIO_T10p	DATA3	F8	133			DQ1T
B8	VREFB8N0	IO	DIFFIO_T9n		A7		DQ3T	DQ5T	
B8	VREFB8N0	IO	DIFFIO_T9p	DATA4	B7		DQ3T	DQ5T	
B8	VREFB8N0	IO	DIFFIO_T8n		F6	135			DQ1T
B8	VREFB8N0	IO	DIFFIO_T8p		F7				
B8	VREFB8N0	IO	VREFB8N0		C6	136			
B8	VREFB8N0	IO	DIFFIO_T7n		A6		DQS3T/CQ3T#	DQS3T/CQ3T#	DQS3T/CQ3T#
B8	VREFB8N0	IO	DIFFIO_T7p		B6		DQ3T	DQ5T	
B8	VREFB8N0	IO		DATA5	E7	137	DQ3T	DQ5T	DQ1T
B8	VREFB8N0	IO		DATA6	E6	138	DQ3T	DQ5T	
B8	VREFB8N0	IO	DIFFIO_T6n	DATA7	A5		DQ3T	DQ5T	
B8	VREFB8N0	IO	DIFFIO_T5n		A2				
B8	VREFB8N0	IO	DIFFIO_T5p		B5	141	DQ3T	DQ5T	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F256/ U256	E144 (4)	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in E144
B8	VREFB8N0	IO	DIFFIO_T4n		A4		DM3T/BWS#3T	DM5T/BWS#5T	
B8	VREFB8N0	IO	DIFFIO_T4p		B4				
B8	VREFB8N0	IO	DIFFIO_T3n		D5				
B8	VREFB8N0	IO	DIFFIO_T3p		D6				
B8	VREFB8N0	IO	DIFFIO_T2n		A3				
B8	VREFB8N0	IO	DIFFIO_T2p		B3	142	DQS1T/CQ1T#,DPCLK7	DQS1T/CQ1T#,DPCLK7	DQS1T/CQ1T#,DPCLK7
B8	VREFB8N0	IO	DIFFIO_T1n		C3	143			DQ1T
B8	VREFB8N0	IO	DIFFIO_T1p		D3	144			DM1T
		GND			H7	19			
		GND			H8	27			
		GND			H9	41			
		GND			H10	48			
		GND			J7	57			
		GND			J8	63			
		GND			J9	82			
		GND			J10	95			
		GND			B2	118			
		GND			B15	123			
		GND			C5	131			
		GND			C12	140			
		GND			D7	4			
		GND			D10	22			
		GND			E4	79			
		GND			E13				
		GND			G4				
		GND			G13				
		GND			K4				
		GND			K13				
		GND			M4				
		GND			M13				
		GND			N7				
		GND			N10				
		GND			P5				
		GND			P12				
		GND			R2				
		GND			R15				
		GND			E2				
		GND			H16				
		GND			H15				
		GNDA1			M5	36			
		GNDA2			E12	108			
		VCCINT			G6	5			
		VCCINT			G7	29			
		VCCINT			G8	45			
		VCCINT			G9	61			
		VCCINT			G10	78			
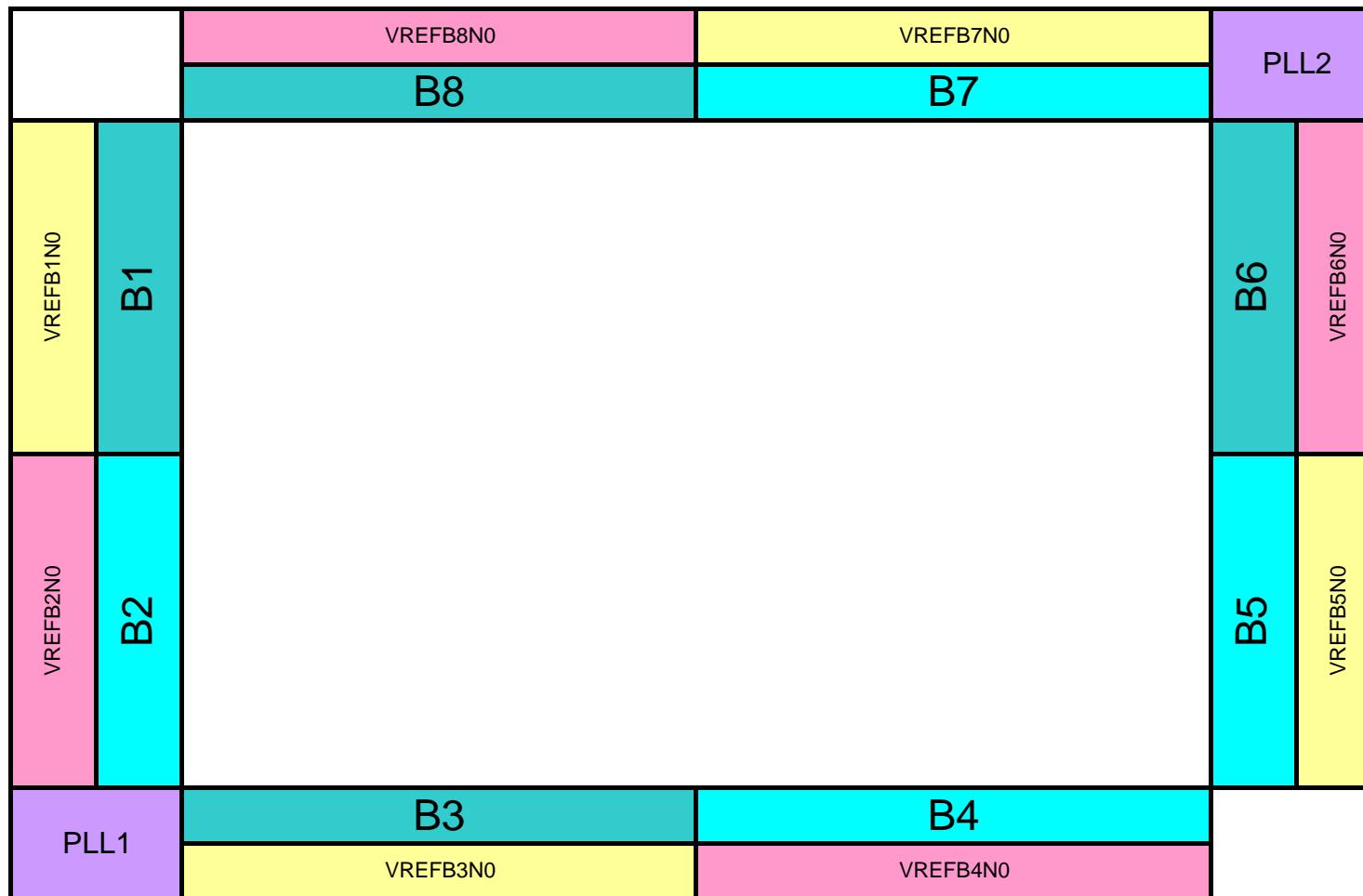
Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F256/ U256	E144 (4)	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in E144
		VCCINT			H6	102			
		VCCINT			H11	116			
		VCCINT			K7	134			
		VCCIO1			E3	17			
		VCCIO1			G3				
		VCCIO2			K3	26			
		VCCIO2			M3				
		VCCIO3			P4	40			
		VCCIO3			P7	47			
		VCCIO3			T1				
		VCCIO4			P10	56			
		VCCIO4			P13	62			
		VCCIO4			T16				
		VCCIO5			K14	81			
		VCCIO5			M14				
		VCCIO6			E14	93			
		VCCIO6			G14				
		VCCIO7			A16	117			
		VCCIO7			C10	122			
		VCCIO7			C13				
		VCCIO8			A1	130			
		VCCIO8			C4	139			
		VCCIO8			C7				
		VCCA1			L5	35			
		VCCA2			F12	107			
		VCCD_PLL1			N4	37			
		VCCD_PLL2			D13	109			

Notes:

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For DQS pins that do not have the associated DQ pins, the particular DQS is not supported.

(3) For more information about pin definition and pin connection guidelines, refer to the
Cyclone IV Device Family Pin Connection Guidelines.

(4) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. This exposed pad is used for electrical connectivity, and not for thermal purposes.

ALTERA

	VREFB8N0	VREFB7N0	PLL2
	B8	B7	

VREFB1N0	B1		B6	VREFB6N0
VREFB2N0	B2		B5	VREFB5N0

PLL1	B3	B4	
	VREFB3N0	VREFB4N0	

Notes:

1. This is a top view of the silicon die.

2. This is only a pictorial representation to provide an idea of placement on the device. For exact locations, refer to the pin list and the Quartus® II software.

Version Number	Date	Changes made
1.0	1/25/2010	Initial Release.
1.1	12/6/2010	Added UBGA package support.
1.2	6/10/2011	Removed Pin Definitions sheet.