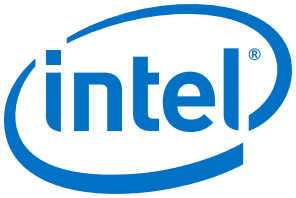


Intel® Cyclone® 10 GX Device Family Pin Connection Guidelines

Subscribe
Send Feedback

PCG-01022 | 2019.07.01
Latest document on the web: PDF | HTML

Contents

PCG-01022 | 2019.07.01

Send Feedback

Intel® Cyclone® 10 GX Device Family Pin Connection Guidelines

Disclaimer

These pin connection guidelines, and your use thereof, are subject to and governed by Intel's terms and conditions below. By using these pin connection guidelines, you indicate your acceptance of all such terms and conditions. If you do not agree with such terms and conditions, you may not use the pin connection guidelines, and you are required to promptly and irrevocably destroy the pin connection guidelines and any copies or portions thereof in your possession or under your control.

Terms and Conditions:

1. These pin connection guidelines are provided as examples only, and should not be deemed to be technical specifications or recommendations. The use of the pin connection guidelines for any particular design should be verified for device operation with the applicable datasheet and Intel.
2. Subject to these terms and conditions, Intel grants to you the use of these pin connection guidelines as examples of possible pin connections of an Intel programmable logic device-based design. You may not use these pin connection guidelines for any other purpose except as expressly permitted in these terms and conditions. Intel does not recommend, suggest, or require that these pin connection guidelines be used in conjunction or combination with any other software or product, and makes no representations, warranties or guaranties, implied or express as well as any warranties arising from course of performance, course of dealing, or usage in trade including but not limited to the accuracy, completeness or genuineness thereof.
3. Intel will not be liable for any lost revenue, lost profits, or other consequential, indirect, or special damages caused by your use of these pin connection guidelines even if advised of the possibility of such damages occurring.
4. This agreement shall be governed in all respects by the laws of the State of Delaware, without regard to conflict of law or choice of law principles. You agree to submit to the exclusive jurisdiction of the federal and state courts in the State of Delaware for the resolution of any dispute or claim arising out of or relating to these terms of use.

Intel® Cyclone® 10 GX Pin Connection Guidelines

Clock and PLL Pins

Note: Intel® recommends that you create an Intel Quartus® Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 1. Clock and PLL Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK_[2,3] [A,B,J,K,L]_[0,1]p	I/O, Clock Input	Dedicated high speed clock input pins that can be used for data inputs or outputs. Differential input OCT R_D, single-ended input OCT R_T, and single-ended output OCT R_S are supported on these pins.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
CLK_[2,3] [A,B,J,K,L]_[0,1]n	I/O, Clock Input	Dedicated high speed clock input pins that can be used for data inputs or outputs. Differential input OCT R_D, single-ended input OCT R_T, and single-ended output OCT R_S are supported on these pins.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[2,3] [A,B,J,K,L]_FB[0,1]	I/O, Clock	Dual-purpose I/O pins that can be used as single-ended inputs, single-ended outputs, or external feedback input pin. For more information about the supported pins, refer to the device pinout file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[2,3] [A,B,J,K,L]_CLKOUT[0:1], PLL_[2,3] [A,B,J,K,L]_CLKOUT[0:1]p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair. For more information about the supported pins, refer to the device pinout file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[2,3] [A,B,J,K,L]_CLKOUT[0:1]n	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair. For more information about the supported pins, refer to the device pinout file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.

Dedicated Configuration/JTAG Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 2. Dedicated Configuration/JTAG Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
nIO_PULLUP	Input	Dedicated input pin that determines the internal pull-ups on user I/O pins and dual-purpose I/O pins (DATA[0:31], CLKUSR, INIT_DONE, DEV_OE, and DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns on the weak pull-up.	Tie the nIO-PULLUP pin directly to VCC using a 1 kΩ pull-up resistor, or directly to GND. This pin has an internal 25-kΩ pull-down. If you tie this pin to VCC, ensure all user I/O pins and dual-purpose I/O pins are at logic–0 before and during configuration.
TEMPDIODEp	Input	Pin used for temperature sensing diode (bias-high input) inside the FPGA.	If you do not use the temperature sensing diode with an external temperature sensing device, connect this pin to GND.
TEMPDIODEn	Input	Pin used for temperature sensing diode (bias-low input) inside the FPGA.	If you do not use the temperature sensing diode with an external temperature sensing device, connect this pin to GND.
MSEL[0:2]	Input	Configuration input pins that set the configuration scheme for the FPGA device.	These pins are internally connected through a 25-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused, connect them to GND. Depending on the configuration scheme used, tie these pins to VCCPGM or GND. For more information about the configuration scheme options, refer to the *Configuration, Design Security, and Remote System Upgrades for Intel Cyclone® 10 GX Devices* chapter. If you use JTAG configuration scheme, connect these pins to GND.
nCE	Input	Dedicated active-low chip enable pin. When the nCE pin is low, the device is enabled. When the nCE pin is high, the device is disabled.	In multi-device configuration, the nCE pin of the first device is tied low while its nCEO pin drives the nCE pin of the next device in the chain. In single-device configuration and JTAG programming, connect the nCE pin to GND.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
nCONFIG	Input	Dedicated configuration control input pin. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level initiates reconfiguration.	Connect the nCONFIG pin directly to the configuration controller when the FPGA uses a passive configuration scheme. Connect the nCONFIG pin through a 10-kΩ resistor tied to VCCPGM when the FPGA uses an active serial (AS) configuration scheme. If you do not use this pin, connect the pin directly or through a 10-kΩ resistor to VCCPGM.
CONF_DONE	Bidirectional (open-drain)	Dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, the CONF_DONE pin goes high after all data is received. Then the device initializes and enters user mode. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistors to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host. When you use passive configuration schemes, the configuration controller monitors this pin.
nCEO	I/O, Output (open-drain)	When device configuration is complete, the nCEO pin drives low. If you do not use this pin as a configuration pin, you can use this pin as a user I/O pin.	In multi-device configuration, the nCEO pin feeds the nCE pin of a subsequent FPGA. Connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. In single-device configuration, you can leave this pin floating.
nSTATUS	Bidirectional (open-drain)	Dedicated configuration status pin. The FPGA drives the nSTATUS pin low immediately after power-up, and releases the pin after power-on reset (POR) time. As a status output, the nSTATUS pin is pulled low if an error occurs during configuration. As a status input, the device enters an error state when the nSTATUS pin is driven low by an external source during configuration or initialization. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistors to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host. When you use passive configuration schemes, the configuration controller monitors this pin.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin through a 1-kΩ pull-down resistor to GND. This pin has an internal 25-kΩ pull-down. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TCK pin. The TCK input pin is powered by the VCCPGM supply.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin through a 1–10-kΩ pull-up resistor to VCCPGM.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			If the JTAG interface is not used, connect the TMS pin to VCCPGM using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TMS pin. The TMS input pin is powered by the VCCPGM supply.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin through a 1–10-kΩ pull-up resistor to VCCPGM. If the JTAG interface is not used, connect the TDI pin to VCCPGM using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TDI pin. The TDI input pin is powered by the VCCPGM supply.
TDO	Output	Dedicated JTAG test data output pin.	If the JTAG interface is not used, leave the TDO pin unconnected.
TRST	Input	Dedicated active low JTAG test reset input pin. The TRST pin is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of the TRST pin is optional. If you do not use this pin, tie this pin through a 1-kΩ pull-up resistor to VCCPGM. When you use this pin, ensure that the TMS pin is held high or the TCK pin is static when the TRST pin is changing from low to high. To disable the JTAG circuitry, tie this pin to GND. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TRST pin. The TRST input pin is powered by the VCCPGM supply.
nCSO[0:2]	Output	Dedicated output control signal from the FPGA to the EPCQ-L device in AS configuration scheme that enables the EPCQ-L device.	When you are not programming the FPGA in the AS configuration scheme, the nCSO pin is not used. When you do not use this pin as an output pin, leave this pin unconnected.

Optional/Dual-Purpose Configuration Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 3. Optional/Dual-Purpose Configuration Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DCLK	Input (PS, FPP); Output (AS)	Dedicated configuration clock pin. In passive serial (PS) and fast passive parallel (FPP) configuration schemes, DCLK is used to clock configuration data from an external source into the FPGA. In the AS configuration scheme, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	I/O, Output (open-drain)	Active high signal indicates the error detection circuit has detected errors in the configuration RAM (CRAM) bits. Falling edge of this signal indicates the information about the error location and type are available in the error message register (EMR). This dual-purpose pin is only used when you enable error detection in user mode. This pin can be used as a user I/O pin.	When you use the open-drain output dedicated CRC_ERROR pin as an optional pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the open-drain output dual-purpose CRC_ERROR pin as an optional pin, and the CRC_ERROR pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared. When this pin is driven high (VCCPGM), all registers behave as programmed.	When you do not use the dual-purpose DEV_CLRn pin and when this pin is not used as an I/O pin, tie this pin to GND.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated. When this pin is driven high (VCCPGM), all I/O pins behave as programmed.	When you do not use the dual-purpose DEV_OE pin and when this pin is not used as an I/O pin, tie this pin to GND.
DATA0	I/O, Input	Dual-purpose configuration data input pin. You can use the DATA0 pin for PS or FPP configuration scheme, or as an I/O pin after configuration is complete.	When you do not use the dedicated input DATA0 pin and when this pin is not used as an I/O pin, leave this pin unconnected.
DATA[1:31]	I/O, Input	Dual-purpose configuration data input pins. Use DATA [1:7] pins for FPP x8, DATA [1:15] pins for FPP x16, and DATA [1:31] pins for FPP x32 configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When you do not use the dual-purpose DATA[1:31] pins and when these pins are not used as I/O pins, leave these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as the INIT_DONE pin.	When you use the optionally open-drain output dedicated INIT_DONE pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
		When you enable this pin, a transition from low to high at the pin indicates the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When you use this pin in an AS or PS multi-device configuration mode, ensure you enable the INIT_DONE pin in the Intel Quartus Prime designs. When you do not use the dedicated INIT_DONE optionally open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.
nPERSTL0	I/O, Input	Dual-purpose fundamental reset pin that is only available when you use together with PCI Express® (PCIe®) hard IP (HIP). When the pin is low, the transceivers are in reset. When the pin is high, the transceivers are out of reset. When you do not use this pin as the fundamental reset, you can use this pin as a user I/O pin.	Connect this pin as defined in the Intel Quartus Prime software. This pin is powered by 1.8V VCCIO supply and must be driven by 1.8V compatible I/O standards. When this pin is not used for configuration purpose, you have the option to select 1.2V, 1.5V, or 1.8V compatible I/O standard. However, you must shift down the 3.3V LVTTL voltage from the PCIe nPERST pin to the selected Intel Cyclone 10 GX nPERST I/O standard voltage level.
AS_DATA0/ASDO	Bidirectional	Dedicated AS configuration pin. When using an EPCQ-L device (x1 mode), this is the ASDO pin and is used to send address and control signals between the FPGA device and the EPCQ-L device.	When you do not program the device in the AS configuration mode, the ASDO pin is not used. When you do not use this pin, leave the pin unconnected.
AS_DATA[1:3]	Bidirectional	Dedicated AS configuration data pins. Configuration data is transported on these pins when connected to the EPCQ-L devices.	When you do not use this pin, leave the pin unconnected.

Differential I/O Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 4. Differential I/O Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
LVDS[2,3][A,B,J,K,L]_[1:24]p, LVDS[2,3][A,B,J,K,L]_[1:24]n	I/O, TX/RX channel	These are true LVDS receiver/transmitter channels on column I/O banks. Each I/O pair can be configured as LVDS receiver or LVDS transmitter. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix	Connect unused pins as defined in the Intel Quartus Prime software.

Pin Name	Pin Functions	Pin Description	Connection Guidelines
		carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	

External Memory Interface Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 5. External Memory Interface Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQS[#]	I/O,bi-directional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.
DQSn[#]	I/O,bi-directional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.
DQ[#]	I/O,bi-directional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan on migrating to a different memory interface that has a different DQ bus width, you will need to reevaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Intel Quartus Prime software.
DQS[#]_[#]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in the Intel Quartus Prime software.
DQSn[#]_[#]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQ[#]_[#]_[#]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan on migrating to a different memory interface that has a different DQ bus width, you will need to reevaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Intel Quartus Prime software.
DM[#]_[#]	I/O, Output	Optional write data mask, edge-aligned to DQ during write.	Connect unused pins as defined in the Intel Quartus Prime software.
RESET_N_0	I/O, Output	Active low reset signal.	Connect unused pins as defined in the Intel Quartus Prime software.
A_[#]	I/O, Output	Address input for DDR3 SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.
BA_[#]	I/O, Output	Bank address input for DDR3 SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.
CK_[#]	I/O, Output	Input clock for external memory devices.	Connect unused pins as defined in the Intel Quartus Prime software.
CK_N_[#]	I/O, Output	Input clock for external memory devices, inverted CK.	Connect unused pins as defined in the Intel Quartus Prime software.
CKE_[#]	I/O, Output	High signal enables clock, low signal disables clock.	Connect unused pins as defined in the Intel Quartus Prime software.
CS_N_[#]	I/O, Output	Active low chip select.	Connect unused pins as defined in the Intel Quartus Prime software.
CA_[#]_[#]	I/O, Output	Command and address input for LPDDR3 SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.
ODT_[#]	I/O, Output	On die termination signal to set the termination resistors to each pin.	Connect unused pins as defined in the Intel Quartus Prime software.
WE_N_0	I/O, Output	Write-enable input for DDR3 SDRAM and all supported protocols.	Connect unused pins as defined in the Intel Quartus Prime software.
CAS_N_0	I/O, Output	Column address strobe for DDR3 SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.
RAS_N_0	I/O, Output	Row address strobe for DDR3 SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
ALERT_N_0	I/O, Input	Alert input that indicate to the system's memory controller that a specific alert or event has occurred.	Connect unused pins as defined in the Intel Quartus Prime software.
PAR_0	I/O, Output	Command and Address Parity Output.	Connect unused pins as defined in the Intel Quartus Prime software.
CFG_N_0	I/O, Output	Configuration bit.	Connect unused pins as defined in the Intel Quartus Prime software.
LBK[#]_N_0	I/O, Output	Loop-back mode.	Connect unused pins as defined in the Intel Quartus Prime software.

Voltage Sensor Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 6. Voltage Sensor Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VREFP_ADC	Input	Dedicated precision analog voltage reference.	Tie VREFP_ADC to an external 1.25V accurate reference source (+/- 0.2%) for better ADC performance. Treat VREFP_ADC as an analog signal that together with the VREFN_ADC signal provides a differential 1.25V voltage. If no external reference is supplied, always connect VREFP_ADC to GND. An on-chip reference source (+/-10%) is activated by connecting this pin to GND. VREFP_ADC must be equal to or lower than VCCA_PLL to prevent damage.
VREFN_ADC	Input		Tie VREFN_ADC to the GND pin of an external 1.25V accurate reference source (+/- 0.2%) for better ADC performance. Treat VREFN_ADC as an analog signal that together with the

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			VREFP_ADC signal provides a differential 1.25V voltage. If no external reference is supplied, always connect VREFN_ADC to GND.
VSIGP_[0,1]	Input	2 pairs of analog differential inputs pins used with the voltage sensor inside the FPGA to monitor external analog voltages.	Tie these pins to GND of the voltage sensor feature if not used. For details on the usage of these pins, refer to the *Power Management in Intel Cyclone 10 GX Devices* chapter. Do not drive VSIGP and VSIGN pins until the VCCA_PLL power rail has reached 1.62V to prevent damage.
VSIGN_[0,1]	Input		

Reference Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 7. Reference Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RZQ_[#]	I/O	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. Connect the external precision resistor to the designated pin within the bank. If not required, this pin is a regular I/O pin.	When using OCT tie these pins to GND through either a 240-Ω or 100-Ω resistor, depending on the desired OCT impedance. Refer to the *Intel Cyclone 10 GX Device Handbook* for the OCT impedance options for the desired OCT scheme.
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, GND, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration, you have the option to connect these pins to either power, GND, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.

Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 8. Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCP	Power	VCCP supplies power to the periphery.	VCC, VCCP, and VCCERAM must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. Connect VCCP pins to a 0.9V supply. For more information about the performance and power consumption, refer to the Intel Quartus Prime software timing reports and Intel Cyclone 10 GX Early Power Estimator (EPE). For details about the recommended operating conditions, refer to the Electrical Characteristics in the device datasheet. Use the Intel Cyclone 10 GX Early Power Estimator (EPE) to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board. See Notes 2, 3, 4, 5, 6, and 10.
VCC	Power	VCC supplies power to the core. VCC also supplies power to the Hard IP for PCI Express cores.	VCC, VCCP, and VCCERAM must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. Connect VCC pins to a 0.9V supply. For more information about the performance and power consumption, refer to the Intel Quartus Prime software timing reports and Intel Cyclone 10 GX Early Power Estimator (EPE). For details about the recommended operating conditions, refer to the Electrical Characteristics in the device datasheet. Use the Intel Cyclone 10 GX Early Power Estimator (EPE) to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board. See Notes 2, 3, 4, 5, 6, and 10.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCPT	Power	Power supply for the programmable power technology and I/O pre-drivers.	Connect VCCPT to a 1.8V low noise switching regulator. You have the option to source the following from the same regulator as VCCPT: • VCCH_GXB and VCCA_PLL with proper isolation filtering • VCCBAT if it is using the same voltage level and the design security key feature is not required Provide a minimum decoupling of 1uF for the VCCPT power rail near the VCCPT pin. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Cyclone 10 GX Devices*. See Notes 2, 3, 4, 7, and 10.
VCCA_PLL	Power	PLL analog power.	Connect VCCA_PLL to a 1.8V low noise switching regulator. With proper isolation filtering, you have the option to source VCCA_PLL from the same regulator as VCCPT. See Notes 2, 3, 4, 7, and 10.
VCCIO([2][A,J,K,L], [3][A,B])	Power	These are I/O supply voltage pins for banks 1 through 12. Each bank can support a different voltage level. Supports VCCIO standards that include Diff HSTL/HSTL(12, 15, 18), Diff SSTL/SSTL(12, 125, 135, 15, 18), Diff HSUL/HSUL(12), Diff POD 12, LVDS/Mini_LVDS/RSDS, 1.2V, 1.5V, 1.8V, 2.5V, 3.0V I/O standards.	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, or 3.0V supplies, depending on the I/O standard required by the specified bank. When these pins require the same voltage level as VCCPGM, you have the option to tie them to the same regulator as VCCPGM. Not all I/O banks support 2.5V or 3.0V supplies. For more details, refer to the *I/O and High Speed I/O in Intel Cyclone 10 GX Devices*. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Cyclone 10 GX Devices*. See Notes 2, 3, 4, 8, and 10.
VCCPGM	Power	Configuration pins power supply.	Connect these pins to a 1.2V, 1.5V, or 1.8V power supply. When dual-purpose configuration pins are used for configuration, tie VCCIO of the bank to the same regulator as VCCPGM, ranging from 1.2V, 1.5V, or 1.8V. When you do not use dual-purpose configuration pins for configuration, connect VCCIO to 1.2V, 1.25V, 1.35V, 1.5V, or 1.8V. When these pins require the same voltage level as VCCIO, you have the option to tie them to the same regulator as VCCIO. Provide a minimum decoupling of 47nF for the VCCPGM power rail near the VCCPGM pin. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Cyclone 10 GX Devices*.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			See Notes 2, 3, 4, and 10.
VCCERAM	Power	Memory power pins.	Connect all VCCERAM pins to a 0.9V linear or low noise switching power supply. VCC, VCCP, and VCCERAM must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. See Notes 2, 3, 7, and 10.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	When using the design security volatile key, connect this pin to a non-volatile battery power source in the range of 1.2V – 1.8V. When not using the volatile key, tie this pin to a supply ranging from 1.5V to 1.8V. If 1.8V is selected when the design security key is unused, you have the option to source this pin from the same regulator as VCCPT. This pin must be properly powered as per the recommended voltage range as the POR circuitry of the Intel Cyclone 10 GX devices monitoring VCCBAT. Provide a minimum decoupling of 47nF for the VCCBAT power rail near the VCCBAT pin. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Cyclone 10 GX Devices*.
GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.
VREFB[[2][A,J,K,L], [3][A,B]]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then use these pins as voltage-reference pins for the bank.	If VREF pins are not used, connect them to either the VCCIO in the bank in which the pin resides or GND. See Notes 2, 8, 10, and 11.
VCCLSENSE	Power	Differential sense line to external regulator.	VCCLSENSE and GNDSENSE are differential remote sense pins for the VCC power. Connect your regulators' differential remote sense lines to the respective VCCLSENSE and GNDSENSE pins. This compensates for the DC IR drop associated with the PCB and device package from the VCC power. Route these connections as differential pair traces and keep them isolated from any other noise source. Connect VCCLSENSE and GNDSENSE lines to the regulator's remote sense inputs when I_{CC} current >30A.
GNDSENSE	Ground		

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			VCCLSENSE and GNDSENSE line connections are optional if I_{CC} current <=30A. However, Intel recommends connecting the VCCLSENSE and GNDSENSE for regulators that support remote sense line feature. If you do not use the VCCLSENSE and GNDSENSE pins, leave the VCCLSENSE and GNDSENSE pins unconnected.
ADCGND	Ground	Dedicated quiet ground.	If you are using voltage sensor, you must connect ADCGND plane to board GND through a proper isolation filter with ferrite bead. Select the ferrite bead according to the frequency of the noise profile when it shows the maximum noise level. Alternatively, you can choose the ferrite bead based on the ADCGND maximum current value as well, which is 10 mA. If you are not using voltage sensor, isolation filter with ferrite bead to board GND is optional.

Transceiver Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 9. Transceiver Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCR_GXB[L1] [C,D]	Power	Analog power, receiver, specific to each transceiver bank of the left (L) side of the device.	Connect VCCR_GXB pins to a 0.95V or 1.03V low noise switching regulator. All VCCR_GXB of all transceiver banks must be powered on for proper device operation. The VCCR_GXB and VCCT_GXB power supplies voltage level must be equivalent if both power supplies are powered on. See Notes 2, 3, 4, 7, and 10.
VCCT_GXB[L1] [C,D]	Power	Analog power, transmitter, specific to each transceiver bank of the left (L) side of the device.	Connect VCCT_GXB pins to a 0.95V or 1.03V low noise switching regulator.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			If all of the transceivers, fPLLs, and IOPLLs are not used, then the VCCT_GXB power rails can be tied to GND to save power. The VCCR_GXB and VCCT_GXB power supplies voltage level must be equivalent if both power supplies are powered on. To meet DisplayPort TX electrical full compliance, VCCT_GXB must be 1.03V. See Notes 2, 3, 4, 7, and 10.
VCCH_GXB[L]	Power	Analog power, block level transmitter buffers, specific to the left (L) side of the device.	Connect VCCH_GXB to 1.8V low noise switching regulator. With a proper isolation filtering, you have the option to source VCCH_GXB from the same regulator as VCCPT. All VCCH_GXB of all transceiver banks must be powered on for proper device operation. VCCH_GXB pins on the same side of the device must have the same voltage. Provide a minimum decoupling of 2.2nF for the VCCH_GXB power rail near the VCCH_GXB pin. See Notes 2, 3, 4, 7, and 10.
GXB[L1] [C,D]_RX_[0:5]p, GXB[L][1] [C,D]_REFCLK_CH[0:5]p	Input	High speed positive differential receiver channels. Specific to each transceiver bank of the left (L) side of the device.	These pins can be AC-coupled or DC-coupled when used. Connect all unused GXB_RXp pins directly to GND, VCCR_GXB, or VCCT_GXB pins. For DC-coupled support condition, refer to the *Intel Cyclone 10 GX Device Datasheet*.
GXB[L1] [C,D]_RX_[0:5]n, GXB[L][1] [C,D]_REFCLK_CH[0:5]n	Input	High speed negative differential receiver channels. Specific to each transceiver bank of the left (L) side of the device.	These pins can be AC-coupled or DC-coupled when used. Connect all unused GXB_RXn pins directly to GND. For DC-coupled support condition, refer to the *Intel Cyclone 10 GX Device Datasheet*.
GXB[L1] [C,D]_TX_CH[0:5]p	Output	High speed positive differential transmitter channels. Specific to each transceiver bank of the left (L) side of the device.	Leave all unused GXB_TXp pins floating.
GXB[L1] [C,D]_TX_CH[0:5]n	Output	High speed negative differential transmitter channels. Specific to each transceiver bank of the left (L) side of the device.	Leave all unused GXB_TXn pins floating.
REFCLK_GXB[L1] [C,D]_CH[B,T]p	Input	High speed differential reference clock positive receiver channels, specific to each transceiver bank of the left (L) side of the device.	These pins must be AC-coupled if the selected REFCLK I/O standard is not HCSL. In the PCI Express configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is HCSL.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
		REFCLK_GXB can be used as dedicated clock input pins with fPLL for core clock generation even when the transceiver channel is not available.	Connect all unused pins either individually to GND or tie all unused pins together through a single 10-kΩ resistor to GND. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.
REFCLK_GXB[L1] [C,D]_CH[B,T]n	Input	High speed differential reference clock complement, complementary receiver channel, specific to each transceiver bank of the left (L) side of the device. REFCLK_GXB can be used as dedicated clock input pins with fPLL for core clock generation even when the transceiver channel is not available.	These pins must be AC-coupled if the selected REFCLK I/O standard is not HCSL. In the PCI Express configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is HCSL. Connect all unused pins either individually to GND or tie all unused pins together through a single 10-kΩ resistor to GND. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.
CLKUSR	I/O	This pin is used as the clock for transceiver calibration, and is a mandatory requirement when using transceivers. This pin is optionally used for EMIF HMC calibration, as well as a configuration clock input for synchronizing the initialization of more than one device. This is a user-supplied clock and the input frequency range must be in the range from 100 MHz to 125 MHz. This pin can be used as a GPIO pin only if you are not using transceivers, not using EMIF HMC, and not using this pin as a user-supplied configuration clock.	If you are using the CLKUSR pin for configuration and transceiver calibration, you must supply an external free running and stable clock to the CLKUSR pin at start of device configuration and also when the device entered user mode. If the clock is not present at device power-up, transceiver calibration will be delayed until the clock is available. This may impact protocol compliance. You need to ensure supplying the CLKUSR pin with a common clock frequency that is applicable for both the configuration mode and transceiver calibration.
			If you are not using the CLKUSR pin for configuration but using the CLKUSR pin for transceiver calibration, you must supply an external free running and stable clock to the CLKUSR pin at start of device configuration and also when the device entered user mode. If the clock is not present at device power-up, transceiver calibration will be delayed until the clock is available. This may impact protocol compliance.
			If you are using the CLKUSR pin for configuration but not using the CLKUSR pin for transceiver calibration, you must use a user-supplied clock input.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			For more information, refer to the *Configuration, Design Security, and Remote System Upgrades for Intel Cyclone 10 GX GX Devices* chapter.
			Connect the CLKUSR pin to GND if you are not using the CLKUSR pin for any of the following: • Configuration clock input • Transceiver calibration clock • An I/O pin
RREF_[T,B][L]	Input	Reference resistor for fPLL, IOPLL, and transceiver, specific to the top (T) side or bottom (B) side and left (L) side of the device.	If any REFCLK pin or transceiver channel on one side of the device or IOPLL is used, you must connect each RREF pin on that side of the device to its own individual 2kΩ resistor to GND. Otherwise, you can connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Related Information

Intel Cyclone 10 GX Device Datasheet

Notes to Intel Cyclone 10 GX Pin Connection Guidelines

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Cyclone 10 GX device variant.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Then, decouple the power plane using the

appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.

3. Use the Intel Cyclone 10 GX Early Power Estimator (EPE) to determine the current requirements for VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Cyclone 10 GX devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
6. Example 1 and Example 2 illustrate the power supply sharing guidelines for the Intel Cyclone 10 GX devices.
7. Low Noise Switching Regulator—defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response. The switching frequency range is not an Intel requirement. However, Intel does require the Line Regulation and Load Regulation meet the following specifications:
   - Line Regulation < 0.4%
   - Load Regulation < 1.2%
8. The number of modular I/O banks on Intel Cyclone 10 GX devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the *Intel Cyclone 10 GX Device Handbook*.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel subject to the protocol or design requirement. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.
11. Do not connect voltage above 1.8V to the VREFB[[2][A,J,K, L], [3][A,B]]N0 pins. For 3V I/O banks, tie unused VREF pins to GND.

Power Supply Sharing Guidelines for Intel Cyclone 10 GX Devices

Example 1—Intel Cyclone 10 GX

Table 10. Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Example Requiring 3 Power Regulators

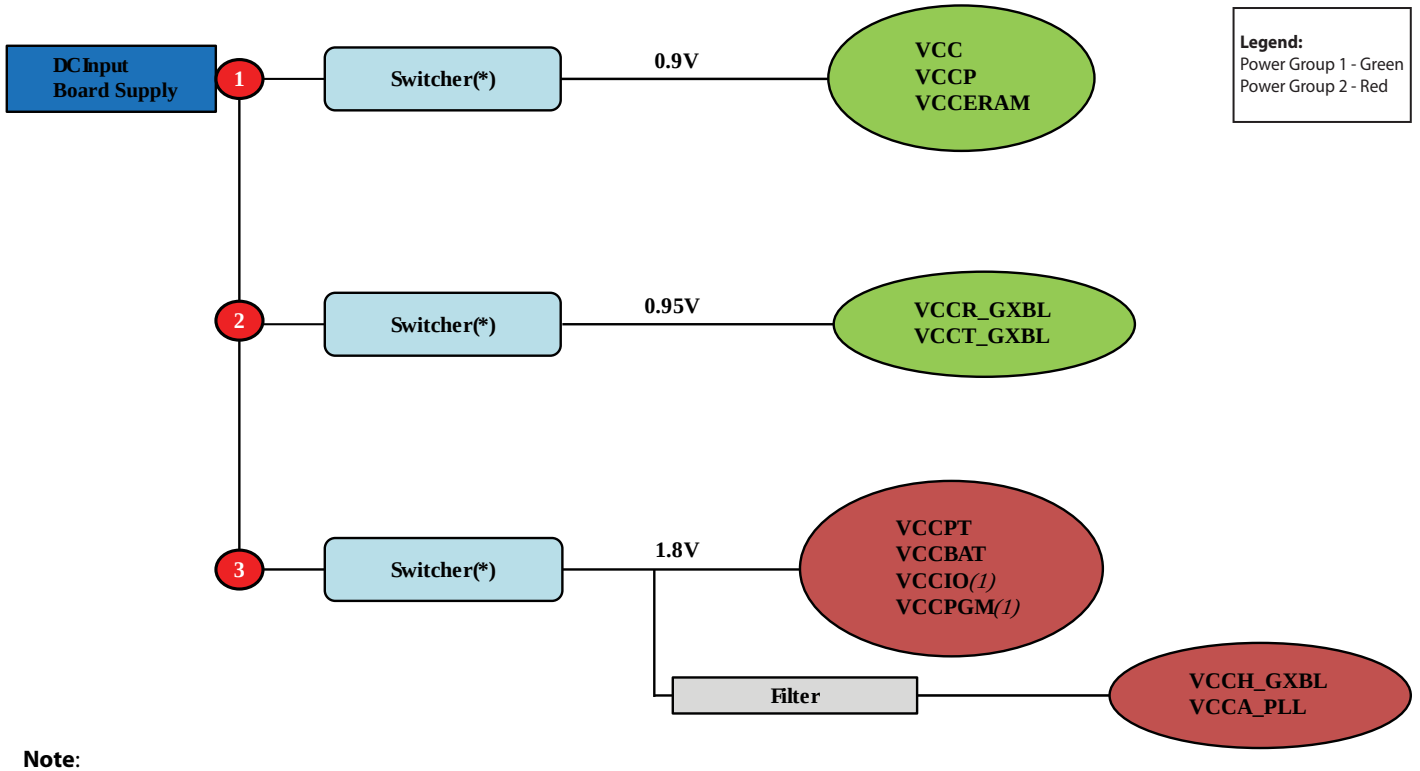
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9	±30 mV	Switcher (*)	Share	—
VCCP						
VCCERAM						
VCCR_GXBL	2	0.95	±30 mV	Switcher (*)	Share	For better performance, isolate VCCR_GXB and VCCT_GXB from each other. To meet DisplayPort TX electrical full compliance, VCCT_GXB must be 1.03V.
VCCT_GXBL						
VCCBAT	3	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails required 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Cyclone 10 GX devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXBL		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Cyclone 10 GX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Cyclone 10 GX Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Cyclone 10 GX device is provided in Figure 1.

Figure 1. Example Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications



Note:
(1) Assumes VCCIO and VCCPGM are 1.8V. Only if these power rails share the same regulator as VCCPT can their power sequence ramp with VCCPT in Group 2. If any of these rails are other than 1.8V, then these rails must be separately regulated and must follow the power sequence requirement in Group 3. For more information about the power sequence requirements, refer to the *Power Management for Intel Cyclone 10 GX Devices*.

Example 2—Intel Cyclone 10 GX

Table 11. Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 12.5 Gbps for Chip-to-Chip Applications (Transceiver Data Rate <= 6.6 Gbps for Backplane Applications)

Example Requiring 3 Power Regulators

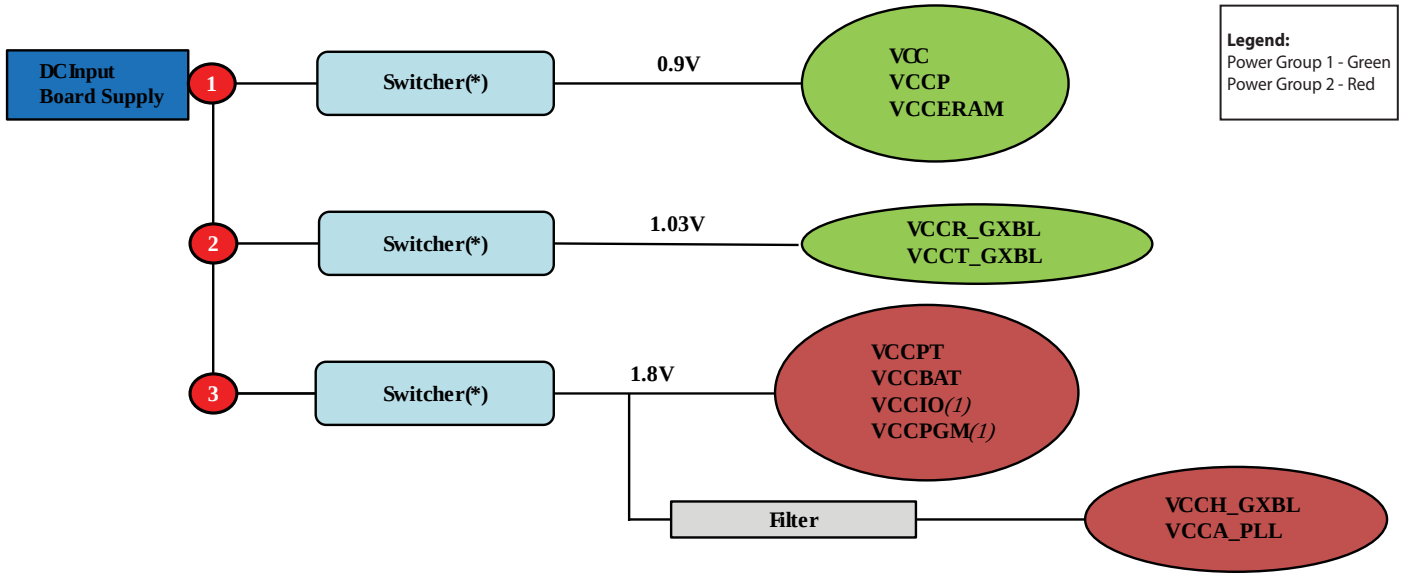
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9	±30 mV	Switcher(*)	Share	—
VCCP						
VCCERAM						
VCCR_GXBL	2	1.03	±30 mV	Switcher(*)	Share	Option provided for VCCR_GXB and VCCT_GXB to share the same regulator. For better performance, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCT_GXBL						
VCCBAT	3	Varies	± 5% (**)	Switcher(*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO and VCCPGM to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Cyclone 10 GX devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXBL		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Cyclone 10 GX Pin Connection Guidelines*.

(**)The supported tolerance for the VCCIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Cyclone 10 GX Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Cyclone 10 GX device is provided in Figure 2.

Figure 2. Example Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 12.5 Gbps for Chip-to-Chip Applications (Transceiver Data Rate <= 6.6 Gbps for Backplane Applications)



Note:

(1) Assumes VCCIO and VCCPGM are 1.8V. Only if these power rails share the same regulator as VCCPT can their power sequence ramp with VCCPT in Group 2. If any of these rails are other than 1.8V, then these rails must be separately regulated and must follow the power sequence requirement in Group 3. For more information about the power sequence requirements, refer to the *Power Management for Intel Cyclone 10 GX Devices*.

Document Revision History for the Intel Cyclone 10 GX Device Family Pin Connection Guidelines

Document Version	Changes
2019.07.01	• Updated the connection guidelines of the TMS and TDI pins to provide more clarity. • Updated the connection guidelines of the INIT_DONE pin to provide more clarity. • Updated the connection guidelines of the VCCBAT pin to provide more clarity. • Updated the connection guidelines of the nPERSTL0 pin. • Updated the connection guidelines of the VCCP and VCC pins. • Updated the connection guidelines of the VCCR_GXB[L1] [C,D] and VCCT_GXB[L1] [C,D] pins. • Updated the connection guidelines of the GXB[L1][C,D]_RX_[0:5]p, GXB[L][1][C,D]_REFCLK_CH[0:5]p, GXB[L1][C,D]_RX_[0:5]n, and GXB[L][1][C,D]_REFCLK_CH[0:5]n pins. • Updated the requirement for VCCT_GXBL pin in the *Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications* section. • Updated the *Example Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications* and *Example Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 12.5 Gbps for Chip-to-Chip Applications (Transceiver Data Rate <= 6.6 Gbps for Backplane Applications)* figures to include grouping legend for the power rails.

Date	Version	Description of Changes
November 2017	2017.11.06	• The document is no longer preliminary. • Added the VCCR_GXB and VCCT_GXB must be powered at the same voltage level guideline in the connection guidelines of the VCCR_GXB[L1] [C,D] and VCCT_GXB[L1] [C,D] pins. • Updated the voltage level supported in the connection guidelines of the VCCR_GXB[L1] [C,D] and VCCT_GXB[L1] [C,D] pins. • Updated the connection guidelines of the VCCIO([2][A,J,K,L], [3][A,B]) pins.
June 2017	2017.06.21	• Added the Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 12.5 Gbps for Chip-to-Chip Applications (Transceiver Data Rate <= 6.6 Gbps for Backplane Applications. • Updated the nPERSTL0 pin name. • Updated the pin function and connection guidelines for RZQ_[#] pins. • Updated the pin function for the CLKUSR pin. • Updated the Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications.

continued...

Date	Version	Description of Changes
		• Updated the Power Supply Sharing Guidelines for Intel Cyclone 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications to include a note for the DisplayPort TX electrical full compliance. • Removed 0.95V support from VCCERAM. • Removed support for partial reconfiguration.
February 2017	2017.02.13	Initial release.