Index within I/O Bank	DDR3 Scheme 1: Component/UDIMM/SODIMM	DDR3 Scheme 2: Component/UDIMM/SODIMM	DDR3 Scheme 3: RDIMM	DDR3 Scheme 4: RDIMM	DDR3 Scheme 5: LRDIMM	LPDDR3 Scheme 1
47			CK_N_1		CK_N_1	
46			CK_1		CK_1	
45	CK_N_3					
44	CK_3					
43	CK_N_2					
42	CK_2					
41	CKE_3		CKE_3			
40	CKE_2		CKE_2			
39	ODT_3		ODT_3		RM_1	
38	ODT_2		ODT_2		RM_0	
37	CS_N_3		CS_N_3		CS_N_3	
36	CS_N_2		CS_N_2		CS_N_2	
35	BA_2	BA_2	BA_2	BA_2	BA_2	CK_N_3
34	BA_1	BA_1	BA_1	BA_1	BA_1	CK_3
33	BA_0	BA_0	BA_0	BA_0	BA_0	CK_N_2
32	CAS_N_0	CAS_N_0	CAS_N_0	CAS_N_0	CAS_N_0	CK_2
31	RAS_N_0	RAS_N_0	RAS_N_0	RAS_N_0	RAS_N_0	
30	A_15	A_15	A_15	A_15	A_15	CKE_3
29	A_14	A_14	A_14	A_14	A_14	CKE_2
28	A_13	A_13	A_13	A_13	A_13	ODT_3
27	A_12	A_12	A_12	A_12	A_12	ODT_2
26						
25						
24						
23	A_11	A_11	A_11	A_11	A_11	
22	A_10	A_10	A_10	A_10	A_10	
21	A_9	A_9	A_9	A_9	A_9	A_9
20	A_8	A_8	A_8	A_8	A_8	A_8
19	A_7	A_7	A_7	A_7	A_7	A_7
18	A_6	A_6	A_6	A_6	A_6	A_6
17	A_5	A_5	A_5	A_5	A_5	A_5
16	A_4	A_4	A_4	A_4	A_4	A_4
15	A_3	A_3	A_3	A_3	A_3	A_3
14	A_2	A_2	A_2	A_2	A_2	A_2
13	A_1	A_1	A_1	A_1	A_1	A_1
12	A_0	A_0	A_0	A_0	A_0	A_0
11	CK_N_1	CK_N_1	PAR_0	PAR_0	PAR_0	CK_N_1
10	CK_1	CK_1	ALERT_N_0	ALERT_N_0	ALERT_N_0	CK_1
9	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0
8	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0
7	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1
6	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0
5	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1
4	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0
3	CS_N_1	CS_N_1	CS_N_1	CS_N_1	CS_N_1	CS_N_1
2	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0
1	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	CS_N_3
0	WE_N_0	WE_N_0	WE_N_0	WE_N_0	WE_N_0	CS_N_2

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April 2017	2017.04.20	Initial release.

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