Pin Information for the Intel® Cyclone®10 10CL120 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B1	VREFB1N0	IO			DIFFIO_L1p	H7
B1	VREFB1N0	IO			DIFFIO_L1n	G3
B1	VREFB1N0	IO			DIFFIO_L2p	B2
B1	VREFB1N0	IO			DIFFIO_L2n	B1
B1	VREFB1N0	IO	VREFB1N0			G5
B1	VREFB1N0	IO			DIFFIO_L3p	E4
B1	VREFB1N0	IO			DIFFIO_L3n	E3
B1	VREFB1N0	IO			DIFFIO_L5p	D2
B1	VREFB1N0	IO		DATA1,ASDO	DIFFIO_L5n	D1
B1	VREFB1N0	IO			DIFFIO_L6p	H6
B1	VREFB1N0	IO			DIFFIO_L6n	J6
B1	VREFB1N0	IO			DIFFIO_L7n	H3
B1	VREFB1N0	IO		FLASH_nCE,nCSO	DIFFIO_L8p	E2
B1	VREFB1N0	IO			DIFFIO_L8n	E1
B1	VREFB1N1	IO			DIFFIO_L9p	F2
B1	VREFB1N1	IO			DIFFIO_L9n	F1
B1	VREFB1N1	IO				H4
B1	VREFB1N1	IO	VREFB1N1			H5
B1	VREFB1N1	nSTATUS		nSTATUS		K6
B1	VREFB1N1	IO	DPCLK0		DIFFIO_L12p	J4
B1	VREFB1N1	IO			DIFFIO_L13p	H2
B1	VREFB1N1	IO			DIFFIO_L13n	H1
B1	VREFB1N2	IO	VREFB1N2			J3
B1	VREFB1N2	IO			DIFFIO_L23p	J2
B1	VREFB1N2	IO			DIFFIO_L23n	J1
B1	VREFB1N2	IO		DCLK		K2
B1	VREFB1N2	IO		DATA0		K1
B1	VREFB1N2	nCONFIG		nCONFIG		K5
B1	VREFB1N2	TDI		TDI		L5
B1	VREFB1N2	TCK		TCK		L2
B1	VREFB1N2	TMS		TMS		L1
B1	VREFB1N2	TDO		TDO		L4
B1	VREFB1N2	nCE		nCE		L3
B1	VREFB1N2	CLK0	DIFFCLK_0p			G2
B1	VREFB1N2	CLK1	DIFFCLK_0n			G1
B2	VREFB2N0	CLK2	DIFFCLK_1p			T2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B2	VREFB2N0	CLK3	DIFFCLK_1n			T1
B2	VREFB2N0	IO			DIFFIO_L25p	L6
B2	VREFB2N0	IO			DIFFIO_L25n	M6
B2	VREFB2N0	IO			DIFFIO_L27p	M2
B2	VREFB2N0	IO			DIFFIO_L27n	M1
B2	VREFB2N0	IO			DIFFIO_L28p	M4
B2	VREFB2N0	IO			DIFFIO_L28n	M3
B2	VREFB2N0	IO			DIFFIO_L29p	N2
B2	VREFB2N0	IO			DIFFIO_L29n	N1
B2	VREFB2N0	IO	VREFB2N0			M5
B2	VREFB2N0	IO			DIFFIO_L30p	P2
B2	VREFB2N0	IO			DIFFIO_L30n	P1
B2	VREFB2N0	IO			DIFFIO_L31p	R2
B2	VREFB2N0	IO			DIFFIO_L31n	R1
B2	VREFB2N0	IO			DIFFIO_L32n	N5
B2	VREFB2N0	IO	DPCLK1		DIFFIO_L33p	P4
B2	VREFB2N0	IO			DIFFIO_L33n	P3
B2	VREFB2N0	IO			DIFFIO_L34p	U2
B2	VREFB2N1	IO			DIFFIO_L34n	U1
B2	VREFB2N1	IO			DIFFIO_L35p	V2
B2	VREFB2N1	IO			DIFFIO_L35n	V1
B2	VREFB2N1	IO			DIFFIO_L36p	P5
B2	VREFB2N1	IO			DIFFIO_L36n	N6
B2	VREFB2N1	IO			DIFFIO_L37p	R4
B2	VREFB2N1	IO			DIFFIO_L37n	R3
B2	VREFB2N1	IO			DIFFIO_L38p	W2
B2	VREFB2N1	IO			DIFFIO_L38n	W1
B2	VREFB2N1	IO			DIFFIO_L39p	Y2
B2	VREFB2N1	IO			DIFFIO_L39n	Y1
B2	VREFB2N1	IO	VREFB2N1			T3
B2	VREFB2N1	IO	RUP1			V4
B2	VREFB2N1	IO	RDN1			V3
B2	VREFB2N2	IO	VREFB2N2			R5
B2	VREFB2N2	IO	CDPCLK1		DIFFIO_L48p	T4
B2	VREFB2N2	IO			DIFFIO_L48n	T5
B3	VREFB3N2	IO			DIFFIO_B1n	V5

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B3	VREFB3N2	IO			DIFFIO_B3p	Y4
B3	VREFB3N2	IO			DIFFIO_B3n	Y3
B3	VREFB3N2	IO	CDPCLK2			Y6
B3	VREFB3N2	IO	PLL1_CLKOUTp			AA3
B3	VREFB3N2	IO	PLL1_CLKOUTn			AB3
B3	VREFB3N2	IO			DIFFIO_B4p	W6
B3	VREFB3N2	IO				AA4
B3	VREFB3N2	IO	VREFB3N2			AB4
B3	VREFB3N2	IO			DIFFIO_B5p	AA5
B3	VREFB3N2	IO			DIFFIO_B7n	AA6
B3	VREFB3N2	IO			DIFFIO_B8p	AB6
B3	VREFB3N2	IO			DIFFIO_B8n	AB5
B3	VREFB3N2	IO			DIFFIO_B9p	W7
B3	VREFB3N1	IO			DIFFIO_B9n	Y7
B3	VREFB3N1	IO			DIFFIO_B12n	U9
B3	VREFB3N1	IO			DIFFIO_B13p	V8
B3	VREFB3N1	IO			DIFFIO_B13n	W8
B3	VREFB3N1	IO			DIFFIO_B14p	AA7
B3	VREFB3N1	IO			DIFFIO_B14n	AB7
B3	VREFB3N1	IO				Y8
B3	VREFB3N1	IO	VREFB3N1			V9
B3	VREFB3N1	IO	DPCLK2		DIFFIO_B15p	V10
B3	VREFB3N1	IO			DIFFIO_B15n	U10
B3	VREFB3N1	IO			DIFFIO_B17p	AA8
B3	VREFB3N1	IO			DIFFIO_B17n	AB8
B3	VREFB3N1	IO			DIFFIO_B18p	AA9
B3	VREFB3N1	IO	DPCLK3		DIFFIO_B18n	AB9
B3	VREFB3N0	IO	VREFB3N0			U11
B3	VREFB3N0	IO				V11
B3	VREFB3N0	IO			DIFFIO_B23p	W10
B3	VREFB3N0	IO			DIFFIO_B23n	Y10
B3	VREFB3N0	IO			DIFFIO_B24p	AA10
B3	VREFB3N0	IO			DIFFIO_B24n	AB10
B3	VREFB3N0	CLK15	DIFFCLK_6p			AA11
B3	VREFB3N0	CLK14	DIFFCLK_6n			AB11
B4	VREFB4N2	CLK13	DIFFCLK_7p			AA12

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B4	VREFB4N2	CLK12	DIFFCLK_7n			AB12
B4	VREFB4N2	IO			DIFFIO_B32p	AA13
B4	VREFB4N2	IO			DIFFIO_B32n	AB13
B4	VREFB4N2	IO			DIFFIO_B35p	AA14
B4	VREFB4N2	IO			DIFFIO_B35n	AB14
B4	VREFB4N2	IO	VREFB4N2			V12
B4	VREFB4N2	IO			DIFFIO_B36p	W13
B4	VREFB4N2	IO	DPCLK4		DIFFIO_B36n	Y13
B4	VREFB4N2	IO			DIFFIO_B37p	AA15
B4	VREFB4N2	IO			DIFFIO_B37n	AB15
B4	VREFB4N2	IO			DIFFIO_B38p	U12
B4	VREFB4N2	IO			DIFFIO_B39p	Y14
B4	VREFB4N2	IO			DIFFIO_B39n	Y15
B4	VREFB4N2	IO			DIFFIO_B40p	AA16
B4	VREFB4N2	IO			DIFFIO_B40n	AB16
B4	VREFB4N2	IO	DPCLK5		DIFFIO_B41p	V13
B4	VREFB4N1	IO			DIFFIO_B41n	W14
B4	VREFB4N1	IO			DIFFIO_B43p	V14
B4	VREFB4N1	IO			DIFFIO_B44p	U14
B4	VREFB4N1	IO			DIFFIO_B44n	V15
B4	VREFB4N1	IO			DIFFIO_B45p	W15
B4	VREFB4N1	IO			DIFFIO_B46n	T15
B4	VREFB4N1	IO				AB18
B4	VREFB4N1	IO	VREFB4N1			AA18
B4	VREFB4N1	IO	RUP2			AA19
B4	VREFB4N1	IO	RDN2			AB19
B4	VREFB4N1	IO			DIFFIO_B48p	W17
B4	VREFB4N1	IO	CDPCLK3		DIFFIO_B48n	Y17
B4	VREFB4N1	IO			DIFFIO_B49p	AA20
B4	VREFB4N1	IO			DIFFIO_B49n	AB20
B4	VREFB4N0	IO	VREFB4N0			V16
B4	VREFB4N0	IO	PLL4_CLKOUTp			T16
B4	VREFB4N0	IO	PLL4_CLKOUTn			R16
B5	VREFB5N2	IO			DIFFIO_R51n	AA22
B5	VREFB5N2	IO			DIFFIO_R51p	AA21
B5	VREFB5N2	IO	RUP3			T17

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B5	VREFB5N2	IO	RDN3			T18
B5	VREFB5N2	IO	CDPCLK4		DIFFIO_R50n	W20
B5	VREFB5N2	IO	VREFB5N2			W19
B5	VREFB5N2	IO			DIFFIO_R49n	Y22
B5	VREFB5N2	IO			DIFFIO_R49p	R17
B5	VREFB5N2	IO			DIFFIO_R48n	U20
B5	VREFB5N2	IO			DIFFIO_R48p	M16
B5	VREFB5N2	IO			DIFFIO_R46n	W22
B5	VREFB5N2	IO			DIFFIO_R46p	W21
B5	VREFB5N2	IO			DIFFIO_R45n	T20
B5	VREFB5N2	IO			DIFFIO_R45p	T19
B5	VREFB5N1	IO			DIFFIO_R43n	V22
B5	VREFB5N1	IO			DIFFIO_R43p	V21
B5	VREFB5N1	IO			DIFFIO_R42n	R20
B5	VREFB5N1	IO			DIFFIO_R41n	U22
B5	VREFB5N1	IO			DIFFIO_R41p	U21
B5	VREFB5N1	IO			DIFFIO_R40p	R19
B5	VREFB5N1	IO			DIFFIO_R38n	R22
B5	VREFB5N1	IO			DIFFIO_R38p	R21
B5	VREFB5N1	IO	VREFB5N1			P20
B5	VREFB5N1	IO			DIFFIO_R36n	P22
B5	VREFB5N1	IO			DIFFIO_R36p	P21
B5	VREFB5N0	IO			DIFFIO_R33n	N20
B5	VREFB5N0	IO	VREFB5N0			N19
B5	VREFB5N0	IO	DPCLK6		DIFFIO_R30p	N18
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R29n	N22
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R29p	N21
B5	VREFB5N0	IO			DIFFIO_R28n	M22
B5	VREFB5N0	IO			DIFFIO_R28p	M21
B5	VREFB5N0	IO			DIFFIO_R27n	M20
B5	VREFB5N0	IO			DIFFIO_R27p	M19
B5	VREFB5N0	CLK7	DIFFCLK_3n			T22
B5	VREFB5N0	CLK6	DIFFCLK_3p			T21
B6	VREFB6N2	CLK5	DIFFCLK_2n			G22
B6	VREFB6N2	CLK4	DIFFCLK_2p			G21
B6	VREFB6N2	CONF_DONE		CONF_DONE		M18

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B6	VREFB6N2	MSEL0		MSEL0		M17
B6	VREFB6N2	MSEL1		MSEL1		L18
B6	VREFB6N2	MSEL2		MSEL2		L17
B6	VREFB6N2	MSEL3		MSEL3		K20
B6	VREFB6N2	IO		INIT_DONE	DIFFIO_R24n	L22
B6	VREFB6N2	IO		CRC_ERROR	DIFFIO_R24p	L21
B6	VREFB6N2	IO	VREFB6N2			K19
B6	VREFB6N2	IO		nCEO	DIFFIO_R23n	K22
B6	VREFB6N2	IO		CLKUSR	DIFFIO_R23p	K21
B6	VREFB6N2	IO	DPCLK7		DIFFIO_R22n	J22
B6	VREFB6N2	IO			DIFFIO_R22p	J21
B6	VREFB6N2	IO			DIFFIO_R21n	H22
B6	VREFB6N2	IO			DIFFIO_R21p	H21
B6	VREFB6N2	IO			DIFFIO_R20n	K18
B6	VREFB6N2	IO			DIFFIO_R20p	J18
B6	VREFB6N2	IO			DIFFIO_R18n	F22
B6	VREFB6N1	IO			DIFFIO_R18p	F21
B6	VREFB6N1	IO			DIFFIO_R17n	J20
B6	VREFB6N1	IO			DIFFIO_R16n	H20
B6	VREFB6N1	IO			DIFFIO_R16p	H19
B6	VREFB6N1	IO			DIFFIO_R15n	E22
B6	VREFB6N1	IO			DIFFIO_R15p	E21
B6	VREFB6N1	IO	VREFB6N1			H18
B6	VREFB6N1	IO			DIFFIO_R14n	D22
B6	VREFB6N1	IO			DIFFIO_R14p	D21
B6	VREFB6N1	IO			DIFFIO_R13n	F20
B6	VREFB6N1	IO			DIFFIO_R13p	F19
B6	VREFB6N1	IO			DIFFIO_R12n	G18
B6	VREFB6N1	IO			DIFFIO_R10n	C22
B6	VREFB6N1	IO			DIFFIO_R10p	C21
B6	VREFB6N0	IO			DIFFIO_R9n	B22
B6	VREFB6N0	IO			DIFFIO_R9p	B21
B6	VREFB6N0	IO	CDPCLK5		DIFFIO_R8n	C20
B6	VREFB6N0	IO	VREFB6N0			D20
B6	VREFB6N0	IO			DIFFIO_R2n	F17
B7	VREFB7N0	IO			DIFFIO_T60n	E16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B7	VREFB7N0	IO			DIFFIO_T60p	F15
B7	VREFB7N0	IO	CDPCLK6		DIFFIO_T59p	F14
B7	VREFB7N0	IO			DIFFIO_T58n	C18
B7	VREFB7N0	IO			DIFFIO_T58p	D18
B7	VREFB7N0	IO	VREFB7N0			D17
B7	VREFB7N0	IO			DIFFIO_T56n	C19
B7	VREFB7N0	IO			DIFFIO_T56p	D19
B7	VREFB7N0	IO	PLL2_CLKOUTp			B20
B7	VREFB7N0	IO	PLL2_CLKOUTn			A20
B7	VREFB7N0	IO			DIFFIO_T54p	C17
B7	VREFB7N0	IO	RUP4			B19
B7	VREFB7N0	IO	RDN4			A19
B7	VREFB7N1	IO			DIFFIO_T53n	A18
B7	VREFB7N1	IO			DIFFIO_T53p	B18
B7	VREFB7N1	IO			DIFFIO_T52n	D15
B7	VREFB7N1	IO			DIFFIO_T52p	E15
B7	VREFB7N1	IO			DIFFIO_T50n	A17
B7	VREFB7N1	IO			DIFFIO_T50p	B17
B7	VREFB7N1	IO			DIFFIO_T49n	A16
B7	VREFB7N1	IO			DIFFIO_T49p	B16
B7	VREFB7N1	IO	VREFB7N1			C15
B7	VREFB7N1	IO			DIFFIO_T46n	E14
B7	VREFB7N1	IO	DPCLK8		DIFFIO_T46p	F13
B7	VREFB7N1	IO			DIFFIO_T45n	A15
B7	VREFB7N1	IO			DIFFIO_T45p	B15
B7	VREFB7N1	IO			DIFFIO_T44n	C13
B7	VREFB7N1	IO			DIFFIO_T44p	D13
B7	VREFB7N2	IO	VREFB7N2			E13
B7	VREFB7N2	IO			DIFFIO_T36n	A14
B7	VREFB7N2	IO			DIFFIO_T36p	B14
B7	VREFB7N2	IO			DIFFIO_T35n	A13
B7	VREFB7N2	IO	DPCLK9		DIFFIO_T35p	B13
B7	VREFB7N2	IO			DIFFIO_T33p	E12
B7	VREFB7N2	IO			DIFFIO_T32n	E11
B7	VREFB7N2	IO			DIFFIO_T32p	F11
B7	VREFB7N2	CLK8	DIFFCLK_5n			A12

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B7	VREFB7N2	CLK9	DIFFCLK_5p			B12
B8	VREFB8N0	CLK10	DIFFCLK_4n			A11
B8	VREFB8N0	CLK11	DIFFCLK_4p			B11
B8	VREFB8N0	IO			DIFFIO_T31n	D10
B8	VREFB8N0	IO			DIFFIO_T30n	A10
B8	VREFB8N0	IO			DIFFIO_T30p	B10
B8	VREFB8N0	IO			DIFFIO_T29n	A9
B8	VREFB8N0	IO	DPCLK10		DIFFIO_T29p	B9
B8	VREFB8N0	IO	VREFB8N0			C10
B8	VREFB8N0	IO		DATA2	DIFFIO_T25n	A8
B8	VREFB8N0	IO		DATA3	DIFFIO_T25p	B8
B8	VREFB8N0	IO			DIFFIO_T23n	A7
B8	VREFB8N0	IO		DATA4	DIFFIO_T23p	B7
B8	VREFB8N0	IO			DIFFIO_T22n	A6
B8	VREFB8N0	IO			DIFFIO_T22p	B6
B8	VREFB8N0	IO			DIFFIO_T21n	E9
B8	VREFB8N1	IO	DPCLK11		DIFFIO_T20n	C8
B8	VREFB8N1	IO			DIFFIO_T20p	C7
B8	VREFB8N1	IO			DIFFIO_T19n	D8
B8	VREFB8N1	IO			DIFFIO_T19p	E8
B8	VREFB8N1	IO		DATA5	DIFFIO_T18p	A5
B8	VREFB8N1	IO	VREFB8N1			B5
B8	VREFB8N1	IO		DATA6	DIFFIO_T17p	F10
B8	VREFB8N1	IO		DATA7	DIFFIO_T15n	C6
B8	VREFB8N1	IO			DIFFIO_T15p	D7
B8	VREFB8N1	IO			DIFFIO_T14n	A4
B8	VREFB8N1	IO			DIFFIO_T14p	B4
B8	VREFB8N1	IO			DIFFIO_T11n	F8
B8	VREFB8N2	IO			DIFFIO_T9n	A3
B8	VREFB8N2	IO			DIFFIO_T9p	B3
B8	VREFB8N2	IO	VREFB8N2			D6
B8	VREFB8N2	IO			DIFFIO_T7n	E7
B8	VREFB8N2	IO			DIFFIO_T4n	C3
B8	VREFB8N2	IO	CDPCLK7		DIFFIO_T4p	C4
B8	VREFB8N2	IO			DIFFIO_T3n	F7
B8	VREFB8N2	IO				F9

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B8	VREFB8N2	IO	PLL3_CLKOUTp			E5
B8	VREFB8N2	IO	PLL3_CLKOUTn			E6
		GND				L10
		GND				L11
		GND				M10
		GND				M11
		GND				L12
		GND				L13
		GND				M12
		GND				M13
		GND				N11
		GND				K11
		GND				N12
		GND				K12
		GND				K13
		GND				N13
		GND				N10
		GND				K10
		GND				J9
		GND				F12
		GND				H12
		GND				H13
		GND				J15
		GND				K16
		GND				L15
		GND				N15
		GND				R13
		GND				R11
		GND				R9
		GND				P8
		GND				H14
		GND				H10
		GND				H8
		GND				N8
		GND				R7
		GND				T8

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		GND				T12
		GND				P16
		GND				L8
		GND				G17
		GND				M7
		GND				F16
		GND				H16
		GND				G15
		GND				G13
		GND				G11
		GND				E10
		GND				G9
		GND				K7
		GND				P6
		GND				U7
		GND				V6
		GND				T10
		GND				U13
		GND				T14
		GND				N17
		GND				G7
		GND				U19
		GND				Y21
		GND				R18
		GND				J5
		GND				J19
		GND				A1
		GND				C5
		GND				C9
		GND				C11
		GND				C12
		GND				C14
		GND				C16
		GND				A22
		GND				E20
		GND				G20

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		GND				L20
		GND				P19
		GND				V20
		GND				Y20
		GND				AB22
		GND				Y18
		GND				Y16
		GND				Y12
		GND				Y11
		GND				Y9
		GND				Y5
		GND				AB1
		GND				N3
		GND				U3
		GND				W3
		GND				D3
		GND				F3
		GND				K3
		GND				AA2
		GND				AA1
		GND				C1
		GND				C2
		GND				AA17
		GND				AB17
		GNDA1				U5
		GNDA2				E18
		GNDA3				F5
		GNDA4				V18
		VCCD_PLL1				U6
		VCCD_PLL2				E17
		VCCD_PLL3				F6
		VCCD_PLL4				V17
		VCCIO1				D4
		VCCIO1				F4
		VCCIO1				K4
		VCCIO2				N4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		VCCIO2				U4
		VCCIO2				W4
		VCCIO3				AB2
		VCCIO3				W5
		VCCIO3				W9
		VCCIO3				W11
		VCCIO4				AB21
		VCCIO4				W12
		VCCIO4				W16
		VCCIO4				W18
		VCCIO5				P18
		VCCIO5				V19
		VCCIO5				Y19
		VCCIO6				E19
		VCCIO6				G19
		VCCIO6				L19
		VCCIO7				A21
		VCCIO7				D12
		VCCIO7				D14
		VCCIO7				D16
		VCCIO8				A2
		VCCIO8				D5
		VCCIO8				D9
		VCCIO8				D11
		VCCA1				T6
		VCCA2				F18
		VCCA3				G6
		VCCA4				U18
		VCCINT				J11
		VCCINT				J12
		VCCINT				L14
		VCCINT				M14
		VCCINT				P11
		VCCINT				P12
		VCCINT				L9
		VCCINT				M9

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		VCCINT				J13
		VCCINT				J14
		VCCINT				K14
		VCCINT				J10
		VCCINT				K9
		VCCINT				N9
		VCCINT				P9
		VCCINT				P10
		VCCINT				P13
		VCCINT				P14
		VCCINT				N14
		VCCINT				J16
		VCCINT				K15
		VCCINT				L16
		VCCINT				M15
		VCCINT				R12
		VCCINT				R10
		VCCINT				R8
		VCCINT				H9
		VCCINT				G12
		VCCINT				J8
		VCCINT				M8
		VCCINT				T7
		VCCINT				T9
		VCCINT				T13
		VCCINT				P15
		VCCINT				H15
		VCCINT				H11
		VCCINT				K8
		VCCINT				P17
		VCCINT				L7
		VCCINT				N16
		VCCINT				K17
		VCCINT				J17
		VCCINT				G16
		VCCINT				G14

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		VCCINT				G10
		VCCINT				G8
		VCCINT				J7
		VCCINT				N7
		VCCINT				P7
		VCCINT				R6
		VCCINT				U8
		VCCINT				V7
		VCCINT				T11
		VCCINT				R15
		VCCINT				G4
		VCCINT				H17
		VCCINT				U17
		VCCINT				U16
		VCCINT				U15
		VCCINT				R14

Notes:

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B1	VREFB1N0	IO			DIFFIO_L1p	D3
B1	VREFB1N0	IO			DIFFIO_L1n	C2
B1	VREFB1N0	IO			DIFFIO_L2p	D2
B1	VREFB1N0	IO			DIFFIO_L2n	D1
B1	VREFB1N0	IO	VREFB1N0			H7
B1	VREFB1N0	IO			DIFFIO_L3p	G6
B1	VREFB1N0	IO			DIFFIO_L3n	G5
B1	VREFB1N0	IO	CDPCLK0		DIFFIO_L4p	E3
B1	VREFB1N0	IO			DIFFIO_L4n	F3
B1	VREFB1N0	IO			DIFFIO_L5p	F5
B1	VREFB1N0	IO		DATA1,ASDO	DIFFIO_L5n	F4
B1	VREFB1N0	IO				H6
B1	VREFB1N0	IO			DIFFIO_L6p	G4
B1	VREFB1N0	IO			DIFFIO_L6n	G3
B1	VREFB1N0	IO		FLASH_nCE,nCSO	DIFFIO_L8p	E2
B1	VREFB1N0	IO			DIFFIO_L8n	E1
B1	VREFB1N1	IO			DIFFIO_L9p	F2
B1	VREFB1N1	IO			DIFFIO_L9n	F1
B1	VREFB1N1	IO				H5
B1	VREFB1N1	IO	VREFB1N1			L5
B1	VREFB1N1	IO			DIFFIO_L10p	J4
B1	VREFB1N1	IO			DIFFIO_L10n	J3
B1	VREFB1N1	nSTATUS		nSTATUS		M6
B1	VREFB1N1	IO			DIFFIO_L11p	G2
B1	VREFB1N1	IO			DIFFIO_L11n	G1
B1	VREFB1N1	IO	DPCLK0		DIFFIO_L12p	K2
B1	VREFB1N1	IO			DIFFIO_L12n	K1
B1	VREFB1N1	IO			DIFFIO_L13p	K4
B1	VREFB1N1	IO			DIFFIO_L13n	K3
B1	VREFB1N1	IO			DIFFIO_L15p	M4
B1	VREFB1N1	IO			DIFFIO_L15n	M3
B1	VREFB1N1	IO			DIFFIO_L16p	J6
B1	VREFB1N1	IO			DIFFIO_L16n	J5
B1	VREFB1N1	IO			DIFFIO_L17p	J7
B1	VREFB1N1	IO			DIFFIO_L17n	K7
B1	VREFB1N2	IO			DIFFIO_L18p	K8
B1	VREFB1N2	IO			DIFFIO_L18n	L8
B1	VREFB1N2	IO	VREFB1N2			M5
B1	VREFB1N2	IO			DIFFIO_L19p	L7
B1	VREFB1N2	IO			DIFFIO_L19n	L6

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B1	VREFB1N2	IO			DIFFIO_L20p	N4
B1	VREFB1N2	IO			DIFFIO_L20n	N3
B1	VREFB1N2	IO			DIFFIO_L21p	M8
B1	VREFB1N2	IO			DIFFIO_L21n	M7
B1	VREFB1N2	IO			DIFFIO_L22p	L2
B1	VREFB1N2	IO			DIFFIO_L22n	L1
B1	VREFB1N2	IO			DIFFIO_L23p	M2
B1	VREFB1N2	IO			DIFFIO_L23n	M1
B1	VREFB1N2	IO			DIFFIO_L24p	P2
B1	VREFB1N2	IO			DIFFIO_L24n	P1
B1	VREFB1N2	IO				N8
B1	VREFB1N2	IO		DCLK		P3
B1	VREFB1N2	IO		DATA0		N7
B1	VREFB1N2	nCONFIG		nCONFIG		P4
B1	VREFB1N2	TDI		TDI		P7
B1	VREFB1N2	TCK		TCK		P5
B1	VREFB1N2	TMS		TMS		P8
B1	VREFB1N2	TDO		TDO		P6
B1	VREFB1N2	nCE		nCE		R8
B1	VREFB1N2	CLK0	DIFFCLK_0p			J2
B1	VREFB1N2	CLK1	DIFFCLK_0n			J1
B2	VREFB2N0	CLK2	DIFFCLK_1p			Y2
B2	VREFB2N0	CLK3	DIFFCLK_1n			Y1
B2	VREFB2N0	IO			DIFFIO_L25p	R2
B2	VREFB2N0	IO			DIFFIO_L25n	R1
B2	VREFB2N0	IO			DIFFIO_L26p	R7
B2	VREFB2N0	IO			DIFFIO_L26n	R6
B2	VREFB2N0	IO			DIFFIO_L27p	U3
B2	VREFB2N0	IO			DIFFIO_L27n	U4
B2	VREFB2N0	IO			DIFFIO_L28p	R3
B2	VREFB2N0	IO			DIFFIO_L28n	R4
B2	VREFB2N0	IO			DIFFIO_L29p	T4
B2	VREFB2N0	IO			DIFFIO_L29n	T3
B2	VREFB2N0	IO				R5
B2	VREFB2N0	IO	VREFB2N0			T7
B2	VREFB2N0	IO			DIFFIO_L30p	U2
B2	VREFB2N0	IO			DIFFIO_L30n	U1
B2	VREFB2N0	IO			DIFFIO_L31p	V4
B2	VREFB2N0	IO			DIFFIO_L31n	V3
B2	VREFB2N0	IO			DIFFIO_L32p	V2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B2	VREFB2N0	IO			DIFFIO_L32n	V1
B2	VREFB2N0	IO	DPCLK1		DIFFIO_L33p	AB2
B2	VREFB2N0	IO			DIFFIO_L33n	AB1
B2	VREFB2N0	IO			DIFFIO_L34p	W2
B2	VREFB2N1	IO			DIFFIO_L34n	W1
B2	VREFB2N1	IO			DIFFIO_L35p	U6
B2	VREFB2N1	IO			DIFFIO_L35n	U5
B2	VREFB2N1	IO			DIFFIO_L36p	Y4
B2	VREFB2N1	IO			DIFFIO_L36n	Y3
B2	VREFB2N1	IO			DIFFIO_L37p	AC2
B2	VREFB2N1	IO			DIFFIO_L37n	AC1
B2	VREFB2N1	IO			DIFFIO_L38p	AC3
B2	VREFB2N1	IO			DIFFIO_L38n	AD3
B2	VREFB2N1	IO			DIFFIO_L39p	AD2
B2	VREFB2N1	IO			DIFFIO_L39n	AD1
B2	VREFB2N1	IO				AB3
B2	VREFB2N1	IO	VREFB2N1			T8
B2	VREFB2N1	IO			DIFFIO_L40p	AA4
B2	VREFB2N1	IO			DIFFIO_L40n	AA3
B2	VREFB2N1	IO	RUP1			U7
B2	VREFB2N1	IO	RDN1			U8
B2	VREFB2N1	IO			DIFFIO_L41p	AE2
B2	VREFB2N1	IO			DIFFIO_L41n	AE1
B2	VREFB2N1	IO			DIFFIO_L42p	V6
B2	VREFB2N1	IO			DIFFIO_L42n	V5
B2	VREFB2N1	IO			DIFFIO_L43p	V8
B2	VREFB2N1	IO			DIFFIO_L43n	V7
B2	VREFB2N2	IO			DIFFIO_L44p	W4
B2	VREFB2N2	IO			DIFFIO_L44n	W3
B2	VREFB2N2	IO			DIFFIO_L45p	Y6
B2	VREFB2N2	IO			DIFFIO_L45n	Y5
B2	VREFB2N2	IO				W7
B2	VREFB2N2	IO			DIFFIO_L46p	W8
B2	VREFB2N2	IO			DIFFIO_L46n	Y7
B2	VREFB2N2	IO			DIFFIO_L47p	AA6
B2	VREFB2N2	IO			DIFFIO_L47n	AA5
B2	VREFB2N2	IO				AA7
B2	VREFB2N2	IO	VREFB2N2			AB4
B2	VREFB2N2	IO	CDPCLK1		DIFFIO_L48p	AE3
B2	VREFB2N2	IO			DIFFIO_L48n	AF2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B2	VREFB2N2	IO			DIFFIO_L50p	AB6
B2	VREFB2N2	IO			DIFFIO_L50n	AB5
B3	VREFB3N2	IO			DIFFIO_B1p	AD5
B3	VREFB3N2	IO			DIFFIO_B1n	AE6
B3	VREFB3N2	IO			DIFFIO_B2p	AD4
B3	VREFB3N2	IO			DIFFIO_B2n	AF4
B3	VREFB3N2	IO			DIFFIO_B3p	AE4
B3	VREFB3N2	IO			DIFFIO_B3n	AG3
B3	VREFB3N2	IO	CDPCLK2			AD7
B3	VREFB3N2	IO	PLL1_CLKOUTp			AE5
B3	VREFB3N2	IO	PLL1_CLKOUTn			AF5
B3	VREFB3N2	IO			DIFFIO_B4p	AH3
B3	VREFB3N2	IO			DIFFIO_B4n	AF3
B3	VREFB3N2	IO				AF6
B3	VREFB3N2	IO	VREFB3N2			Y10
B3	VREFB3N2	IO			DIFFIO_B5p	AG4
B3	VREFB3N2	IO			DIFFIO_B5n	AH4
B3	VREFB3N2	IO			DIFFIO_B6p	AD8
B3	VREFB3N2	IO			DIFFIO_B6n	AC7
B3	VREFB3N2	IO			DIFFIO_B7p	AG6
B3	VREFB3N2	IO			DIFFIO_B7n	AH6
B3	VREFB3N2	IO			DIFFIO_B8p	AB9
B3	VREFB3N2	IO			DIFFIO_B8n	AB8
B3	VREFB3N2	IO				AD10
B3	VREFB3N2	IO			DIFFIO_B9p	AG7
B3	VREFB3N1	IO			DIFFIO_B9n	AH7
B3	VREFB3N1	IO			DIFFIO_B10p	AB7
B3	VREFB3N1	IO			DIFFIO_B10n	AC8
B3	VREFB3N1	IO			DIFFIO_B11p	AA8
B3	VREFB3N1	IO			DIFFIO_B11n	AA10
B3	VREFB3N1	IO			DIFFIO_B12p	AG8
B3	VREFB3N1	IO			DIFFIO_B12n	AH8
B3	VREFB3N1	IO			DIFFIO_B13p	AE7
B3	VREFB3N1	IO			DIFFIO_B13n	AF7
B3	VREFB3N1	IO				AF9
B3	VREFB3N1	IO			DIFFIO_B14p	AE8
B3	VREFB3N1	IO			DIFFIO_B14n	AF8
B3	VREFB3N1	IO				AE9
B3	VREFB3N1	IO	VREFB3N1			AB11
B3	VREFB3N1	IO	DPCLK2		DIFFIO_B15p	AE10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B3	VREFB3N1	IO			DIFFIO_B15n	AF10
B3	VREFB3N1	IO			DIFFIO_B16p	AG10
B3	VREFB3N1	IO			DIFFIO_B16n	AH10
B3	VREFB3N1	IO			DIFFIO_B17p	AE12
B3	VREFB3N1	IO			DIFFIO_B17n	AF12
B3	VREFB3N1	IO			DIFFIO_B18p	AE11
B3	VREFB3N1	IO	DPCLK3		DIFFIO_B18n	AF11
B3	VREFB3N1	IO			DIFFIO_B19p	AB10
B3	VREFB3N0	IO			DIFFIO_B19n	AC10
B3	VREFB3N0	IO			DIFFIO_B20p	AG11
B3	VREFB3N0	IO			DIFFIO_B20n	AH11
B3	VREFB3N0	IO			DIFFIO_B21p	AE13
B3	VREFB3N0	IO			DIFFIO_B21n	AF13
B3	VREFB3N0	IO			DIFFIO_B22p	AC12
B3	VREFB3N0	IO			DIFFIO_B22n	AB12
B3	VREFB3N0	IO	VREFB3N0			AB13
B3	VREFB3N0	IO				AD12
B3	VREFB3N0	IO			DIFFIO_B23p	AE14
B3	VREFB3N0	IO			DIFFIO_B23n	AF14
B3	VREFB3N0	IO			DIFFIO_B24p	AC11
B3	VREFB3N0	IO			DIFFIO_B24n	AD11
B3	VREFB3N0	IO			DIFFIO_B25p	Y12
B3	VREFB3N0	IO			DIFFIO_B25n	AA12
B3	VREFB3N0	IO			DIFFIO_B26p	Y13
B3	VREFB3N0	IO			DIFFIO_B26n	AA13
B3	VREFB3N0	IO			DIFFIO_B27p	AA14
B3	VREFB3N0	IO			DIFFIO_B27n	AB14
B3	VREFB3N0	IO			DIFFIO_B28p	AG12
B3	VREFB3N0	IO			DIFFIO_B28n	AH12
B3	VREFB3N0	IO			DIFFIO_B29p	AC14
B3	VREFB3N0	IO			DIFFIO_B29n	AD14
B3	VREFB3N0	IO			DIFFIO_B30p	Y14
B3	VREFB3N0	IO			DIFFIO_B30n	Y15
B3	VREFB3N0	CLK15	DIFFCLK_6p			AG14
B3	VREFB3N0	CLK14	DIFFCLK_6n			AH14
B4	VREFB4N2	CLK13	DIFFCLK_7p			AG15
B4	VREFB4N2	CLK12	DIFFCLK_7n			AH15
B4	VREFB4N2	IO			DIFFIO_B31p	AC15
B4	VREFB4N2	IO			DIFFIO_B31n	AD15
B4	VREFB4N2	IO			DIFFIO_B32p	AE15

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B4	VREFB4N2	IO			DIFFIO_B32n	AF15
B4	VREFB4N2	IO			DIFFIO_B33p	AG17
B4	VREFB4N2	IO			DIFFIO_B33n	AH17
B4	VREFB4N2	IO			DIFFIO_B34p	AE16
B4	VREFB4N2	IO			DIFFIO_B34n	AF16
B4	VREFB4N2	IO			DIFFIO_B35p	AA16
B4	VREFB4N2	IO			DIFFIO_B35n	AB16
B4	VREFB4N2	IO	VREFB4N2			AA15
B4	VREFB4N2	IO				AB15
B4	VREFB4N2	IO			DIFFIO_B36p	AE17
B4	VREFB4N2	IO	DPCLK4		DIFFIO_B36n	AF17
B4	VREFB4N2	IO			DIFFIO_B37p	AG18
B4	VREFB4N2	IO			DIFFIO_B37n	AH18
B4	VREFB4N2	IO			DIFFIO_B38p	AG19
B4	VREFB4N2	IO			DIFFIO_B38n	AH19
B4	VREFB4N2	IO			DIFFIO_B39p	AC17
B4	VREFB4N2	IO			DIFFIO_B39n	AD17
B4	VREFB4N2	IO			DIFFIO_B40p	AG21
B4	VREFB4N2	IO			DIFFIO_B40n	AH21
B4	VREFB4N2	IO	DPCLK5		DIFFIO_B41p	AE18
B4	VREFB4N1	IO			DIFFIO_B41n	AF18
B4	VREFB4N1	IO			DIFFIO_B42p	AG22
B4	VREFB4N1	IO			DIFFIO_B42n	AH22
B4	VREFB4N1	IO			DIFFIO_B43p	AG23
B4	VREFB4N1	IO			DIFFIO_B43n	AH23
B4	VREFB4N1	IO			DIFFIO_B44p	AE19
B4	VREFB4N1	IO			DIFFIO_B44n	AF19
B4	VREFB4N1	IO			DIFFIO_B45p	AF24
B4	VREFB4N1	IO			DIFFIO_B45n	AF25
B4	VREFB4N1	IO			DIFFIO_B46p	AE20
B4	VREFB4N1	IO			DIFFIO_B46n	AF20
B4	VREFB4N1	IO				AD18
B4	VREFB4N1	IO			DIFFIO_B47p	AE21
B4	VREFB4N1	IO			DIFFIO_B47n	AF21
B4	VREFB4N1	IO	VREFB4N1			AC18
B4	VREFB4N1	IO	RUP2			AA17
B4	VREFB4N1	IO	RDN2			AB17
B4	VREFB4N1	IO			DIFFIO_B48p	AE25
B4	VREFB4N1	IO	CDPCLK3		DIFFIO_B48n	AF26
B4	VREFB4N1	IO			DIFFIO_B49p	AG25

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B4	VREFB4N1	IO			DIFFIO_B49n	AH25
B4	VREFB4N0	IO			DIFFIO_B50p	AC19
B4	VREFB4N0	IO			DIFFIO_B50n	AD19
B4	VREFB4N0	IO			DIFFIO_B51p	Y17
B4	VREFB4N0	IO			DIFFIO_B51n	Y16
B4	VREFB4N0	IO			DIFFIO_B52p	AE22
B4	VREFB4N0	IO			DIFFIO_B52n	AF22
B4	VREFB4N0	IO			DIFFIO_B53p	AB19
B4	VREFB4N0	IO			DIFFIO_B53n	AB18
B4	VREFB4N0	IO			DIFFIO_B54p	AD25
B4	VREFB4N0	IO			DIFFIO_B54n	AE24
B4	VREFB4N0	IO	VREFB4N0			AB20
B4	VREFB4N0	IO			DIFFIO_B55p	AC21
B4	VREFB4N0	IO			DIFFIO_B55n	AD21
B4	VREFB4N0	IO				AD24
B4	VREFB4N0	IO	PLL4_CLKOUTp			AE23
B4	VREFB4N0	IO	PLL4_CLKOUTn			AF23
B4	VREFB4N0	IO			DIFFIO_B56p	Y19
B4	VREFB4N0	IO			DIFFIO_B56n	AA19
B4	VREFB4N0	IO			DIFFIO_B57p	AB22
B4	VREFB4N0	IO			DIFFIO_B57n	AB21
B4	VREFB4N0	IO			DIFFIO_B58p	AC22
B4	VREFB4N0	IO			DIFFIO_B58n	AD22
B4	VREFB4N0	IO				AA21
B4	VREFB4N0	IO			DIFFIO_B59p	AG26
B4	VREFB4N0	IO			DIFFIO_B59n	AH26
B5	VREFB5N2	IO			DIFFIO_R51n	AC25
B5	VREFB5N2	IO			DIFFIO_R51p	AC24
B5	VREFB5N2	IO				AB24
B5	VREFB5N2	IO	RUP3			AA22
B5	VREFB5N2	IO	RDN3			AB23
B5	VREFB5N2	IO	CDPCLK4		DIFFIO_R50n	AF27
B5	VREFB5N2	IO			DIFFIO_R50p	AE26
B5	VREFB5N2	IO	VREFB5N2			AA24
B5	VREFB5N2	IO				AA23
B5	VREFB5N2	IO			DIFFIO_R49n	AD26
B5	VREFB5N2	IO			DIFFIO_R49p	AC26
B5	VREFB5N2	IO			DIFFIO_R48n	AE28
B5	VREFB5N2	IO			DIFFIO_R48p	AE27
B5	VREFB5N2	IO			DIFFIO_R47n	AD28

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B5	VREFB5N2	IO			DIFFIO_R47p	AD27
B5	VREFB5N2	IO			DIFFIO_R46n	Y24
B5	VREFB5N2	IO			DIFFIO_R46p	Y23
B5	VREFB5N2	IO			DIFFIO_R45n	AC28
B5	VREFB5N2	IO			DIFFIO_R45p	AC27
B5	VREFB5N1	IO			DIFFIO_R44n	AB26
B5	VREFB5N1	IO			DIFFIO_R44p	AB25
B5	VREFB5N1	IO			DIFFIO_R43n	AA26
B5	VREFB5N1	IO			DIFFIO_R43p	AA25
B5	VREFB5N1	IO			DIFFIO_R42n	AB28
B5	VREFB5N1	IO			DIFFIO_R42p	AB27
B5	VREFB5N1	IO			DIFFIO_R41n	Y26
B5	VREFB5N1	IO			DIFFIO_R41p	Y25
B5	VREFB5N1	IO			DIFFIO_R40n	W26
B5	VREFB5N1	IO			DIFFIO_R40p	W25
B5	VREFB5N1	IO			DIFFIO_R39n	W27
B5	VREFB5N1	IO			DIFFIO_R39p	W28
B5	VREFB5N1	IO			DIFFIO_R38n	V28
B5	VREFB5N1	IO			DIFFIO_R38p	V27
B5	VREFB5N1	IO	VREFB5N1			U23
B5	VREFB5N1	IO			DIFFIO_R37n	V26
B5	VREFB5N1	IO			DIFFIO_R37p	V25
B5	VREFB5N1	IO			DIFFIO_R36n	V24
B5	VREFB5N1	IO			DIFFIO_R36p	V23
B5	VREFB5N1	IO			DIFFIO_R35n	W21
B5	VREFB5N1	IO			DIFFIO_R35p	V21
B5	VREFB5N1	IO			DIFFIO_R34n	V22
B5	VREFB5N0	IO			DIFFIO_R34p	U22
B5	VREFB5N0	IO			DIFFIO_R33n	U26
B5	VREFB5N0	IO			DIFFIO_R33p	U25
B5	VREFB5N0	IO	VREFB5N0			U24
B5	VREFB5N0	IO			DIFFIO_R32n	U28
B5	VREFB5N0	IO			DIFFIO_R32p	U27
B5	VREFB5N0	IO				U21
B5	VREFB5N0	IO			DIFFIO_R31n	Y22
B5	VREFB5N0	IO			DIFFIO_R31p	W22
B5	VREFB5N0	IO			DIFFIO_R30n	T26
B5	VREFB5N0	IO	DPCLK6		DIFFIO_R30p	T25
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R29n	T22
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R29p	T21

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B5	VREFB5N0	IO			DIFFIO_R28n	R26
B5	VREFB5N0	IO			DIFFIO_R28p	R25
B5	VREFB5N0	IO			DIFFIO_R27n	R28
B5	VREFB5N0	IO			DIFFIO_R27p	R27
B5	VREFB5N0	IO				R24
B5	VREFB5N0	IO			DIFFIO_R26n	R23
B5	VREFB5N0	IO			DIFFIO_R26p	R22
B5	VREFB5N0	IO			DIFFIO_R25n	R21
B5	VREFB5N0	IO			DIFFIO_R25p	P21
B5	VREFB5N0	CLK7	DIFFCLK_3n			Y28
B5	VREFB5N0	CLK6	DIFFCLK_3p			Y27
B6	VREFB6N2	CLK5	DIFFCLK_2n			J28
B6	VREFB6N2	CLK4	DIFFCLK_2p			J27
B6	VREFB6N2	CONF_DONE		CONF_DONE		P24
B6	VREFB6N2	MSEL0		MSEL0		N22
B6	VREFB6N2	MSEL1		MSEL1		P23
B6	VREFB6N2	MSEL2		MSEL2		M22
B6	VREFB6N2	MSEL3		MSEL3		P22
B6	VREFB6N2	IO				M23
B6	VREFB6N2	IO		INIT_DONE	DIFFIO_R24n	P26
B6	VREFB6N2	IO		CRC_ERROR	DIFFIO_R24p	P25
B6	VREFB6N2	IO				M24
B6	VREFB6N2	IO	VREFB6N2			N21
B6	VREFB6N2	IO		nCEO	DIFFIO_R23n	P28
B6	VREFB6N2	IO		CLKUSR	DIFFIO_R23p	P27
B6	VREFB6N2	IO	DPCLK7		DIFFIO_R22n	N26
B6	VREFB6N2	IO			DIFFIO_R22p	N25
B6	VREFB6N2	IO			DIFFIO_R21n	M28
B6	VREFB6N2	IO			DIFFIO_R21p	M27
B6	VREFB6N2	IO			DIFFIO_R20n	M26
B6	VREFB6N2	IO			DIFFIO_R20p	M25
B6	VREFB6N2	IO			DIFFIO_R19n	L28
B6	VREFB6N2	IO			DIFFIO_R19p	L27
B6	VREFB6N2	IO			DIFFIO_R18n	L24
B6	VREFB6N1	IO			DIFFIO_R18p	L23
B6	VREFB6N1	IO			DIFFIO_R17n	K28
B6	VREFB6N1	IO			DIFFIO_R17p	K27
B6	VREFB6N1	IO				L26
B6	VREFB6N1	IO			DIFFIO_R16n	J26
B6	VREFB6N1	IO			DIFFIO_R16p	J25

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B6	VREFB6N1	IO			DIFFIO_R15n	G28
B6	VREFB6N1	IO			DIFFIO_R15p	G27
B6	VREFB6N1	IO	VREFB6N1			M21
B6	VREFB6N1	IO				L25
B6	VREFB6N1	IO			DIFFIO_R14n	K26
B6	VREFB6N1	IO			DIFFIO_R14p	K25
B6	VREFB6N1	IO			DIFFIO_R13n	F28
B6	VREFB6N1	IO			DIFFIO_R13p	F27
B6	VREFB6N1	IO			DIFFIO_R12n	E28
B6	VREFB6N1	IO			DIFFIO_R12p	E27
B6	VREFB6N1	IO			DIFFIO_R11n	H26
B6	VREFB6N1	IO			DIFFIO_R11p	H25
B6	VREFB6N1	IO			DIFFIO_R10n	E26
B6	VREFB6N1	IO			DIFFIO_R10p	F26
B6	VREFB6N0	IO			DIFFIO_R9n	D28
B6	VREFB6N0	IO			DIFFIO_R9p	D27
B6	VREFB6N0	IO	CDPCLK5		DIFFIO_R8n	C27
B6	VREFB6N0	IO			DIFFIO_R8p	D26
B6	VREFB6N0	IO			DIFFIO_R7n	L22
B6	VREFB6N0	IO			DIFFIO_R7p	L21
B6	VREFB6N0	IO			DIFFIO_R6n	J24
B6	VREFB6N0	IO			DIFFIO_R6p	J23
B6	VREFB6N0	IO			DIFFIO_R5n	K22
B6	VREFB6N0	IO			DIFFIO_R5p	K21
B6	VREFB6N0	IO			DIFFIO_R4n	H24
B6	VREFB6N0	IO			DIFFIO_R4p	H23
B6	VREFB6N0	IO			DIFFIO_R3n	G26
B6	VREFB6N0	IO			DIFFIO_R3p	G25
B6	VREFB6N0	IO	VREFB6N0			J22
B6	VREFB6N0	IO			DIFFIO_R2n	F25
B6	VREFB6N0	IO			DIFFIO_R2p	F24
B6	VREFB6N0	IO			DIFFIO_R1n	G24
B6	VREFB6N0	IO			DIFFIO_R1p	G23
B6	VREFB6N0	IO				H22
B7	VREFB7N0	IO			DIFFIO_T61n	C26
B7	VREFB7N0	IO			DIFFIO_T61p	B26
B7	VREFB7N0	IO			DIFFIO_T60n	D22
B7	VREFB7N0	IO			DIFFIO_T60p	E22
B7	VREFB7N0	IO			DIFFIO_T59n	A26
B7	VREFB7N0	IO	CDPCLK6		DIFFIO_T59p	A25

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B7	VREFB7N0	IO				B25
B7	VREFB7N0	IO			DIFFIO_T58n	E21
B7	VREFB7N0	IO			DIFFIO_T58p	F21
B7	VREFB7N0	IO	VREFB7N0			F22
B7	VREFB7N0	IO			DIFFIO_T57n	D25
B7	VREFB7N0	IO			DIFFIO_T57p	C25
B7	VREFB7N0	IO			DIFFIO_T56n	A23
B7	VREFB7N0	IO			DIFFIO_T56p	B23
B7	VREFB7N0	IO	PLL2_CLKOUTp			D23
B7	VREFB7N0	IO	PLL2_CLKOUTn			C23
B7	VREFB7N0	IO			DIFFIO_T55n	C24
B7	VREFB7N0	IO			DIFFIO_T55p	D24
B7	VREFB7N0	IO			DIFFIO_T54n	C22
B7	VREFB7N0	IO			DIFFIO_T54p	D21
B7	VREFB7N0	IO	RUP4			F19
B7	VREFB7N0	IO	RDN4			E19
B7	VREFB7N0	IO				C21
B7	VREFB7N1	IO			DIFFIO_T53n	A22
B7	VREFB7N1	IO			DIFFIO_T53p	B22
B7	VREFB7N1	IO			DIFFIO_T52n	A21
B7	VREFB7N1	IO			DIFFIO_T52p	B21
B7	VREFB7N1	IO			DIFFIO_T51n	E18
B7	VREFB7N1	IO			DIFFIO_T51p	F18
B7	VREFB7N1	IO			DIFFIO_T50n	C18
B7	VREFB7N1	IO			DIFFIO_T50p	D18
B7	VREFB7N1	IO			DIFFIO_T49n	C20
B7	VREFB7N1	IO			DIFFIO_T49p	D20
B7	VREFB7N1	IO			DIFFIO_T48n	E24
B7	VREFB7N1	IO			DIFFIO_T48p	E25
B7	VREFB7N1	IO			DIFFIO_T47n	C19
B7	VREFB7N1	IO			DIFFIO_T47p	D19
B7	VREFB7N1	IO	VREFB7N1			G17
B7	VREFB7N1	IO			DIFFIO_T46n	C17
B7	VREFB7N1	IO	DPCLK8		DIFFIO_T46p	D17
B7	VREFB7N1	IO			DIFFIO_T45n	A19
B7	VREFB7N1	IO			DIFFIO_T45p	B19
B7	VREFB7N1	IO			DIFFIO_T44n	A18
B7	VREFB7N1	IO			DIFFIO_T44p	B18
B7	VREFB7N1	IO			DIFFIO_T43n	G20
B7	VREFB7N1	IO			DIFFIO_T43p	G21

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B7	VREFB7N2	IO			DIFFIO_T42n	H19
B7	VREFB7N2	IO			DIFFIO_T42p	J19
B7	VREFB7N2	IO			DIFFIO_T41n	H21
B7	VREFB7N2	IO			DIFFIO_T41p	G22
B7	VREFB7N2	IO				J17
B7	VREFB7N2	IO			DIFFIO_T40n	G19
B7	VREFB7N2	IO			DIFFIO_T40p	G18
B7	VREFB7N2	IO			DIFFIO_T39n	G16
B7	VREFB7N2	IO			DIFFIO_T39p	H17
B7	VREFB7N2	IO			DIFFIO_T38n	F17
B7	VREFB7N2	IO			DIFFIO_T38p	E17
B7	VREFB7N2	IO	VREFB7N2			G15
B7	VREFB7N2	IO			DIFFIO_T37n	J16
B7	VREFB7N2	IO			DIFFIO_T37p	H16
B7	VREFB7N2	IO			DIFFIO_T36n	C16
B7	VREFB7N2	IO			DIFFIO_T36p	D16
B7	VREFB7N2	IO			DIFFIO_T35n	A17
B7	VREFB7N2	IO	DPCLK9		DIFFIO_T35p	B17
B7	VREFB7N2	IO			DIFFIO_T34n	H15
B7	VREFB7N2	IO			DIFFIO_T34p	J15
B7	VREFB7N2	IO			DIFFIO_T33n	F15
B7	VREFB7N2	IO			DIFFIO_T33p	E15
B7	VREFB7N2	IO			DIFFIO_T32n	C15
B7	VREFB7N2	IO			DIFFIO_T32p	D15
B7	VREFB7N2	CLK8	DIFFCLK_5n			A15
B7	VREFB7N2	CLK9	DIFFCLK_5p			B15
B8	VREFB8N0	CLK10	DIFFCLK_4n			A14
B8	VREFB8N0	CLK11	DIFFCLK_4p			B14
B8	VREFB8N0	IO			DIFFIO_T31n	C13
B8	VREFB8N0	IO			DIFFIO_T31p	D13
B8	VREFB8N0	IO			DIFFIO_T30n	C14
B8	VREFB8N0	IO			DIFFIO_T30p	D14
B8	VREFB8N0	IO			DIFFIO_T29n	C12
B8	VREFB8N0	IO	DPCLK10		DIFFIO_T29p	D12
B8	VREFB8N0	IO			DIFFIO_T28n	H14
B8	VREFB8N0	IO			DIFFIO_T28p	J14
B8	VREFB8N0	IO			DIFFIO_T27n	A12
B8	VREFB8N0	IO			DIFFIO_T27p	B12
B8	VREFB8N0	IO	VREFB8N0			G14
B8	VREFB8N0	IO			DIFFIO_T26n	F14

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B8	VREFB8N0	IO			DIFFIO_T26p	E14
B8	VREFB8N0	IO		DATA2	DIFFIO_T25n	A11
B8	VREFB8N0	IO		DATA3	DIFFIO_T25p	B11
B8	VREFB8N0	IO			DIFFIO_T24n	J13
B8	VREFB8N0	IO			DIFFIO_T24p	J12
B8	VREFB8N0	IO			DIFFIO_T23n	A10
B8	VREFB8N0	IO		DATA4	DIFFIO_T23p	B10
B8	VREFB8N0	IO			DIFFIO_T22n	G13
B8	VREFB8N0	IO			DIFFIO_T22p	H13
B8	VREFB8N0	IO			DIFFIO_T21n	C10
B8	VREFB8N1	IO			DIFFIO_T21p	D10
B8	VREFB8N1	IO	DPCLK11		DIFFIO_T20n	E12
B8	VREFB8N1	IO			DIFFIO_T20p	F12
B8	VREFB8N1	IO			DIFFIO_T19n	E11
B8	VREFB8N1	IO			DIFFIO_T19p	F11
B8	VREFB8N1	IO			DIFFIO_T18n	A7
B8	VREFB8N1	IO		DATA5	DIFFIO_T18p	B7
B8	VREFB8N1	IO	VREFB8N1			G12
B8	VREFB8N1	IO			DIFFIO_T17n	A6
B8	VREFB8N1	IO		DATA6	DIFFIO_T17p	B6
B8	VREFB8N1	IO			DIFFIO_T16n	G11
B8	VREFB8N1	IO			DIFFIO_T16p	H12
B8	VREFB8N1	IO		DATA7	DIFFIO_T15n	C11
B8	VREFB8N1	IO			DIFFIO_T15p	D11
B8	VREFB8N1	IO			DIFFIO_T14n	C9
B8	VREFB8N1	IO			DIFFIO_T14p	D9
B8	VREFB8N1	IO			DIFFIO_T13n	F10
B8	VREFB8N1	IO			DIFFIO_T13p	G10
B8	VREFB8N1	IO			DIFFIO_T12n	H10
B8	VREFB8N1	IO			DIFFIO_T12p	J10
B8	VREFB8N1	IO				E10
B8	VREFB8N1	IO			DIFFIO_T11n	A8
B8	VREFB8N1	IO			DIFFIO_T11p	B8
B8	VREFB8N1	IO			DIFFIO_T10n	C8
B8	VREFB8N2	IO			DIFFIO_T10p	D8
B8	VREFB8N2	IO			DIFFIO_T9n	C7
B8	VREFB8N2	IO			DIFFIO_T9p	D7
B8	VREFB8N2	IO			DIFFIO_T8n	E7
B8	VREFB8N2	IO			DIFFIO_T8p	D6
B8	VREFB8N2	IO	VREFB8N2			G9

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
B8	VREFB8N2	IO			DIFFIO_T7n	E8
B8	VREFB8N2	IO			DIFFIO_T7p	F8
B8	VREFB8N2	IO			DIFFIO_T6n	G8
B8	VREFB8N2	IO			DIFFIO_T6p	H8
B8	VREFB8N2	IO			DIFFIO_T5n	G7
B8	VREFB8N2	IO			DIFFIO_T5p	F7
B8	VREFB8N2	IO			DIFFIO_T4n	A4
B8	VREFB8N2	IO	CDPCLK7		DIFFIO_T4p	B4
B8	VREFB8N2	IO			DIFFIO_T3n	B3
B8	VREFB8N2	IO			DIFFIO_T3p	A3
B8	VREFB8N2	IO				C6
B8	VREFB8N2	IO	PLL3_CLKOUTp			D5
B8	VREFB8N2	IO	PLL3_CLKOUTn			C5
B8	VREFB8N2	IO			DIFFIO_T2n	C4
B8	VREFB8N2	IO			DIFFIO_T2p	D4
B8	VREFB8N2	IO			DIFFIO_T1n	E4
B8	VREFB8N2	IO			DIFFIO_T1p	E5
B8	VREFB8N2	IO				C3
		GND				K10
		GND				K12
		GND				K14
		GND				K16
		GND				K18
		GND				K20
		GND				L9
		GND				L11
		GND				L13
		GND				L15
		GND				L17
		GND				L19
		GND				M10
		GND				M12
		GND				M14
		GND				M16
		GND				M18
		GND				M20
		GND				N9
		GND				N11
		GND				N13
		GND				N15

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
		GND				N17
		GND				N19
		GND				P10
		GND				P12
		GND				P14
		GND				P16
		GND				P18
		GND				P20
		GND				R9
		GND				R11
		GND				R13
		GND				R15
		GND				R17
		GND				R19
		GND				T10
		GND				T12
		GND				T14
		GND				T16
		GND				T18
		GND				T20
		GND				U9
		GND				U11
		GND				U13
		GND				U15
		GND				U17
		GND				U19
		GND				V10
		GND				V12
		GND				V14
		GND				V16
		GND				V18
		GND				V20
		GND				W9
		GND				W11
		GND				W13
		GND				W15
		GND				W17
		GND				W19
		GND				AA2
		GND				AA27

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
		GND				AC6
		GND				AC9
		GND				AC13
		GND				AC16
		GND				AC20
		GND				AC23
		GND				AF1
		GND				AF28
		GND				AG2
		GND				AG5
		GND				AG9
		GND				AG13
		GND				AG16
		GND				AG20
		GND				AG24
		GND				AG27
		GND				B2
		GND				B5
		GND				B9
		GND				B13
		GND				B16
		GND				B20
		GND				B24
		GND				B27
		GND				C1
		GND				C28
		GND				F6
		GND				F9
		GND				F13
		GND				F16
		GND				F20
		GND				F23
		GND				H2
		GND				H27
		GND				J11
		GND				J18
		GND				K6
		GND				K23
		GND				N2
		GND				N6

Pin Information for the Intel® Cyclone®10 10CL120 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
		GND				N23
		GND				N27
		GND				T2
		GND				T6
		GND				T23
		GND				T27
		GND				W6
		GND				W23
		GND				Y11
		GND				Y18
		GND				H4
		GND				H3
		GND				L3
		GND				L4
		GND				AC4
		GND				AC5
		GNDA1				AA9
		GNDA2				H20
		GNDA3				H9
		GNDA4				AA20
		VCCD_PLL1				Y9
		VCCD_PLL2				J20
		VCCD_PLL3				J9
		VCCD_PLL4				Y20
		VCCIO1				B1
		VCCIO1				H1
		VCCIO1				K5
		VCCIO1				N1
		VCCIO1				N5
		VCCIO2				AA1
		VCCIO2				AG1
		VCCIO2				T1
		VCCIO2				T5
		VCCIO2				W5
		VCCIO3				AA11
		VCCIO3				AD6
		VCCIO3				AD9
		VCCIO3				AD13
		VCCIO3				AH2
		VCCIO3				AH5

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
		VCCIO3				AH9
		VCCIO3				AH13
		VCCIO4				AA18
		VCCIO4				AD16
		VCCIO4				AD20
		VCCIO4				AD23
		VCCIO4				AH16
		VCCIO4				AH20
		VCCIO4				AH24
		VCCIO4				AH27
		VCCIO5				AA28
		VCCIO5				AG28
		VCCIO5				T24
		VCCIO5				T28
		VCCIO5				W24
		VCCIO6				B28
		VCCIO6				H28
		VCCIO6				K24
		VCCIO6				N24
		VCCIO6				N28
		VCCIO7				A16
		VCCIO7				A20
		VCCIO7				A24
		VCCIO7				A27
		VCCIO7				E16
		VCCIO7				E20
		VCCIO7				E23
		VCCIO7				H18
		VCCIO8				A2
		VCCIO8				A5
		VCCIO8				A9
		VCCIO8				A13
		VCCIO8				E6
		VCCIO8				E9
		VCCIO8				E13
		VCCIO8				H11
		VCCA1				Y8
		VCCA2				J21
		VCCA3				J8
		VCCA4				Y21

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
		VCCINT				K9
		VCCINT				K11
		VCCINT				K13
		VCCINT				K15
		VCCINT				K17
		VCCINT				K19
		VCCINT				L10
		VCCINT				L12
		VCCINT				L14
		VCCINT				L16
		VCCINT				L18
		VCCINT				L20
		VCCINT				M9
		VCCINT				M11
		VCCINT				M13
		VCCINT				M15
		VCCINT				M17
		VCCINT				M19
		VCCINT				N10
		VCCINT				N12
		VCCINT				N14
		VCCINT				N16
		VCCINT				N18
		VCCINT				N20
		VCCINT				P9
		VCCINT				P11
		VCCINT				P13
		VCCINT				P15
		VCCINT				P17
		VCCINT				P19
		VCCINT				R10
		VCCINT				R12
		VCCINT				R14
		VCCINT				R16
		VCCINT				R18
		VCCINT				R20
		VCCINT				T9
		VCCINT				T11
		VCCINT				T13
		VCCINT				T15

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F780
		VCCINT				T17
		VCCINT				T19
		VCCINT				U10
		VCCINT				U12
		VCCINT				U14
		VCCINT				U16
		VCCINT				U18
		VCCINT				U20
		VCCINT				V9
		VCCINT				V11
		VCCINT				V13
		VCCINT				V15
		VCCINT				V17
		VCCINT				V19
		VCCINT				W10
		VCCINT				W12
		VCCINT				W14
		VCCINT				W16
		VCCINT				W18
		VCCINT				W20

Notes:

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.

Date	Version	Changes
February 2017	2017.02.13	Initial release.
May 2017	2017.05.19	Updated description for the Configuration pins.
March 2019	2019.03.29	Added DPCLK and CDPCLK support in optional pin function column.