Pin Information for the Intel® Cyclone®10 10CL055 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B1	VREFB1N0	IO			DIFFIO_L1p	G4
B1	VREFB1N0	IO			DIFFIO_L1n	G3
B1	VREFB1N0	IO			DIFFIO_L2p	B2
B1	VREFB1N0	IO			DIFFIO_L2n	B1
B1	VREFB1N0	IO	VREFB1N0			G5
B1	VREFB1N0	IO			DIFFIO_L3p	E4
B1	VREFB1N0	IO			DIFFIO_L3n	E3
B1	VREFB1N0	IO			DIFFIO_L5p	D2
B1	VREFB1N0	IO		DATA1,ASDO	DIFFIO_L5n	D1
B1	VREFB1N0	IO				H7
B1	VREFB1N0	IO			DIFFIO_L6p	H6
B1	VREFB1N0	IO			DIFFIO_L6n	J6
B1	VREFB1N0	IO			DIFFIO_L7p	H4
B1	VREFB1N0	IO			DIFFIO_L7n	H3
B1	VREFB1N0	IO		FLASH_nCE,nCSO	DIFFIO_L8p	E2
B1	VREFB1N0	IO			DIFFIO_L8n	E1
B1	VREFB1N0	IO			DIFFIO_L9p	F2
B1	VREFB1N1	IO			DIFFIO_L9n	F1
B1	VREFB1N1	IO				J5
B1	VREFB1N1	IO	VREFB1N1			H5
B1	VREFB1N1	nSTATUS		nSTATUS		K6
B1	VREFB1N1	IO			DIFFIO_L11p	J7
B1	VREFB1N1	IO			DIFFIO_L11n	K7
B1	VREFB1N1	IO	DPCLK0		DIFFIO_L12p	J4
B1	VREFB1N1	IO			DIFFIO_L13p	H2
B1	VREFB1N1	IO			DIFFIO_L13n	H1
B1	VREFB1N1	IO			DIFFIO_L14n	J3
B1	VREFB1N1	IO			DIFFIO_L15p	J2
B1	VREFB1N1	IO			DIFFIO_L15n	J1
B1	VREFB1N1	IO		DCLK		K2
B1	VREFB1N1	IO		DATA0		K1
B1	VREFB1N1	nCONFIG		nCONFIG		K5
B1	VREFB1N1	TDI		TDI		L5
B1	VREFB1N1	TCK		TCK		L2
B1	VREFB1N1	TMS		TMS		L1
B1	VREFB1N1	TDO		TDO		L4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B1	VREFB1N1	nCE		nCE		L3
B1	VREFB1N1	CLK0	DIFFCLK_0p			G2
B1	VREFB1N1	CLK1	DIFFCLK_0n			G1
B2	VREFB2N0	CLK2	DIFFCLK_1p			T2
B2	VREFB2N0	CLK3	DIFFCLK_1n			T1
B2	VREFB2N0	IO			DIFFIO_L16p	L6
B2	VREFB2N0	IO			DIFFIO_L16n	M6
B2	VREFB2N0	IO			DIFFIO_L17p	M2
B2	VREFB2N0	IO			DIFFIO_L17n	M1
B2	VREFB2N0	IO			DIFFIO_L18p	M4
B2	VREFB2N0	IO			DIFFIO_L18n	M3
B2	VREFB2N0	IO			DIFFIO_L19p	N2
B2	VREFB2N0	IO			DIFFIO_L19n	N1
B2	VREFB2N0	IO	VREFB2N0			M5
B2	VREFB2N0	IO			DIFFIO_L20p	P2
B2	VREFB2N0	IO			DIFFIO_L20n	P1
B2	VREFB2N0	IO			DIFFIO_L21p	R2
B2	VREFB2N0	IO			DIFFIO_L21n	R1
B2	VREFB2N0	IO			DIFFIO_L22n	N5
B2	VREFB2N0	IO	DPCLK1		DIFFIO_L23p	P4
B2	VREFB2N0	IO			DIFFIO_L23n	P3
B2	VREFB2N0	IO			DIFFIO_L24p	U2
B2	VREFB2N0	IO			DIFFIO_L24n	U1
B2	VREFB2N0	IO			DIFFIO_L25p	V2
B2	VREFB2N1	IO			DIFFIO_L25n	V1
B2	VREFB2N1	IO			DIFFIO_L26p	P5
B2	VREFB2N1	IO			DIFFIO_L26n	N6
B2	VREFB2N1	IO			DIFFIO_L27p	R4
B2	VREFB2N1	IO			DIFFIO_L27n	R3
B2	VREFB2N1	IO			DIFFIO_L28p	W2
B2	VREFB2N1	IO			DIFFIO_L28n	W1
B2	VREFB2N1	IO			DIFFIO_L29p	Y2
B2	VREFB2N1	IO			DIFFIO_L29n	Y1
B2	VREFB2N1	IO	VREFB2N1			T3
B2	VREFB2N1	IO			DIFFIO_L30p	N7
B2	VREFB2N1	IO			DIFFIO_L30n	P7

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B2	VREFB2N1	IO	RUP1			V4
B2	VREFB2N1	IO	RDN1			V3
B2	VREFB2N1	IO			DIFFIO_L32p	P6
B2	VREFB2N1	IO			DIFFIO_L32n	R5
B2	VREFB2N1	IO	CDPCLK1			T4
B2	VREFB2N1	IO			DIFFIO_L33p	T5
B2	VREFB2N1	IO			DIFFIO_L33n	R6
B3	VREFB3N1	IO			DIFFIO_B1p	V6
B3	VREFB3N1	IO			DIFFIO_B1n	V5
B3	VREFB3N1	IO			DIFFIO_B2p	U7
B3	VREFB3N1	IO			DIFFIO_B2n	U8
B3	VREFB3N1	IO			DIFFIO_B3p	Y4
B3	VREFB3N1	IO			DIFFIO_B3n	Y3
B3	VREFB3N1	IO	CDPCLK2			Y6
B3	VREFB3N1	IO	PLL1_CLKOUTp			AA3
B3	VREFB3N1	IO	PLL1_CLKOUTn			AB3
B3	VREFB3N1	IO			DIFFIO_B4p	W6
B3	VREFB3N1	IO			DIFFIO_B4n	V7
B3	VREFB3N1	IO				AA4
B3	VREFB3N1	IO	VREFB3N1			AB4
B3	VREFB3N1	IO			DIFFIO_B5p	AA5
B3	VREFB3N1	IO			DIFFIO_B5n	AA6
B3	VREFB3N1	IO			DIFFIO_B6p	AB6
B3	VREFB3N1	IO			DIFFIO_B6n	AB5
B3	VREFB3N1	IO			DIFFIO_B7p	W7
B3	VREFB3N1	IO			DIFFIO_B7n	Y7
B3	VREFB3N1	IO			DIFFIO_B8p	U9
B3	VREFB3N1	IO			DIFFIO_B8n	V8
B3	VREFB3N1	IO				W8
B3	VREFB3N1	IO			DIFFIO_B10p	AA7
B3	VREFB3N1	IO			DIFFIO_B10n	AB7
B3	VREFB3N0	IO			DIFFIO_B11p	Y8
B3	VREFB3N0	IO			DIFFIO_B13p	T10
B3	VREFB3N0	IO			DIFFIO_B13n	T11
B3	VREFB3N0	IO	VREFB3N0			V9
B3	VREFB3N0	IO	DPCLK2		DIFFIO_B15p	V10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B3	VREFB3N0	IO			DIFFIO_B16n	U10
B3	VREFB3N0	IO			DIFFIO_B17p	AA8
B3	VREFB3N0	IO			DIFFIO_B17n	AB8
B3	VREFB3N0	IO			DIFFIO_B18p	AA9
B3	VREFB3N0	IO	DPCLK3		DIFFIO_B18n	AB9
B3	VREFB3N0	IO			DIFFIO_B19p	U11
B3	VREFB3N0	IO			DIFFIO_B19n	V11
B3	VREFB3N0	IO			DIFFIO_B20p	W10
B3	VREFB3N0	IO			DIFFIO_B20n	Y10
B3	VREFB3N0	IO			DIFFIO_B21p	AA10
B3	VREFB3N0	IO			DIFFIO_B21n	AB10
B3	VREFB3N0	CLK15	DIFFCLK_6p			AA11
B3	VREFB3N0	CLK14	DIFFCLK_6n			AB11
B4	VREFB4N1	CLK13	DIFFCLK_7p			AA12
B4	VREFB4N1	CLK12	DIFFCLK_7n			AB12
B4	VREFB4N1	IO			DIFFIO_B23p	AA13
B4	VREFB4N1	IO			DIFFIO_B23n	AB13
B4	VREFB4N1	IO			DIFFIO_B25p	AA14
B4	VREFB4N1	IO			DIFFIO_B25n	AB14
B4	VREFB4N1	IO	VREFB4N1			V12
B4	VREFB4N1	IO			DIFFIO_B26p	W13
B4	VREFB4N1	IO	DPCLK4		DIFFIO_B26n	Y13
B4	VREFB4N1	IO			DIFFIO_B27p	AA15
B4	VREFB4N1	IO			DIFFIO_B27n	AB15
B4	VREFB4N1	IO			DIFFIO_B28p	U12
B4	VREFB4N1	IO			DIFFIO_B29p	Y14
B4	VREFB4N1	IO			DIFFIO_B29n	Y15
B4	VREFB4N1	IO			DIFFIO_B30p	AA16
B4	VREFB4N1	IO			DIFFIO_B30n	AB16
B4	VREFB4N1	IO	DPCLK5		DIFFIO_B31p	V13
B4	VREFB4N1	IO			DIFFIO_B31n	W14
B4	VREFB4N1	IO			DIFFIO_B32p	U13
B4	VREFB4N1	IO			DIFFIO_B33p	V14
B4	VREFB4N0	IO			DIFFIO_B33n	U14
B4	VREFB4N0	IO			DIFFIO_B34p	U15
B4	VREFB4N0	IO			DIFFIO_B34n	V15

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B4	VREFB4N0	IO			DIFFIO_B35p	W15
B4	VREFB4N0	IO			DIFFIO_B36p	T14
B4	VREFB4N0	IO			DIFFIO_B36n	T15
B4	VREFB4N0	IO				AB18
B4	VREFB4N0	IO	VREFB4N0			AA18
B4	VREFB4N0	IO	RUP2			AA19
B4	VREFB4N0	IO	RDN2			AB19
B4	VREFB4N0	IO			DIFFIO_B38p	W17
B4	VREFB4N0	IO	CDPCLK3		DIFFIO_B38n	Y17
B4	VREFB4N0	IO			DIFFIO_B39p	AA20
B4	VREFB4N0	IO			DIFFIO_B39n	AB20
B4	VREFB4N0	IO				V16
B4	VREFB4N0	IO			DIFFIO_B40p	U16
B4	VREFB4N0	IO			DIFFIO_B40n	U17
B4	VREFB4N0	IO	PLL4_CLKOUTp			T16
B4	VREFB4N0	IO	PLL4_CLKOUTn			R16
B4	VREFB4N0	IO			DIFFIO_B41p	R14
B4	VREFB4N0	IO			DIFFIO_B41n	R15
B5	VREFB5N1	IO			DIFFIO_R36n	AA22
B5	VREFB5N1	IO			DIFFIO_R36p	AA21
B5	VREFB5N1	IO	RUP3			T17
B5	VREFB5N1	IO	RDN3			T18
B5	VREFB5N1	IO	CDPCLK4			W20
B5	VREFB5N1	IO	VREFB5N1			W19
B5	VREFB5N1	IO			DIFFIO_R35n	Y22
B5	VREFB5N1	IO			DIFFIO_R35p	Y21
B5	VREFB5N1	IO			DIFFIO_R34n	U20
B5	VREFB5N1	IO			DIFFIO_R34p	U19
B5	VREFB5N1	IO			DIFFIO_R32n	W22
B5	VREFB5N1	IO			DIFFIO_R32p	W21
B5	VREFB5N1	IO			DIFFIO_R31n	T20
B5	VREFB5N1	IO			DIFFIO_R31p	T19
B5	VREFB5N1	IO			DIFFIO_R30n	R17
B5	VREFB5N1	IO			DIFFIO_R30p	P17
B5	VREFB5N1	IO			DIFFIO_R29n	V22
B5	VREFB5N1	IO			DIFFIO_R29p	V21

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B5	VREFB5N1	IO			DIFFIO_R28n	R20
B5	VREFB5N0	IO			DIFFIO_R27n	U22
B5	VREFB5N0	IO			DIFFIO_R27p	U21
B5	VREFB5N0	IO			DIFFIO_R26n	R18
B5	VREFB5N0	IO			DIFFIO_R26p	R19
B5	VREFB5N0	IO			DIFFIO_R25p	N16
B5	VREFB5N0	IO			DIFFIO_R24n	R22
B5	VREFB5N0	IO			DIFFIO_R24p	R21
B5	VREFB5N0	IO	VREFB5N0			P20
B5	VREFB5N0	IO			DIFFIO_R23n	P22
B5	VREFB5N0	IO			DIFFIO_R23p	P21
B5	VREFB5N0	IO			DIFFIO_R22n	N20
B5	VREFB5N0	IO			DIFFIO_R22p	N19
B5	VREFB5N0	IO			DIFFIO_R21n	N17
B5	VREFB5N0	IO	DPCLK6		DIFFIO_R21p	N18
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R20n	N22
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R20p	N21
B5	VREFB5N0	IO			DIFFIO_R19n	M22
B5	VREFB5N0	IO			DIFFIO_R19p	M21
B5	VREFB5N0	IO			DIFFIO_R18n	M20
B5	VREFB5N0	IO			DIFFIO_R18p	M19
B5	VREFB5N0	IO				M16
B5	VREFB5N0	CLK7	DIFFCLK_3n			T22
B5	VREFB5N0	CLK6	DIFFCLK_3p			T21
B6	VREFB6N1	CLK5	DIFFCLK_2n			G22
B6	VREFB6N1	CLK4	DIFFCLK_2p			G21
B6	VREFB6N1	CONF_DONE		CONF_DONE		M18
B6	VREFB6N1	MSEL0		MSEL0		M17
B6	VREFB6N1	MSEL1		MSEL1		L18
B6	VREFB6N1	MSEL2		MSEL2		L17
B6	VREFB6N1	MSEL3		MSEL3		K20
B6	VREFB6N1	IO		INIT_DONE	DIFFIO_R17n	L22
B6	VREFB6N1	IO		CRC_ERROR	DIFFIO_R17p	L21
B6	VREFB6N1	IO	VREFB6N1			K19
B6	VREFB6N1	IO		nCEO	DIFFIO_R16n	K22
B6	VREFB6N1	IO		CLKUSR	DIFFIO_R16p	K21

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B6	VREFB6N1	IO	DPCLK7		DIFFIO_R15n	J22
B6	VREFB6N1	IO			DIFFIO_R15p	J21
B6	VREFB6N1	IO			DIFFIO_R14n	H22
B6	VREFB6N1	IO			DIFFIO_R14p	H21
B6	VREFB6N1	IO			DIFFIO_R13n	K17
B6	VREFB6N1	IO			DIFFIO_R13p	K18
B6	VREFB6N1	IO			DIFFIO_R12n	J18
B6	VREFB6N1	IO			DIFFIO_R11n	F22
B6	VREFB6N1	IO			DIFFIO_R11p	F21
B6	VREFB6N1	IO			DIFFIO_R10n	J20
B6	VREFB6N1	IO			DIFFIO_R10p	J19
B6	VREFB6N0	IO				J17
B6	VREFB6N0	IO			DIFFIO_R9n	H20
B6	VREFB6N0	IO			DIFFIO_R9p	H19
B6	VREFB6N0	IO			DIFFIO_R8n	E22
B6	VREFB6N0	IO			DIFFIO_R8p	E21
B6	VREFB6N0	IO	VREFB6N0			H18
B6	VREFB6N0	IO				H16
B6	VREFB6N0	IO			DIFFIO_R7n	D22
B6	VREFB6N0	IO			DIFFIO_R7p	D21
B6	VREFB6N0	IO			DIFFIO_R6n	F20
B6	VREFB6N0	IO			DIFFIO_R6p	F19
B6	VREFB6N0	IO			DIFFIO_R5n	G18
B6	VREFB6N0	IO			DIFFIO_R5p	H17
B6	VREFB6N0	IO			DIFFIO_R4n	C22
B6	VREFB6N0	IO			DIFFIO_R4p	C21
B6	VREFB6N0	IO			DIFFIO_R3n	B22
B6	VREFB6N0	IO			DIFFIO_R3p	B21
B6	VREFB6N0	IO	CDPCLK5		DIFFIO_R2n	C20
B6	VREFB6N0	IO			DIFFIO_R2p	D20
B6	VREFB6N0	IO			DIFFIO_R1n	F17
B6	VREFB6N0	IO			DIFFIO_R1p	G17
B7	VREFB7N0	IO			DIFFIO_T42n	F16
B7	VREFB7N0	IO			DIFFIO_T42p	E16
B7	VREFB7N0	IO			DIFFIO_T41n	F15
B7	VREFB7N0	IO			DIFFIO_T41p	G16

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B7	VREFB7N0	IO			DIFFIO_T40n	G15
B7	VREFB7N0	IO	CDPCLK6		DIFFIO_T40p	F14
B7	VREFB7N0	IO			DIFFIO_T39n	C18
B7	VREFB7N0	IO			DIFFIO_T39p	D18
B7	VREFB7N0	IO	VREFB7N0			D17
B7	VREFB7N0	IO			DIFFIO_T37n	C19
B7	VREFB7N0	IO			DIFFIO_T37p	D19
B7	VREFB7N0	IO	PLL2_CLKOUTn			A20
B7	VREFB7N0	IO	PLL2_CLKOUTp			B20
B7	VREFB7N0	IO			DIFFIO_T35p	C17
B7	VREFB7N0	IO	RUP4			B19
B7	VREFB7N0	IO	RDN4			A19
B7	VREFB7N0	IO			DIFFIO_T34n	A18
B7	VREFB7N0	IO			DIFFIO_T34p	B18
B7	VREFB7N0	IO			DIFFIO_T33n	D15
B7	VREFB7N1	IO			DIFFIO_T33p	E15
B7	VREFB7N1	IO			DIFFIO_T32n	G14
B7	VREFB7N1	IO			DIFFIO_T32p	G13
B7	VREFB7N1	IO			DIFFIO_T31n	A17
B7	VREFB7N1	IO			DIFFIO_T31p	B17
B7	VREFB7N1	IO			DIFFIO_T30n	A16
B7	VREFB7N1	IO			DIFFIO_T30p	B16
B7	VREFB7N1	IO	VREFB7N1			C15
B7	VREFB7N1	IO			DIFFIO_T28n	E14
B7	VREFB7N1	IO	DPCLK8		DIFFIO_T28p	F13
B7	VREFB7N1	IO			DIFFIO_T27n	A15
B7	VREFB7N1	IO			DIFFIO_T27p	B15
B7	VREFB7N1	IO			DIFFIO_T26n	C13
B7	VREFB7N1	IO			DIFFIO_T26p	D13
B7	VREFB7N1	IO				E13
B7	VREFB7N1	IO			DIFFIO_T25n	A14
B7	VREFB7N1	IO			DIFFIO_T25p	B14
B7	VREFB7N1	IO			DIFFIO_T24n	A13
B7	VREFB7N1	IO	DPCLK9		DIFFIO_T24p	B13
B7	VREFB7N1	IO				E12
B7	VREFB7N1	IO			DIFFIO_T23n	E11

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B7	VREFB7N1	IO			DIFFIO_T23p	F11
B7	VREFB7N1	CLK8	DIFFCLK_5n			A12
B7	VREFB7N1	CLK9	DIFFCLK_5p			B12
B8	VREFB8N0	CLK10	DIFFCLK_4n			A11
B8	VREFB8N0	CLK11	DIFFCLK_4p			B11
B8	VREFB8N0	IO			DIFFIO_T22n	D10
B8	VREFB8N0	IO			DIFFIO_T22p	E10
B8	VREFB8N0	IO			DIFFIO_T21n	A10
B8	VREFB8N0	IO			DIFFIO_T21p	B10
B8	VREFB8N0	IO			DIFFIO_T20n	A9
B8	VREFB8N0	IO	DPCLK10		DIFFIO_T20p	B9
B8	VREFB8N0	IO	VREFB8N0			C10
B8	VREFB8N0	IO			DIFFIO_T18n	G11
B8	VREFB8N0	IO		DATA2	DIFFIO_T17n	A8
B8	VREFB8N0	IO		DATA3	DIFFIO_T17p	B8
B8	VREFB8N0	IO			DIFFIO_T16n	A7
B8	VREFB8N0	IO		DATA4	DIFFIO_T16p	B7
B8	VREFB8N0	IO			DIFFIO_T15n	A6
B8	VREFB8N0	IO			DIFFIO_T15p	B6
B8	VREFB8N0	IO			DIFFIO_T14n	E9
B8	VREFB8N0	IO	DPCLK11		DIFFIO_T13n	C8
B8	VREFB8N0	IO			DIFFIO_T13p	C7
B8	VREFB8N0	IO			DIFFIO_T12n	D8
B8	VREFB8N0	IO			DIFFIO_T12p	E8
B8	VREFB8N1	IO		DATA5	DIFFIO_T11p	A5
B8	VREFB8N1	IO	VREFB8N1			B5
B8	VREFB8N1	IO			DIFFIO_T10n	G10
B8	VREFB8N1	IO		DATA6	DIFFIO_T10p	F10
B8	VREFB8N1	IO		DATA7	DIFFIO_T9n	C6
B8	VREFB8N1	IO			DIFFIO_T9p	D7
B8	VREFB8N1	IO			DIFFIO_T8n	A4
B8	VREFB8N1	IO			DIFFIO_T8p	B4
B8	VREFB8N1	IO			DIFFIO_T7n	F8
B8	VREFB8N1	IO			DIFFIO_T7p	G8
B8	VREFB8N1	IO			DIFFIO_T5n	A3
B8	VREFB8N1	IO			DIFFIO_T5p	B3

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B8	VREFB8N1	IO			DIFFIO_T4n	D6
B8	VREFB8N1	IO			DIFFIO_T4p	E7
B8	VREFB8N1	IO			DIFFIO_T3n	C3
B8	VREFB8N1	IO	CDPCLK7		DIFFIO_T3p	C4
B8	VREFB8N1	IO			DIFFIO_T2n	F7
B8	VREFB8N1	IO			DIFFIO_T2p	G7
B8	VREFB8N1	IO				F9
B8	VREFB8N1	IO	PLL3_CLKOUTn			E6
B8	VREFB8N1	IO	PLL3_CLKOUTp			E5
B8	VREFB8N1	IO			DIFFIO_T1n	G9
		GND				L10
		GND				L11
		GND				M10
		GND				M11
		GND				L12
		GND				L13
		GND				M12
		GND				M13
		GND				N11
		GND				K11
		GND				N12
		GND				K12
		GND				K13
		GND				N13
		GND				N10
		GND				K10
		GND				J9
		GND				F12
		GND				H12
		GND				H13
		GND				J15
		GND				K16
		GND				L15
		GND				N15
		GND				R13
		GND				R11

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		GND				R9
		GND				P8
		GND				H14
		GND				H10
		GND				H8
		GND				N8
		GND				R7
		GND				T8
		GND				T12
		GND				P16
		GND				L8
		GND				M7
		GND				A1
		GND				C5
		GND				C9
		GND				C11
		GND				C12
		GND				C14
		GND				C16
		GND				A22
		GND				E20
		GND				G20
		GND				L20
		GND				P19
		GND				V20
		GND				Y20
		GND				AB22
		GND				Y18
		GND				Y16
		GND				Y12
		GND				Y11
		GND				Y9
		GND				Y5
		GND				AB1
		GND				N3
		GND				U3

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		GND				W3
		GND				D3
		GND				F3
		GND				K3
		GND				AA2
		GND				AA1
		GND				C1
		GND				C2
		GND				AA17
		GND				AB17
		GNDA1				U5
		GNDA2				E18
		GNDA3				F5
		GNDA4				V18
		VCCD_PLL1				U6
		VCCD_PLL2				E17
		VCCD_PLL3				F6
		VCCD_PLL4				V17
		VCCIO1				D4
		VCCIO1				F4
		VCCIO1				K4
		VCCIO2				N4
		VCCIO2				U4
		VCCIO2				W4
		VCCIO3				AB2
		VCCIO3				W5
		VCCIO3				W9
		VCCIO3				W11
		VCCIO4				AB21
		VCCIO4				W12
		VCCIO4				W16
		VCCIO4				W18
		VCCIO5				P18
		VCCIO5				V19
		VCCIO5				Y19
		VCCIO6				E19

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		VCCIO6				G19
		VCCIO6				L19
		VCCIO7				A21
		VCCIO7				D12
		VCCIO7				D14
		VCCIO7				D16
		VCCIO8				A2
		VCCIO8				D5
		VCCIO8				D9
		VCCIO8				D11
		VCCA1				T6
		VCCA2				F18
		VCCA3				G6
		VCCA4				U18
		VCCINT				J11
		VCCINT				J12
		VCCINT				L14
		VCCINT				M14
		VCCINT				P11
		VCCINT				P12
		VCCINT				L9
		VCCINT				M9
		VCCINT				J13
		VCCINT				J14
		VCCINT				K14
		VCCINT				J10
		VCCINT				K9
		VCCINT				N9
		VCCINT				P9
		VCCINT				P10
		VCCINT				P13
		VCCINT				P14
		VCCINT				N14
		VCCINT				J16
		VCCINT				K15
		VCCINT				L16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		VCCINT				M15
		VCCINT				R12
		VCCINT				R10
		VCCINT				R8
		VCCINT				H9
		VCCINT				G12
		VCCINT				J8
		VCCINT				M8
		VCCINT				T7
		VCCINT				T9
		VCCINT				T13
		VCCINT				P15
		VCCINT				H15
		VCCINT				H11
		VCCINT				K8
		VCCINT				L7

Notes:

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.

Pin Information for the Intel® Cyclone®10 10CL055 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B1	VREFB1N0	IO			DIFFIO_L1p	G4
B1	VREFB1N0	IO			DIFFIO_L1n	G3
B1	VREFB1N0	IO			DIFFIO_L2p	B2
B1	VREFB1N0	IO			DIFFIO_L2n	B1
B1	VREFB1N0	IO	VREFB1N0			G5
B1	VREFB1N0	IO			DIFFIO_L3p	E4
B1	VREFB1N0	IO			DIFFIO_L3n	E3
B1	VREFB1N0	IO			DIFFIO_L5p	D2
B1	VREFB1N0	IO		DATA1,ASDO	DIFFIO_L5n	D1
B1	VREFB1N0	IO				H7
B1	VREFB1N0	IO			DIFFIO_L6p	H6
B1	VREFB1N0	IO			DIFFIO_L6n	J6
B1	VREFB1N0	IO			DIFFIO_L7p	H4
B1	VREFB1N0	IO			DIFFIO_L7n	H3
B1	VREFB1N0	IO		FLASH_nCE,nCSO	DIFFIO_L8p	E2
B1	VREFB1N0	IO			DIFFIO_L8n	E1
B1	VREFB1N0	IO			DIFFIO_L9p	F2
B1	VREFB1N1	IO			DIFFIO_L9n	F1
B1	VREFB1N1	IO				J5
B1	VREFB1N1	IO	VREFB1N1			H5
B1	VREFB1N1	nSTATUS		nSTATUS		K6
B1	VREFB1N1	IO			DIFFIO_L11p	J7
B1	VREFB1N1	IO			DIFFIO_L11n	K7
B1	VREFB1N1	IO	DPCLK0		DIFFIO_L12p	J4
B1	VREFB1N1	IO			DIFFIO_L13p	H2
B1	VREFB1N1	IO			DIFFIO_L13n	H1
B1	VREFB1N1	IO			DIFFIO_L14n	J3
B1	VREFB1N1	IO			DIFFIO_L15p	J2
B1	VREFB1N1	IO			DIFFIO_L15n	J1
B1	VREFB1N1	IO		DCLK		K2
B1	VREFB1N1	IO		DATA0		K1
B1	VREFB1N1	nCONFIG		nCONFIG		K5
B1	VREFB1N1	TDI		TDI		L5
B1	VREFB1N1	TCK		TCK		L2
B1	VREFB1N1	TMS		TMS		L1
B1	VREFB1N1	TDO		TDO		L4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B1	VREFB1N1	nCE		nCE		L3
B1	VREFB1N1	CLK0	DIFFCLK_0p			G2
B1	VREFB1N1	CLK1	DIFFCLK_0n			G1
B2	VREFB2N0	CLK2	DIFFCLK_1p			T2
B2	VREFB2N0	CLK3	DIFFCLK_1n			T1
B2	VREFB2N0	IO			DIFFIO_L16p	L6
B2	VREFB2N0	IO			DIFFIO_L16n	M6
B2	VREFB2N0	IO			DIFFIO_L17p	M2
B2	VREFB2N0	IO			DIFFIO_L17n	M1
B2	VREFB2N0	IO			DIFFIO_L18p	M4
B2	VREFB2N0	IO			DIFFIO_L18n	M3
B2	VREFB2N0	IO			DIFFIO_L19p	N2
B2	VREFB2N0	IO			DIFFIO_L19n	N1
B2	VREFB2N0	IO	VREFB2N0			M5
B2	VREFB2N0	IO			DIFFIO_L20p	P2
B2	VREFB2N0	IO			DIFFIO_L20n	P1
B2	VREFB2N0	IO			DIFFIO_L21p	R2
B2	VREFB2N0	IO			DIFFIO_L21n	R1
B2	VREFB2N0	IO			DIFFIO_L22n	N5
B2	VREFB2N0	IO	DPCLK1		DIFFIO_L23p	P4
B2	VREFB2N0	IO			DIFFIO_L23n	P3
B2	VREFB2N0	IO			DIFFIO_L24p	U2
B2	VREFB2N0	IO			DIFFIO_L24n	U1
B2	VREFB2N0	IO			DIFFIO_L25p	V2
B2	VREFB2N1	IO			DIFFIO_L25n	V1
B2	VREFB2N1	IO			DIFFIO_L26p	P5
B2	VREFB2N1	IO			DIFFIO_L26n	N6
B2	VREFB2N1	IO			DIFFIO_L27p	R4
B2	VREFB2N1	IO			DIFFIO_L27n	R3
B2	VREFB2N1	IO			DIFFIO_L28p	W2
B2	VREFB2N1	IO			DIFFIO_L28n	W1
B2	VREFB2N1	IO			DIFFIO_L29p	Y2
B2	VREFB2N1	IO			DIFFIO_L29n	Y1
B2	VREFB2N1	IO	VREFB2N1			T3
B2	VREFB2N1	IO			DIFFIO_L30p	N7
B2	VREFB2N1	IO			DIFFIO_L30n	P7

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B2	VREFB2N1	IO	RUP1			V4
B2	VREFB2N1	IO	RDN1			V3
B2	VREFB2N1	IO			DIFFIO_L32p	P6
B2	VREFB2N1	IO			DIFFIO_L32n	R5
B2	VREFB2N1	IO	CDPCLK1			T4
B2	VREFB2N1	IO			DIFFIO_L33p	T5
B2	VREFB2N1	IO			DIFFIO_L33n	R6
B3	VREFB3N1	IO			DIFFIO_B1p	V6
B3	VREFB3N1	IO			DIFFIO_B1n	V5
B3	VREFB3N1	IO			DIFFIO_B2p	U7
B3	VREFB3N1	IO			DIFFIO_B2n	U8
B3	VREFB3N1	IO			DIFFIO_B3p	Y4
B3	VREFB3N1	IO			DIFFIO_B3n	Y3
B3	VREFB3N1	IO	CDPCLK2			Y6
B3	VREFB3N1	IO	PLL1_CLKOUTp			AA3
B3	VREFB3N1	IO	PLL1_CLKOUTn			AB3
B3	VREFB3N1	IO			DIFFIO_B4p	W6
B3	VREFB3N1	IO			DIFFIO_B4n	V7
B3	VREFB3N1	IO				AA4
B3	VREFB3N1	IO	VREFB3N1			AB4
B3	VREFB3N1	IO			DIFFIO_B5p	AA5
B3	VREFB3N1	IO			DIFFIO_B5n	AA6
B3	VREFB3N1	IO			DIFFIO_B6p	AB6
B3	VREFB3N1	IO			DIFFIO_B6n	AB5
B3	VREFB3N1	IO			DIFFIO_B7p	W7
B3	VREFB3N1	IO			DIFFIO_B7n	Y7
B3	VREFB3N1	IO			DIFFIO_B8p	U9
B3	VREFB3N1	IO			DIFFIO_B8n	V8
B3	VREFB3N1	IO				W8
B3	VREFB3N1	IO			DIFFIO_B10p	AA7
B3	VREFB3N1	IO			DIFFIO_B10n	AB7
B3	VREFB3N0	IO			DIFFIO_B11p	Y8
B3	VREFB3N0	IO			DIFFIO_B13p	T10
B3	VREFB3N0	IO			DIFFIO_B13n	T11
B3	VREFB3N0	IO	VREFB3N0			V9
B3	VREFB3N0	IO	DPCLK2		DIFFIO_B15p	V10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B3	VREFB3N0	IO			DIFFIO_B16n	U10
B3	VREFB3N0	IO			DIFFIO_B17p	AA8
B3	VREFB3N0	IO			DIFFIO_B17n	AB8
B3	VREFB3N0	IO			DIFFIO_B18p	AA9
B3	VREFB3N0	IO	DPCLK3		DIFFIO_B18n	AB9
B3	VREFB3N0	IO			DIFFIO_B19p	U11
B3	VREFB3N0	IO			DIFFIO_B19n	V11
B3	VREFB3N0	IO			DIFFIO_B20p	W10
B3	VREFB3N0	IO			DIFFIO_B20n	Y10
B3	VREFB3N0	IO			DIFFIO_B21p	AA10
B3	VREFB3N0	IO			DIFFIO_B21n	AB10
B3	VREFB3N0	CLK15	DIFFCLK_6p			AA11
B3	VREFB3N0	CLK14	DIFFCLK_6n			AB11
B4	VREFB4N1	CLK13	DIFFCLK_7p			AA12
B4	VREFB4N1	CLK12	DIFFCLK_7n			AB12
B4	VREFB4N1	IO			DIFFIO_B23p	AA13
B4	VREFB4N1	IO			DIFFIO_B23n	AB13
B4	VREFB4N1	IO			DIFFIO_B25p	AA14
B4	VREFB4N1	IO			DIFFIO_B25n	AB14
B4	VREFB4N1	IO	VREFB4N1			V12
B4	VREFB4N1	IO			DIFFIO_B26p	W13
B4	VREFB4N1	IO	DPCLK4		DIFFIO_B26n	Y13
B4	VREFB4N1	IO			DIFFIO_B27p	AA15
B4	VREFB4N1	IO			DIFFIO_B27n	AB15
B4	VREFB4N1	IO			DIFFIO_B28p	U12
B4	VREFB4N1	IO			DIFFIO_B29p	Y14
B4	VREFB4N1	IO			DIFFIO_B29n	Y15
B4	VREFB4N1	IO			DIFFIO_B30p	AA16
B4	VREFB4N1	IO			DIFFIO_B30n	AB16
B4	VREFB4N1	IO	DPCLK5		DIFFIO_B31p	V13
B4	VREFB4N1	IO			DIFFIO_B31n	W14
B4	VREFB4N1	IO			DIFFIO_B32p	U13
B4	VREFB4N1	IO			DIFFIO_B33p	V14
B4	VREFB4N0	IO			DIFFIO_B33n	U14
B4	VREFB4N0	IO			DIFFIO_B34p	U15
B4	VREFB4N0	IO			DIFFIO_B34n	V15

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B4	VREFB4N0	IO			DIFFIO_B35p	W15
B4	VREFB4N0	IO			DIFFIO_B36p	T14
B4	VREFB4N0	IO			DIFFIO_B36n	T15
B4	VREFB4N0	IO				AB18
B4	VREFB4N0	IO	VREFB4N0			AA18
B4	VREFB4N0	IO	RUP2			AA19
B4	VREFB4N0	IO	RDN2			AB19
B4	VREFB4N0	IO			DIFFIO_B38p	W17
B4	VREFB4N0	IO	CDPCLK3		DIFFIO_B38n	Y17
B4	VREFB4N0	IO			DIFFIO_B39p	AA20
B4	VREFB4N0	IO			DIFFIO_B39n	AB20
B4	VREFB4N0	IO				V16
B4	VREFB4N0	IO			DIFFIO_B40p	U16
B4	VREFB4N0	IO			DIFFIO_B40n	U17
B4	VREFB4N0	IO	PLL4_CLKOUTp			T16
B4	VREFB4N0	IO	PLL4_CLKOUTn			R16
B4	VREFB4N0	IO			DIFFIO_B41p	R14
B4	VREFB4N0	IO			DIFFIO_B41n	R15
B5	VREFB5N1	IO			DIFFIO_R36n	AA22
B5	VREFB5N1	IO			DIFFIO_R36p	AA21
B5	VREFB5N1	IO	RUP3			T17
B5	VREFB5N1	IO	RDN3			T18
B5	VREFB5N1	IO	CDPCLK4			W20
B5	VREFB5N1	IO	VREFB5N1			W19
B5	VREFB5N1	IO			DIFFIO_R35n	Y22
B5	VREFB5N1	IO			DIFFIO_R35p	Y21
B5	VREFB5N1	IO			DIFFIO_R34n	U20
B5	VREFB5N1	IO			DIFFIO_R34p	U19
B5	VREFB5N1	IO			DIFFIO_R32n	W22
B5	VREFB5N1	IO			DIFFIO_R32p	W21
B5	VREFB5N1	IO			DIFFIO_R31n	T20
B5	VREFB5N1	IO			DIFFIO_R31p	T19
B5	VREFB5N1	IO			DIFFIO_R30n	R17
B5	VREFB5N1	IO			DIFFIO_R30p	P17
B5	VREFB5N1	IO			DIFFIO_R29n	V22
B5	VREFB5N1	IO			DIFFIO_R29p	V21

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B5	VREFB5N1	IO			DIFFIO_R28n	R20
B5	VREFB5N0	IO			DIFFIO_R27n	U22
B5	VREFB5N0	IO			DIFFIO_R27p	U21
B5	VREFB5N0	IO			DIFFIO_R26n	R18
B5	VREFB5N0	IO			DIFFIO_R26p	R19
B5	VREFB5N0	IO			DIFFIO_R25p	N16
B5	VREFB5N0	IO			DIFFIO_R24n	R22
B5	VREFB5N0	IO			DIFFIO_R24p	R21
B5	VREFB5N0	IO	VREFB5N0			P20
B5	VREFB5N0	IO			DIFFIO_R23n	P22
B5	VREFB5N0	IO			DIFFIO_R23p	P21
B5	VREFB5N0	IO			DIFFIO_R22n	N20
B5	VREFB5N0	IO			DIFFIO_R22p	N19
B5	VREFB5N0	IO			DIFFIO_R21n	N17
B5	VREFB5N0	IO	DPCLK6		DIFFIO_R21p	N18
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R20n	N22
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R20p	N21
B5	VREFB5N0	IO			DIFFIO_R19n	M22
B5	VREFB5N0	IO			DIFFIO_R19p	M21
B5	VREFB5N0	IO			DIFFIO_R18n	M20
B5	VREFB5N0	IO			DIFFIO_R18p	M19
B5	VREFB5N0	IO				M16
B5	VREFB5N0	CLK7	DIFFCLK_3n			T22
B5	VREFB5N0	CLK6	DIFFCLK_3p			T21
B6	VREFB6N1	CLK5	DIFFCLK_2n			G22
B6	VREFB6N1	CLK4	DIFFCLK_2p			G21
B6	VREFB6N1	CONF_DONE		CONF_DONE		M18
B6	VREFB6N1	MSEL0		MSEL0		M17
B6	VREFB6N1	MSEL1		MSEL1		L18
B6	VREFB6N1	MSEL2		MSEL2		L17
B6	VREFB6N1	MSEL3		MSEL3		K20
B6	VREFB6N1	IO		INIT_DONE	DIFFIO_R17n	L22
B6	VREFB6N1	IO		CRC_ERROR	DIFFIO_R17p	L21
B6	VREFB6N1	IO	VREFB6N1			K19
B6	VREFB6N1	IO		nCEO	DIFFIO_R16n	K22
B6	VREFB6N1	IO		CLKUSR	DIFFIO_R16p	K21

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B6	VREFB6N1	IO	DPCLK7		DIFFIO_R15n	J22
B6	VREFB6N1	IO			DIFFIO_R15p	J21
B6	VREFB6N1	IO			DIFFIO_R14n	H22
B6	VREFB6N1	IO			DIFFIO_R14p	H21
B6	VREFB6N1	IO			DIFFIO_R13n	K17
B6	VREFB6N1	IO			DIFFIO_R13p	K18
B6	VREFB6N1	IO			DIFFIO_R12n	J18
B6	VREFB6N1	IO			DIFFIO_R11n	F22
B6	VREFB6N1	IO			DIFFIO_R11p	F21
B6	VREFB6N1	IO			DIFFIO_R10n	J20
B6	VREFB6N1	IO			DIFFIO_R10p	J19
B6	VREFB6N0	IO				J17
B6	VREFB6N0	IO			DIFFIO_R9n	H20
B6	VREFB6N0	IO			DIFFIO_R9p	H19
B6	VREFB6N0	IO			DIFFIO_R8n	E22
B6	VREFB6N0	IO			DIFFIO_R8p	E21
B6	VREFB6N0	IO	VREFB6N0			H18
B6	VREFB6N0	IO				H16
B6	VREFB6N0	IO			DIFFIO_R7n	D22
B6	VREFB6N0	IO			DIFFIO_R7p	D21
B6	VREFB6N0	IO			DIFFIO_R6n	F20
B6	VREFB6N0	IO			DIFFIO_R6p	F19
B6	VREFB6N0	IO			DIFFIO_R5n	G18
B6	VREFB6N0	IO			DIFFIO_R5p	H17
B6	VREFB6N0	IO			DIFFIO_R4n	C22
B6	VREFB6N0	IO			DIFFIO_R4p	C21
B6	VREFB6N0	IO			DIFFIO_R3n	B22
B6	VREFB6N0	IO			DIFFIO_R3p	B21
B6	VREFB6N0	IO	CDPCLK5		DIFFIO_R2n	C20
B6	VREFB6N0	IO			DIFFIO_R2p	D20
B6	VREFB6N0	IO			DIFFIO_R1n	F17
B6	VREFB6N0	IO			DIFFIO_R1p	G17
B7	VREFB7N0	IO			DIFFIO_T42n	F16
B7	VREFB7N0	IO			DIFFIO_T42p	E16
B7	VREFB7N0	IO			DIFFIO_T41n	F15
B7	VREFB7N0	IO			DIFFIO_T41p	G16

Pin Information for the Intel® Cyclone®10 10CL055 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B7	VREFB7N0	IO			DIFFIO_T40n	G15
B7	VREFB7N0	IO	CDPCLK6		DIFFIO_T40p	F14
B7	VREFB7N0	IO			DIFFIO_T39n	C18
B7	VREFB7N0	IO			DIFFIO_T39p	D18
B7	VREFB7N0	IO	VREFB7N0			D17
B7	VREFB7N0	IO			DIFFIO_T37n	C19
B7	VREFB7N0	IO			DIFFIO_T37p	D19
B7	VREFB7N0	IO	PLL2_CLKOUTn			A20
B7	VREFB7N0	IO	PLL2_CLKOUTp			B20
B7	VREFB7N0	IO			DIFFIO_T35p	C17
B7	VREFB7N0	IO	RUP4			B19
B7	VREFB7N0	IO	RDN4			A19
B7	VREFB7N0	IO			DIFFIO_T34n	A18
B7	VREFB7N0	IO			DIFFIO_T34p	B18
B7	VREFB7N0	IO			DIFFIO_T33n	D15
B7	VREFB7N1	IO			DIFFIO_T33p	E15
B7	VREFB7N1	IO			DIFFIO_T32n	G14
B7	VREFB7N1	IO			DIFFIO_T32p	G13
B7	VREFB7N1	IO			DIFFIO_T31n	A17
B7	VREFB7N1	IO			DIFFIO_T31p	B17
B7	VREFB7N1	IO			DIFFIO_T30n	A16
B7	VREFB7N1	IO			DIFFIO_T30p	B16
B7	VREFB7N1	IO	VREFB7N1			C15
B7	VREFB7N1	IO			DIFFIO_T28n	E14
B7	VREFB7N1	IO	DPCLK8		DIFFIO_T28p	F13
B7	VREFB7N1	IO			DIFFIO_T27n	A15
B7	VREFB7N1	IO			DIFFIO_T27p	B15
B7	VREFB7N1	IO			DIFFIO_T26n	C13
B7	VREFB7N1	IO			DIFFIO_T26p	D13
B7	VREFB7N1	IO				E13
B7	VREFB7N1	IO			DIFFIO_T25n	A14
B7	VREFB7N1	IO			DIFFIO_T25p	B14
B7	VREFB7N1	IO			DIFFIO_T24n	A13
B7	VREFB7N1	IO	DPCLK9		DIFFIO_T24p	B13
B7	VREFB7N1	IO				E12
B7	VREFB7N1	IO			DIFFIO_T23n	E11

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B7	VREFB7N1	IO			DIFFIO_T23p	F11
B7	VREFB7N1	CLK8	DIFFCLK_5n			A12
B7	VREFB7N1	CLK9	DIFFCLK_5p			B12
B8	VREFB8N0	CLK10	DIFFCLK_4n			A11
B8	VREFB8N0	CLK11	DIFFCLK_4p			B11
B8	VREFB8N0	IO			DIFFIO_T22n	D10
B8	VREFB8N0	IO			DIFFIO_T22p	E10
B8	VREFB8N0	IO			DIFFIO_T21n	A10
B8	VREFB8N0	IO			DIFFIO_T21p	B10
B8	VREFB8N0	IO			DIFFIO_T20n	A9
B8	VREFB8N0	IO	DPCLK10		DIFFIO_T20p	B9
B8	VREFB8N0	IO	VREFB8N0			C10
B8	VREFB8N0	IO			DIFFIO_T18n	G11
B8	VREFB8N0	IO		DATA2	DIFFIO_T17n	A8
B8	VREFB8N0	IO		DATA3	DIFFIO_T17p	B8
B8	VREFB8N0	IO			DIFFIO_T16n	A7
B8	VREFB8N0	IO		DATA4	DIFFIO_T16p	B7
B8	VREFB8N0	IO			DIFFIO_T15n	A6
B8	VREFB8N0	IO			DIFFIO_T15p	B6
B8	VREFB8N0	IO			DIFFIO_T14n	E9
B8	VREFB8N0	IO	DPCLK11		DIFFIO_T13n	C8
B8	VREFB8N0	IO			DIFFIO_T13p	C7
B8	VREFB8N0	IO			DIFFIO_T12n	D8
B8	VREFB8N0	IO			DIFFIO_T12p	E8
B8	VREFB8N1	IO		DATA5	DIFFIO_T11p	A5
B8	VREFB8N1	IO	VREFB8N1			B5
B8	VREFB8N1	IO			DIFFIO_T10n	G10
B8	VREFB8N1	IO		DATA6	DIFFIO_T10p	F10
B8	VREFB8N1	IO		DATA7	DIFFIO_T9n	C6
B8	VREFB8N1	IO			DIFFIO_T9p	D7
B8	VREFB8N1	IO			DIFFIO_T8n	A4
B8	VREFB8N1	IO			DIFFIO_T8p	B4
B8	VREFB8N1	IO			DIFFIO_T7n	F8
B8	VREFB8N1	IO			DIFFIO_T7p	G8
B8	VREFB8N1	IO			DIFFIO_T5n	A3
B8	VREFB8N1	IO			DIFFIO_T5p	B3

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B8	VREFB8N1	IO			DIFFIO_T4n	D6
B8	VREFB8N1	IO			DIFFIO_T4p	E7
B8	VREFB8N1	IO			DIFFIO_T3n	C3
B8	VREFB8N1	IO	CDPCLK7		DIFFIO_T3p	C4
B8	VREFB8N1	IO			DIFFIO_T2n	F7
B8	VREFB8N1	IO			DIFFIO_T2p	G7
B8	VREFB8N1	IO				F9
B8	VREFB8N1	IO	PLL3_CLKOUTn			E6
B8	VREFB8N1	IO	PLL3_CLKOUTp			E5
B8	VREFB8N1	IO			DIFFIO_T1n	G9
		GND				L10
		GND				L11
		GND				M10
		GND				M11
		GND				L12
		GND				L13
		GND				M12
		GND				M13
		GND				N11
		GND				K11
		GND				N12
		GND				K12
		GND				K13
		GND				N13
		GND				N10
		GND				K10
		GND				J9
		GND				F12
		GND				H12
		GND				H13
		GND				J15
		GND				K16
		GND				L15
		GND				N15
		GND				R13
		GND				R11

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		GND				R9
		GND				P8
		GND				H14
		GND				H10
		GND				H8
		GND				N8
		GND				R7
		GND				T8
		GND				T12
		GND				P16
		GND				L8
		GND				M7
		GND				A1
		GND				C5
		GND				C9
		GND				C11
		GND				C12
		GND				C14
		GND				C16
		GND				A22
		GND				E20
		GND				G20
		GND				L20
		GND				P19
		GND				V20
		GND				Y20
		GND				AB22
		GND				Y18
		GND				Y16
		GND				Y12
		GND				Y11
		GND				Y9
		GND				Y5
		GND				AB1
		GND				N3
		GND				U3

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		GND				W3
		GND				D3
		GND				F3
		GND				K3
		GND				AA2
		GND				AA1
		GND				C1
		GND				C2
		GND				AA17
		GND				AB17
		GNDA1				U5
		GNDA2				E18
		GNDA3				F5
		GNDA4				V18
		VCCD_PLL1				U6
		VCCD_PLL2				E17
		VCCD_PLL3				F6
		VCCD_PLL4				V17
		VCCIO1				D4
		VCCIO1				F4
		VCCIO1				K4
		VCCIO2				N4
		VCCIO2				U4
		VCCIO2				W4
		VCCIO3				AB2
		VCCIO3				W5
		VCCIO3				W9
		VCCIO3				W11
		VCCIO4				AB21
		VCCIO4				W12
		VCCIO4				W16
		VCCIO4				W18
		VCCIO5				P18
		VCCIO5				V19
		VCCIO5				Y19
		VCCIO6				E19

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		VCCIO6				G19
		VCCIO6				L19
		VCCIO7				A21
		VCCIO7				D12
		VCCIO7				D14
		VCCIO7				D16
		VCCIO8				A2
		VCCIO8				D5
		VCCIO8				D9
		VCCIO8				D11
		VCCA1				T6
		VCCA2				F18
		VCCA3				G6
		VCCA4				U18
		VCCINT				J11
		VCCINT				J12
		VCCINT				L14
		VCCINT				M14
		VCCINT				P11
		VCCINT				P12
		VCCINT				L9
		VCCINT				M9
		VCCINT				J13
		VCCINT				J14
		VCCINT				K14
		VCCINT				J10
		VCCINT				K9
		VCCINT				N9
		VCCINT				P9
		VCCINT				P10
		VCCINT				P13
		VCCINT				P14
		VCCINT				N14
		VCCINT				J16
		VCCINT				K15
		VCCINT				L16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		VCCINT				M15
		VCCINT				R12
		VCCINT				R10
		VCCINT				R8
		VCCINT				H9
		VCCINT				G12
		VCCINT				J8
		VCCINT				M8
		VCCINT				T7
		VCCINT				T9
		VCCINT				T13
		VCCINT				P15
		VCCINT				H15
		VCCINT				H11
		VCCINT				K8
		VCCINT				L7

Notes:
(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.

Date	Version	Changes
February 2017	2017.02.13	Initial release.
May 2017	2017.05.19	Updated description for the Configuration pins.
March 2019	2019.03.29	Added DPCLK and CDPCLK support in optional pin function column.